TEXAS INSTRUMENTS

DLPC3430, DLPC3435
DLPS038 – JULY 2014

DLPC343x Display Controller

1 Features

- Display Controller for DLP2010 (.2 WVGA) TRP DMD
  - Supports Input Image Sizes up to 720p
  - Low-Power DMD Interface with Interface Training
- 24-Bit, Input Pixel Interface Support:
  - Parallel or BT656, Interface Protocols
  - Pixel Clock up to 150 MHz
  - Multiple Input Pixel Data Format Options
- Pixel Data Processing:
  - IntelliBright™ Suite of Image Processing Algorithms
    - Content Adaptive Illumination Control
    - Local Area Brightness Boost
  - Image Resizing (Scaling)
  - 1D Keystone Correction
  - Color Coordinate Adjustment
  - Programmable Degamma
  - Active Power Management Processing
  - Color Space Conversion
  - 4:2:2 to 4:4:4 Chroma Interpolation
  - Field Scaled De-interlacing
- Two Package Options:
  - 176-Pin, 7- × 7-mm, 0.4-mm Pitch, VFBGA
  - 201-Pin, 13- × 13-mm, 0.8-mm Pitch, VFBGA
- External Flash Support
- Auto DMD Parking at Power Down
- Embedded Frame Memory (eDRAM)
- System Features:
  - I^2C Control of Device Configuration
  - Programmable Splash Screens
  - Programmable LED Current Control
  - Display Image Rotation
  - One Frame Latency

2 Applications

- Embedded Projection:
  - Smart Phone
  - Tablet
  - Camera
  - Camcorder
  - Laptop
- Battery-Powered Mobile Accessory
- Wearable (Near-Eye) Display
- Interactive Display
- Low-Latency Gaming Display
- Digital Signage

3 Description

The DLPC3430 and DLPC3435 digital controller, part of the DLP2010 (.2 WVGA) chipset, support reliable operation of the DLP2010 digital micromirror device (DMD). The DLPC343x controller provides a convenient, multi-functional interface between user electronics and the DMD, enabling small form factor and low power display applications.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLPC3430	VFBGA (176)	7.00×7.00 mm^2
DLPC3435	VFBGA (201)	13.00×13.00 mm^2

(1) For all available packages, see the orderable addendum at the end of the data sheet.
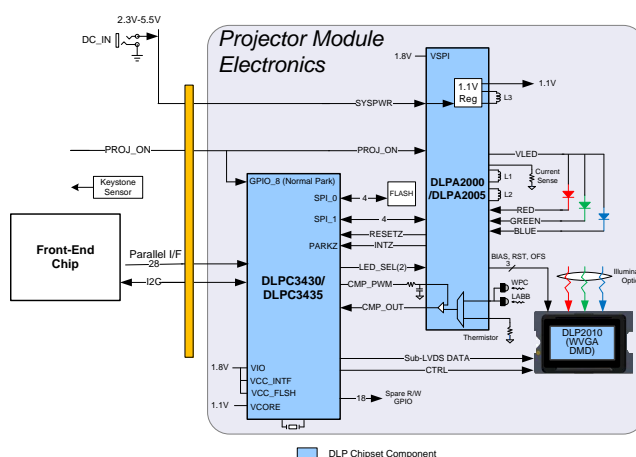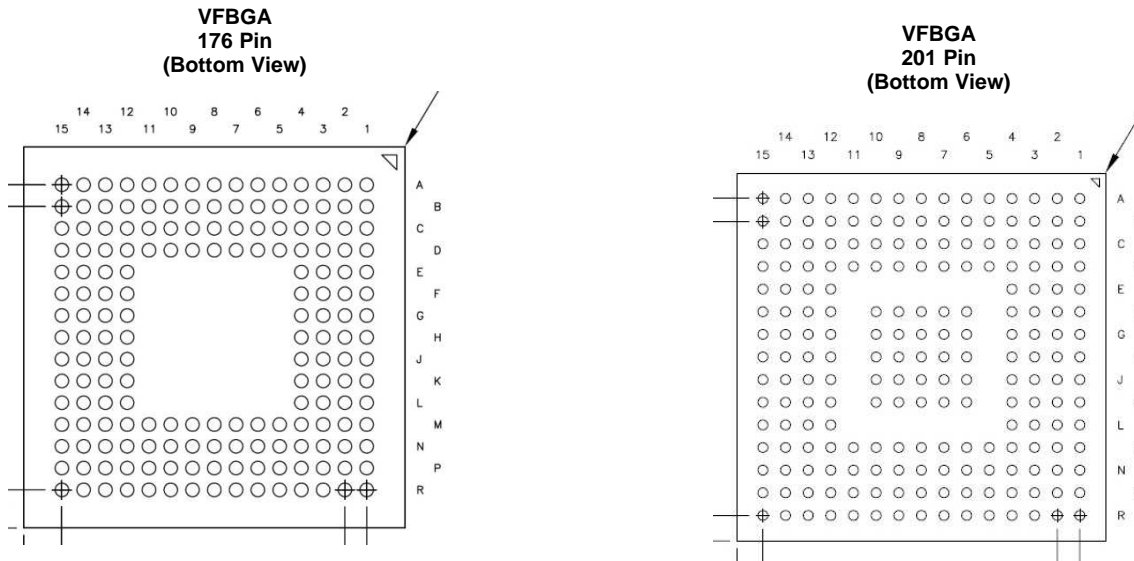
Typical Standalone System

Table of Contents

4 Revision History

DATE	REVISION	NOTES
July 2014	*	Initial release.

5 Pin Configuration and Functions

**VFBGA
176 Pin
(Bottom View)**

**VFBGA
201 Pin
(Bottom View)**

Pin Functions – Board Level Test, Debug, and Initialization

PIN		I/O	DESCRIPTION
NAME	NUMBER		
HWTEST_EN	C10	I_6	Manufacturing test enable signal. This signal should be connected directly to ground on the PCB for normal operation.
PARKZ	C13	I_6	DMD fast PARK control (active low Input) (hysteresis buffer). PARKZ must be set high to enable normal operation. PARKZ should be set high prior to releasing RESETZ (that is, prior to the low-to-high transition on the RESETZ input). PARKZ should be set low for a minimum of 40 µs before any power is removed from the DLPC343x such that the fast DMD PARK operation can be completed. Note for PARKZ, fast PARK control should only be used when loss of power is eminent and beyond the control of the host processor (for example, when the external power source has been disconnected or the battery has dropped below a minimum level). The longest lifetime of the DMD may not be achieved with the fast PARK operation. The longest lifetime is achieved with a normal PARK operation. Because of this, PARKZ is typically used in conjunction with a normal PARK request control input through GPIO_08. The difference being that when the host sets PROJ_ON low, which connects to both GPIO_08 and the DLPA2000 PMIC chip, the DLPC343x takes much longer than 40 µs to park the mirrors. The DLPA2000 holds on all power supplies, and keep RESETZ high, until the longer mirror parking has completed. This longer mirror parking time, of up to 500 µs, ensures the longest DMD lifetime and reliability. The DLPA2000 monitors power to the DLPC343x and detects an eminent power loss condition and drives the PARKZ signal accordingly.
Reserved	P12	I_6	TI internal use. Should be left unconnected.
Reserved	P13	I_6	TI internal use. Should be left unconnected.
Reserved	N13[1]	O_1	TI internal use. Should be left unconnected.
Reserved	N12[1]	O_1	TI internal use. Should be left unconnected.
Reserved	M13	I_6	TI internal use. Should be left unconnected.
Reserved	N11	I_6	TI internal use. Should be left unconnected.
Reserved	P11	I_6	TI internal use This pin must be tied to ground, through an external 8-kΩ, or less, resistor for normal operation. Failure to tie this pin low during normal operation will cause startup and initialization problems.

(1) If operation does not call for an external pullup and there is no external logic that might overcome the weak internal pulldown resistor, then this I/O can be left open or unconnected for normal operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown resistor is recommended to ensure a logic low.

Pin Functions – Board Level Test, Debug, and Initialization (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
RESETZ	C11	I_6	DLPC343x power-on reset (active low input) (hysteresis buffer). Self-configuration starts when a low-to-high transition is detected on RESETZ. All ASIC power and clocks must be stable before this reset is de-asserted. Note that the following signals will be tri-stated while RESETZ is asserted: SPI0_CLK, SPI0_DOUT, SPI0_CSZ0, SPI0_CSZ1, and GPIO(19:00) External pullups or downs (as appropriate) should be added to all tri-stated output signals listed (including bidirectional signals to be configured as outputs) to avoid floating ASIC outputs during reset if connected to devices on the PCB that can malfunction. For SPI, at a minimum, any chip selects connected to the devices should have a pullup. Unused bidirectional signals can be functionally configured as outputs to avoid floating ASIC inputs after RESETZ is set high. The following signals are forced to a logic low state while RESETZ is asserted and corresponding I/O power is applied: LED_SEL_0, LED_SEL_1 and DMD_DEN_ARSTZ No signals will be in their active state while RESETZ is asserted. Note that no I^2C activity is permitted for a minimum of 500 ms after RESETZ (and PARKZ) are set high.
TSTPT_0	R12	B_1	Test pin 0 (includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 μs after de-assertion of RESETZ, and then driven as an output. Normal use: reserved for test output. Should be left open or unconnected for normal use. Note: An external pullup should not be applied to this pin to avoid putting the DLPC343x in a test mode. Without external pullup [2] With external pullup [3] Feeds TMSEL(0) Feeds TMSEL(0)
TSTPT_1	R13	B_1	Test pin 1 (includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 μs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for test output. Should be left open or unconnected for normal use. Note: An external pullup should not be applied to this pin to avoid putting the DLPC343x in a test mode. Without external pullup [4] With external pullup [5] Feeds TMSEL(1) Feeds TMSEL(1)
TSTPT_2	R14	B_1	Test pin 2 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 μs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for test output. Should be left open or unconnected for normal use. Note: An external pullup should not be applied to this pin to avoid putting the DLPC343x in a test mode. Without external pullup [4] With external pullup [5] Feeds TMSEL(2) Feeds TMSEL(2)
TSTPT_3	R15	B_1	Test pin 3 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 μs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for for test output. Should be left open or unconnected for normal use.
TSTPT_4	P14	B_1	Test pin 4 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 μs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for for test output. Should be left open or unconnected for normal use.

(2) External pullup resistor must be 8 kΩ, or less, for pins with internal pullup or down resistors.
(3) If operation does not call for an external pullup and there is no external logic that might overcome the weak internal pulldown resistor, then the TSTPT I/O can be left open/ unconnected for normal operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown resistor is recommended to ensure a logic low.
(4) External pullup resistor must be 8 kΩ, or less, for pins with internal pullup or down resistors.
(5) If operation does not call for an external pullup and there is no external logic that might overcome the weak internal pulldown resistor, then the TSTPT I/O can be left open/ unconnected for normal operation. If operation does not call for an external pullup, but there is external logic that might overcome the weak internal pulldown resistor, then an external pulldown resistor is recommended to ensure a logic low.

Product Folder Links: *DLPC3430 DLPC3435*

Pin Functions – Board Level Test, Debug, and Initialization (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
TSTPT_5	P15	B_1	Test pin 5 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for test output. Should be left open or unconnected for normal use.
TSTPT_6	N14	B_1	Test pin 6 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for test output. should be left open or unconnected for normal use. Alternative use: none. External logic shall not unintentionally pull this pin high to avoid putting the DLPC343x in a test mode.
TSTPT_7	N15	B_1	Test pin 7 (Includes weak internal pulldown) – tri-stated while RESETZ is asserted low. Sampled as an input test mode selection control approximately 1.5 µs after de-assertion of RESETZ and then driven as an output. Normal use: reserved for test output. should be left open or unconnected for normal use.

Submit Documentation Feedback   5

Product Folder Links: *DLPC3430 DLPC3435*

Pin Functions – Parallel Port Input Data and Control[1][2]

PIN		I/O	DESCRIPTION	
NAME	NUMBER		PARALLEL RGB MODE	BT656 INTERFACE MODE
PCLK	P3	I_{11}	Pixel clock[3]	Pixel clock[3]
PDM_CVS_TE	N4	B_5	Parallel data mask[4]	Unused[5]
VSYNC_WE	P1	I_{11}	Vsync[6]	Unused[5]
HSYNC_CS	N5	I_{11}	Hsync[6]	Unused[5]
DATAEN_CMD	P2	I_{11}	Data Valid[6]	Unused[5]
PDATA_0 PDATA_1 PDATA_2 PDATA_3 PDATA_4 PDATA_5 PDATA_6 PDATA_7	K2 K1 L2 L1 M2 M1 N2 N1	I_{11}	**(TYPICAL RGB 888)** Blue (bit weight 1) Blue (bit weight 2) Blue (bit weight 4) Blue (bit weight 8) Blue (bit weight 16) Blue (bit weight 32) Blue (bit weight 64) Blue (bit weight 128)	BT656_Data (0) BT656_Data (1) BT656_Data (2) BT656_Data (3) BT656_Data (4) BT656_Data (5) BT656_Data (6) BT656_Data (7)
PDATA_8 PDATA_9 PDATA_10 PDATA_11 PDATA_12 PDATA_13 PDATA_14 PDATA_15	R1 R2 R3 P4 R4 P5 R5 P6	I_{11}	**(TYPICAL RGB 888)** Green (bit weight 1) Green (bit weight 2) Green (bit weight 4) Green (bit weight 8) Green (bit weight 16) Green (bit weight 32) Green (bit weight 64) Green (bit weight 128)	Unused
PDATA_16 PDATA_17 PDATA_18 PDATA_19 PDATA_20 PDATA_21 PDATA_22 PDATA_23	R6 P7 R7 P8 R8 P9 R9 P10	I_{11}	**(TYPICAL RGB 888)** Red (bit weight 1) Red (bit weight 2) Red (bit weight 4) Red (bit weight 8) Red (bit weight 16) Red (bit weight 32) Red (bit weight 64) Red (bit weight 128)	Unused
3DR	N6		3D reference • For 3D applications: left or right 3D reference (left = 1, right = 0). To be provided by the host when a 3D command is not provided. Must transition in the middle of each frame (no closer than 1 ms to the active edge of VSYNC) • If a 3D application is not used, then this input should be pulled low through an external resistor.	

(1) PDATA(23:0) bus mapping is pixel format and source mode dependent. See later sections for details.
(2) PDM_CVS_TE is optional for parallel interface operation. If unused, inputs should be grounded or pulled down to ground through an external resistor (8 kΩ or less).
(3) Pixel clock capture edge is software programmable.
(4) The parallel data mask signal input is optional for parallel interface operations. If unused, inputs should be grounded or pulled down to ground through an external resistor (8 kΩ or less).
(5) Unused inputs should be grounded or pulled down to ground through an external resistor (8 kΩ or less).
(6) VSYNC, HSYNC, and DATAEN polarity is software programmable.

Product Folder Links: *DLPC3430 DLPC3435*

Pin Functions – DMD Reset and Bias Control

PIN		I/O	DESCRIPTION
NAME	NUMBER		
DMD_DEN_ARSTZ	B1	O_2	DMD driver enable (active high)/ DMD reset (active low). Assuming the corresponding I/O power is supplied, this signal will be driven low after the DMD is parked and before power is removed from the DMD. If the 1.8-V power to the DLPC343x is independent of the 1.8-V power to the DMD, then TI recommends a weak, external pulldown resistor to hold the signal low in the event DLPC343x power is inactive while DMD power is applied.
DMD_LS_CLK	A1	O_3	DMD, low speed interface clock
DMD_LS_WDATA	A2	O_3	DMD, low speed serial write data
DMD_LS_RDATA	B2	I_6	DMD, low speed serial read data

Pin Functions – DMD Sub-LVDS Interface

PIN		I/O	DESCRIPTION
NAME	NUMBER		
DMD_HS_CLK_P DMD_HS_CLK_N	A7 B7	O_4	DMD high speed interface
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	A3 B3 A4 B4 A5 B5 A6 B6 A8 B8 A9 B9 A10 B10 A11 B11	O_4	DMD high speed interface lanes, write data bits: (The true numbering and application of the DMD_HS_DATA pins are software configuration dependent)

Pin Functions – Peripheral Interface[1]

PIN		I/O	DESCRIPTION
NAME	NUMBER		
CMP_OUT	A12	I_6	Successive approximation ADC comparator output (DLPC343x Input). Assumes a successive approximation ADC is implemented with a WPC light sensor and/or a thermistor feeding one input of an external comparator and the other side of the comparator is driven from the ASIC's CMP_PWM pin. Should be pulled-down to ground if this function is not used. (hysteresis buffer)
CMP_PWM	A15	O_1	Successive approximation comparator pulse-duration modulation (output). Supplies a PWM signal to drive the successive approximation ADC comparator used in WPC light-to-voltage sensor applications. Should be left unconnected if this function is not used.
HOST_IRQ[2]	N8	O_9	Host interrupt (output) This signal has two primary uses. The first use is to indicate when DLPC343x auto-initialization is in progress and most importantly when it completes. The second is to indicate when service is requested (that is an interrupt request). The DLPC343x tri-states this output during reset and assumes that an external pullup is in place to drive this signal to its inactive state.
IIC0_SCL	N10	B_7	I^2C slave (port 0) SCL (bidirectional, open-drain signal with input hysteresis): An external pullup is required. The slave I^2C I/Os are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^2C pullups must be connected to an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage would not likely satisfy the VIH specification of the slave I^2C input buffers).
Reserved	R11	B_8	TI internal use. TI recommends an external pullup resistor.
IIC0_SDA	N9	B_7	I^2C slave (port 0) SDA. (bidirectional, open-drain signal with input hysteresis): An external pullup is required. The slave I^2C port is the control port of ASIC. The slave I^2C I/Os are 3.6-V tolerant (high-volt-input tolerant) and are powered by VCC_INTF (which can be 1.8, 2.5, or 3.3 V). External I^2C pullups must be connected to an equal or higher supply voltage, up to a maximum of 3.6 V (a lower pullup supply voltage would not likely satisfy the VIH specification of the slave I^2C input buffers).
Reserved	R10	B_8	TI internal use. TI recommends an external pullup resistor.
LED_SEL_0	B15	O_1	LED enable select. Controlled by programmable DMD sequence Timing Enabled LED LED_SEL(1:0) DLPA2000 application 00 None 01 Red 10 Green 11 Blue
LED_SEL_1	B14	O_1	These signals will be driven low when RESETZ is asserted and the corresponding I/O power is supplied. They will continue to be driven low throughout the auto-initialization process. A weak, external pulldown resistor is still recommended to ensure that the LEDs are disabled when I/O power is not applied.
SPI0_CLK	A13	O_{13}	Synchronous serial port 0, clock
SPI0_CSZ0	A14	O_{13}	SPI port 1, chip select 0 (active low output) TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during ASIC reset assertion.
SPI0_CSZ1	C12	O_{13}	SPI port 1, chip select 1 (active low output) TI recommends an external pullup resistor to avoid floating inputs to the external SPI device during ASIC reset assertion.
SPI0_DIN	B12	I_{12}	Synchronous serial port 0, receive data in
SPI0_DOUT	B13	O_{13}	Synchronous serial port 0, transmit data out

(1) External pullup resistor must be 8 kΩ or less.
(2) For more information about usage, see *HOST_IRQ Usage Model*.

Pin Functions – GPIO Peripheral Interface[1]

PIN		I/O	DESCRIPTION[2]
NAME	NUMBER		
GPIO_19	M15	B_1	General purpose I/O 19 (hysteresis buffer). Options: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). 2. KEYPAD_4 (input): keypad applications
GPIO_18	M14	B_1	General purpose I/O 18 (hysteresis buffer). Options: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). 2. KEYPAD_3 (input): keypad applications
GPIO_17	L15	B_1	General purpose I/O 17 (hysteresis buffer). Options: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). 2. KEYPAD_2 (input): keypad applications
GPIO_16	L14	B_1	General purpose I/O 16 (hysteresis buffer). Options: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). 2. KEYPAD_1 (input): keypad applications
GPIO_15	K15	B_1	General purpose I/O 15 (hysteresis buffer). Options: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input). 2. KEYPAD_0 (input): keypad applications
GPIO_14	K14	B_1	General purpose I/O 14 (hysteresis buffer). Options: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_13	J15	B_1	General purpose I/O 13 (hysteresis buffer). Options: 1. CAL_PWR (output): Intended to feed the calibration control of the successive approximation ADC light sensor. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_12	J14	B_1	General purpose I/O 12 (hysteresis buffer). Options: 1. (Output) power enable control for LABB light sensor. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_11	H15	B_1	General purpose I/O 11 (hysteresis buffer). Options: 1. (Output): thermistor power enable. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_10	H14	B_1	General Purpose I/O 10 (hysteresis buffer). Options: 1. RC_CHARGE (output): Intended to feed the RC charge circuit of the successive approximation ADC used to control the light sensor comparator. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_09	G15	B_1	General purpose I/O 09 (hysteresis buffer). Options: 1. LS_PWR (active high output): Intended to feed the power control signal of the successive approximation ADC light sensor. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).

(1) GPIO signals must be configured through software for input, output, bidirectional, or open-drain. Some GPIO have one or more alternative use modes, which are also software configurable. The reset default for all GPIO is as an input signal. An external pullup is required for each signal configured as open-drain.
(2) DLPC343x general purpose I/O. These GPIO are software configurable.

Pin Functions – GPIO Peripheral Interface(1) (continued)

PIN		I/O	DESCRIPTION(2)
NAME	NUMBER		
GPIO_08	G14	B₁	General purpose I/O 08 (hysteresis buffer). Options: 1. (All) Normal mirror parking request (active low): To be driven by the PROJ_ON output of the host. A logic low on this signal will cause the DLPC343x to PARK the DMD, but it will not power down the DMD (the DLPA2000 does that instead). The minimum high time is 200 ms. The minimum low time is also 200 ms.
GPIO_07	F15	B₁	General purpose I/O 07 (hysteresis buffer). Options: 1. (All) LED_ENABLE (active high input). This signal can be used as an optional shutdown interlock for the LED driver. Specifically, when so configured, setting LED_ENABLE = 0 (disabled), will cause LDEDRV_ON to be forced to 0 and LED_SEL(2:0) to be forced to b000. Otherwise when LED_ENABLE = 1 (enabled), the ASIC is free to control the LED SEL signals as it desires. There is however a 100-ms delay after LED_ENABLE transitions from low-to-high before the interlock is released. 2. (Output): LABB output sample and hold sensor control signal. 3. (All) GPIO (bidirectional): Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_06	F14	B₁	General purpose I/O 06 (hysteresis buffer). Option: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used. An external pulldown resistor is required to deactivate this signal during reset and auto-initialization processes.
GPIO_05	E15	B₁	General purpose I/O 05 (hysteresis buffer). Options: 1. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_04	E14	B₁	General purpose I/O 04 (hysteresis buffer). Options: 1. 3D glasses control (output): intended to be used to control the shutters on 3D glasses (Left = 1, Right = 0). 2. SPI1_CSZ1 (active-low output): optional SPI1 chip select 1 signal. An external pullup resistor is required to deactivate this signal during reset and auto-initialization processes. 3. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_03	D15	B₁	General purpose I/O 03 (hysteresis buffer). Options: 1. SPI1_CSZ0 (active low output): Optional SPI1 chip select 0 signal. An external pullup resistor is required to deactivate this signal during reset and auto-initialization processes. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_02	D14	B₁	General purpose I/O 02 (hysteresis buffer). Options: 1. SPI1_DOUT (output): Optional SPI1 data output signal. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_01	C15	B₁	General purpose I/O 01 (hysteresis buffer). Options: 1. SPI1_CLK (output): Optional SPI1 clock signal. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).
GPIO_00	C14	B₁	General purpose I/O 00 (hysteresis buffer). Options: 1. SPI1_DIN (input): Optional SPI1 data input signal. 2. Optional GPIO. Should be configured as a logic zero GPIO output and left unconnected if not used (otherwise it will require an external pullup or pulldown to avoid a floating GPIO input).

Pin Functions – Clock and PLL Support

PIN		I/O	DESCRIPTION
NAME	NUMBER		
PLL_REFCLK_I	H1	I_{11}	Reference clock crystal input. If an external oscillator is used in place of a crystal, then this pin should be used as the oscillator input.
PLL_REFCLK_O	J1	O_5	Reference clock crystal return. If an external oscillator is used in place of a crystal, then this pin should be left unconnected (that is floating with no added capacitive load).

Pin Functions – Power and Ground[1]

PIN		I/O	DESCRIPTION
NAME	NUMBER		
VDD	C5, D5, D7, D12, J4, J12, K3, L4, L12, M6, M9, D9, D13, F13, H13, L13, M10, D3, E3	PWR	Core power 1.1 V (main 1.1 V)
VDDLP12	C3	PWR	Core power 1.1 V
VSS	Common to all package types C4, D6, D8, D10, E4, E13, F4, G4, G12, H4, H12, J3, J13, K4, K12, L3, M4, M5, M8, M12, G13, C6, C8 Only available on DLPC343x F6, F7, F8, F9, F10, G6, G7, G8, G9, G10, H6, H7, H8, H9, H10, J6, J7, J8, J9, J10, K6, K7, K8, K9, K10	GND	Core ground (eDRAM, I/O ground, thermal ground)
VCC18	C7, C9, D4, E12, F12, K13, M11	PWR	All 1.8-V I/O power: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ LED_SEL, CMP, GPIO, IIC1, TSTPT, and JTAG pins)
VCC_INTF	M3, M7, N3, N7	PWR	Host or parallel interface I/O power: 1.8 to 3.3 V (Includes IIC0, PDATA, video syncs, and HOST_IRQ pins)
VCC_FLSH	D11	PWR	Flash interface I/O power:1.8 to 3.3 V (Dedicated SPI0 power pin)
VDD_PLLM	H2	PWR	MCG PLL 1.1-V power
VSS_PLLM	G3	RTN	MCG PLL return
VDD_PLLD	J2	PWR	DCG PLL 1.1-V power
VSS_PLLD	H3	RTN	DCG PLL return

(1) The only power sequencing restrictions are:
  (a) The VDDLP12 supply must be powered-on at exactly the same time or after the VDD11 supply.
  (b) The VDD11 supply should ramp up with a 1-ms minimum rise time.
  (c) The reverse is needed at power down.

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
SUPPLY VOLTAGE[2][3]				
$V_{(VDD)}$ (core)		−0.3	1.21	V
$V_{(VDDLP12)}$ (core)		−0.3	1.32	
Power + sub-LVDS		−0.3	1.96	
$V_{(VCC\_INTF)}$	Host I/O power	−0.3	3.60	
	If 1.8-V power used	−0.3	1.99	
	If 2.5-V power used	−0.3	2.75	
	If 3.3-V power used	−0.3	3.60	
$V_{(VCC\_FLSH)}$	Flash I/O power	−0.3	3.60	
	If 1.8-V power used	−0.3	1.96	
	If 2.5-V power used	−0.3	2.72	
	If 3.3-V power used	−0.3	3.58	
$V_{(VDD\_PLLM)}$ (MCG PLL)		−0.3	1.21	
$V_{(VDD\_PLLD)}$ (1DCG PLL)		−0.3	1.21	
GENERAL				
T_J	Operating junction temperature	−30	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Overlap currents, if allowed to continue flowing unchecked, not only increase total power dissipation in a circuit, but degrade the circuit reliability, thus shortening its usual operating life.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−40	125	°C
$V_{(ESD)}$[1]	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[2]	−2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[3]	−500	500	

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
$V_{(VDD)}$	Core power 1.1 V (main 1.1 V)	±5% tolerance	1.045	1.1	1.155	V
$V_{(VDDLP12)}$	Core power 1.1 V	±5% tolerance See [1]	1.02	1.1	1.18	V
			1.12	1.2	1.28	
$V_{(VCC18)}$	All 1.8-V I/O power: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ LED_SEL, CMP, GPIO, IIC1, TSTPT, and JTAG pins.)	±8.5% tolerance	1.64	1.8	1.96	V
$V_{(VCC\_INTF)}$	Host or parallel interface I/O power: 1.8 to 3.3 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins)	±8.5% tolerance See [1]	1.64	1.8	1.96	V
			2.28	2.5	2.72	
			3.02	3.3	3.58	
$V_{(VCC\_FLSH)}$	Flash interface I/O power:1.8 to 3.3 V	±8.5% tolerance See [1]	1.64	1.8	1.96	V
			2.28	2.5	2.72	
			3.02	3.3	3.58	
$V_{(VDD\_PLLM)}$	MCG PLL 1.1-V power	±9.1% tolerance See [2]	1.025	1.1	1.155	V
$V_{(VDD\_PLLD)}$	DCG PLL 1.1-V power	±9.1% tolerance See [2]	1.025	1.1	1.155	V
T_A	Operating ambient temperature range[3]		−30		85	°C
T_C	Operating top-center case temperature					°C

(1) These supplies have multiple valid ranges.
(2) These I/O supply ranges are wider to facilitate additional filtering.
(3) The operating ambient temperature range assumes 0 forced air flow, a JEDEC JESD51 junction-to-ambient thermal resistance value at 0 forced air flow ($R_{\theta JA}$ at 0 m/s), a JEDEC JESD51 standard test card and environment, along with min and max estimated power dissipation across process, voltage, and temperature. Thermal conditions vary by application, which will impact $R_{\theta JA}$. Thus, maximum operating ambient temperature varies by application.
    (a) $T_{a\_min} = T_{j\_min} − (P_{d\_min} \times R_{\theta JA}) = −30°C − (0.0W \times 30.3°C/W) = −30°C$
    (b) $T_{a\_max} = T_{j\_max} − (P_{d\_max} \times R_{\theta JA}) = +105°C − (0.348W \times 30.3°C/W) = +94.4°C$

6.4 Thermal Information

THERMAL METRIC[1]		VFBGA		UNIT
		176 PINS	**201 PINS**	
$R_{\theta JC}$	Junction-to-case thermal resistance	11.2	10.1	°C/W
$R_{\theta JA}$ at 0 m/s of forced airflow[2]	Junction-to-air thermal resistance	30.3	28.8	
$R_{\theta JA}$ at 1 m/s of forced airflow[2]	Junction-to-air thermal resistance	27.4	25.3	
$R_{\theta JA}$ at 2 m/s of forced airflow[2]	Junction-to-air thermal resistance	26.6	24.4	
ψ_{JT}[3]	Temperature variance from junction to package top center temperature, per unit power dissipation	.27	.23	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal coefficients abide by JEDEC Standard 51. $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC350 PCB and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different , it is the best information available during the design phase to estimate thermal performance.
(3) Example: (0.5 W) × (0.2 C/W) ≈ 1.00°C temperature rise.

6.5 Electrical Characteristics over Recommended Operating Conditions [1][2][3][4][5][6][7]

PARAMETER		TEST CONDITIONS[8]	MIN	TYP[6][7]	MAX[9][7]	UNIT
$V_{(VDD)}$	Core current 1.1 V (main 1.1 V)	IDLE disabled, WVGA, 60 Hz		112	232.2	mA
		IDLE enabled, WVGA, 60 Hz		85		
		IDLE disabled, WVGA, 120 Hz			252.9	
$V_{(VDD\_PLLM)}$	MCG PLL 1.1-V current	IDLE disabled, WVGA, 60 Hz		112	6	mA
		IDLE enabled, WVGA, 60 Hz		85		
		IDLE disabled, WVGA, 120 Hz			6	
$V_{(VDD\_PLLD)}$	DCG PLL 1.1-V current	IDLE disabled, WVGA, 60 Hz		112	6	mA
		IDLE enabled, WVGA, 60 Hz		85		
		IDLE disabled, WVGA, 120 Hz			6	
$V_{(VCC18)}$	All 1.8-V I/O current: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface. This includes sub-LVDS DMD I/O, RESETZ, PARKZ LED_SEL, CMP, GPIO, IIC1, TSTPT, and JTAG pins)	IDLE disabled, WVGA, 60 Hz		13		mA
		IDLE enabled, WVGA, 60 Hz		13		
		IDLE disabled, WVGA, 120 Hz			12.62	
$V_{(VCC\_INTF)}$	Host or parallel interface I/O current: 1.8 to 3.3 V (includes IIC0, PDATA, video syncs, and HOST_IRQ pins)	IDLE disabled, WVGA, 60 Hz			1.5	mA
		IDLE disabled, WVGA, 120 Hz			1.5	
$V_{(VCC\_FLSH)}$	Flash interface I/O current:1.8 to 3.3 V	IDLE disabled, WVGA, 60 Hz			1.01	mA
		IDLE disabled, WVGA, 120 Hz			1.01	

(1) Assumes 12.5% activity factor, 30% clock gating on appropriate domains, and mixed SVT or HVT cells
(2) Programmable host and flash I/O are at minimum voltage (that is 1.8 V) for this typical scenario.
(3) Max currents column use typical motion video as the input. The typical currents column uses SMPTE color bars as the input.
(4) Some applications (that is, high-resolution 3D) may be forced to use 1-oz copper to manage ASIC package heat.
(5) For the typical cases, all pins using 1.8 V are tied together as are 1.1-V pins, and the current specified is for the collective 1.8-V and 1.1-V current.
(6) Assumes typical case power PVT condition = nominal process, typical voltage, typical temperature (55°C junction). WVGA resolution.
(7) Input image is 854 × 480 (WVGA) 24-bits on the parallel interface at the frame rate shown with 0.2-inch WVGA DMD.
(8) In normal mode
(9) Assumes worse case power PVT condition = corner process, high voltage, high temperature (105°C junction), WVGA resolution

Product Folder Links: *DLPC3430 DLPC3435*

6.6 Electrical Characteristics[1][2]

over operating free-air temperature range (unless otherwise noted)

PARAMETER[3]			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	I²C buffer (I/O type 7)		0.7 × VCC_INTF		[1]	V
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		1.17		3.6	
		1.8-V LVTTL (I/O type 1, 6) identified below: (2) CMP_OUT; PARKZ; RESETZ; GPIO 0 →19		1.3		3.6	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		1.7		3.6	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		2		3.6	
V_{IL}	Low-level input threshold voltage	I²C buffer (I/O type 7)		−0.5		0.3 × VCC_INTF	V
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		−0.3		0.63	
		1.8-V LVTTL (I/O type 1, 6) identified below: (2) CMP_OUT; PARKZ; RESETZ; GPIO_00 through GPIO_19		−0.3		0.5	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		−0.3		0.7	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		−0.3		0.8	
V_{CM}	Steady-state common mode voltage	1.8 sub-LVDS (DMD high speed) (I/O type 4)		0.8	0.9	1	mV
$|V_{OD}|$	Differential output magnitude	1.8 sub-LVDS (DMD high speed) (I/O type 4)			200		mV
V_{OH}	High-level output voltage	1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		1.35			V
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		1.7			
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		2.4			
		1.8 sub-LVDS – DMD high speed (I/O type 4)			1		
V_{OL}	Low-level output voltage	I²C buffer (I/O type 7)	VCC_INTF > 2 V			0.4	V
		I²C buffer (I/O type 7)	VCC_INTF < 2 V			0.2 × VCC_INTF	
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)				0.45	
		2.5 V LVTTL (I/O type 5, 9, 11, 12, 13)				0.7	
		3.3 V LVTTL (I/O type 5, 9, 11, 12, 13)				0.4	
		1.8 sub-LVDS – DMD high speed (I/O type 4)			0.8		

(1) I/O is high voltage tolerant; that is, if VCC = 1.8 V, the input is 3.3-V tolerant, and if VCC = 3.3 V, the input is 5-V tolerant.
(2) ASIC pins: CMP_OUT; PARKZ; RESETZ; GPIO_00 through GPIO_19 have slightly varied V_{IH} and V_{IL} range from other 1.8-V I/O.
(3) The number inside each parenthesis for the I/O refers to the type defined in Table 1.

Electrical Characteristics[(1)(2)] (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER[(3)]			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH}	High-level output current	1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	4 mA	2			mA
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	8 mA	3.5			
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	24 mA	10.6			
		2.5-V LVTTL (I/O type 5)	4 mA	5.4			
		2.5-V LVTTL (I/O type 9, 13)	8 mA	10.8			
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)	24 mA	28.7			
		3.3-V LVTTL (I/O type 5)	4 mA	7.8			
		3.3-V LVTTL (I/O type 9, 13)	8 mA	15			
I_{OL}	Low-level output current	I²C buffer (I/O type 7)		3			mA
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	4 mA	2.3			
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	8 mA	4.6			
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)	24 mA	13.9			
		2.5-V LVTTL (I/O type 5)	4 mA	5.2			
		2.5-V LVTTL (I/O type 9, 13)	8 mA	10.4			
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)	24 mA	31.1			
		3.3-V LVTTL (I/O type 5)	4 mA	4.4			
		3.3-V LVTTL (I/O type 9, 13)	8 mA	8.9			
I_{OZ}	High-impedance leakage current	I²C buffer (I/O type 7)	0.1 × VCC_INTF < VI < 0.9 × VCC_INTF	−10		10	µA
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)		−10		10	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)		−10		10	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)		−10		10	
C_I	Input capacitance (including package)	I²C buffer (I/O type 7)				5	pF
		1.8-V LVTTL (I/O type 1, 2, 3, 5, 6, 8, 9, 11, 12, 13)			2.6	3.5	
		2.5-V LVTTL (I/O type 5, 9, 11, 12, 13)			2.6	3.5	
		3.3-V LVTTL (I/O type 5, 9, 11, 12, 13)			2.6	3.5	
		1.8 sub-LVDS – DMD high speed (I/O type 4)				3	

Product Folder Links: *DLPC3430 DLPC3435*

Table 1. I/O Type Subscript Definition

I/O		SUPPLY REFERENCE	ESD STRUCTURE
SUBSCRIPT	DESCRIPTION		
1	1.8 LVCMOS I/O buffer with 8-mA drive	V_{cc18}	ESD diode to GND and supply rail
2	1.8 LVCMOS I/O buffer with 4-mA drive	V_{cc18}	ESD diode to GND and supply rail
3	1.8 LVCMOS I/O buffer with 24-mA drive	V_{cc18}	ESD diode to GND and supply rail
4	1.8 sub-LVDS output with 4-mA drive	V_{cc18}	ESD diode to GND and supply rail
5	1.8, 2.5, 3.3 LVCMOS with 4-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
6	1.8 LVCMOS input	V_{cc18}	ESD diode to GND and supply rail
7	1.8-, 2.5-, 3.3-V I^2C with 3-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
8	1.8-V I^2C with 3-mA drive	V_{cc18}	ESD diode to GND and supply rail
9	1.8-, 2.5-, 3.3-V LVCMOS with 8-mA drive	V_{cc_INTF}	ESD diode to GND and supply rail
11	1.8, 2.5, 3.3 LVCMOS input	V_{cc_INTF}	ESD diode to GND and supply rail
12	1.8-, 2.5-, 3.3-V LVCMOS input	V_{cc_FLSH}	ESD diode to GND and supply rail
13	1.8-, 2.5-, 3.3-V LVCMOS with 8-mA drive	V_{cc_FLSH}	ESD diode to GND and supply rail

Table 2. Internal Pullup and Pulldown Characteristics[1][2]

| INTERNAL PULLUP AND PULLDOWN RESISTOR CHARACTERISTICS	VCCIO =	MIN	MAX	UNIT
Weak pullup resistance	3.3 V	29	63	kΩ
	2.5 V	38	90	kΩ
	1.8 V	56	148	kΩ
Weak pulldown resistance	3.3 V	30	72	kΩ
	2.5 V	36	101	kΩ
	1.8 V	52	167	kΩ

(1) The resistance is dependent on the supply voltage level applied to the I/O.
(2) An external 8-kΩ pullup or pulldown (if needed) would work for any voltage condition to correctly pull enough to override any associated internal pullups or pulldowns.

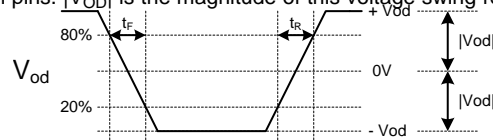## 6.7 High-Speed Sub-LVDS Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{CM}	Steady-state common mode voltage	0.8	0.9	1.0	V
V_{CM} (Δpp)[1]	V_{CM} change peak-to-peak (during switching)			75	mV
V_{CM} (Δss)[1]	V_{CM} change steady state	−10		10	mV
$|V_{OD}|$[2]	Differential output voltage magnitude		200		mV
V_{OD} (Δ)	V_{OD} change (between logic states)	−10		10	mV
V_{OH}	Single-ended output voltage high		1.00		V
V_{OL}	Single-ended output voltage low		0.80		V
t_R[2]	Differential output rise time			250	ps
t_F[2]	Differential output fall time			250	ps
t_{MAX}	Max switching rate			1200	Mbps
DCout	Output duty cycle	45%	50%	55%	
Tx_{term}[1]	Internal differential termination	80	100	120	Ω
Tx_{load}	100-Ω differential PCB trace (50-Ω transmission lines)	0.5		6	inches
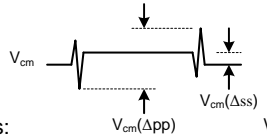
(1) Definition of V_{CM} changes:

(2) Note that V_{OD} is the differential voltage swing measured across a 100-Ω termination resistance connected directly between the transmitter differential pins. $|V_{OD}|$ is the magnitude of this voltage swing relative to 0. Rise and fall times are defined for the differential

Differential Output Signal

V_{OD} signal as follows: (Note Vcm is removed when the signals are viewed differentially)

Product Folder Links: *DLPC3430 DLPC3435*

6.8 Low-Speed SDR Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	ID	TEST CONDITIONS	MIN	MAX	UNIT
Operating voltage	VCC18 (all signal groups)		1.64	1.96	V
DC input high voltage	VIHD(DC) Signal group 1	All	0.7 × VCC18	VCC18 + 0.5	V
DC input low voltage[1]	VILD(DC) Signal group 1	All	−0.50	0.3 × VCC18	V
AC input high voltage[2]	VIHD(AC) Signal group 1	All	0.8 × VCC18	VCC18 + 0.5	V
AC input low voltage	VILD(AC) Signal group 1	All	−0.5	0.2 × VCC18	V
Slew rate [3][4][5][6]	Signal group 1		1	3.0	V/ns
	Signal group 2		0.25		
	Signal group 3		0.5		

(1) VILD(AC) min applies to undershoot.
(2) VIHD(AC) max applies to overshoot.
(3) Signal group 1 output slew rate for rising edge is measured between VILD(DC) to VIHD(AC).
(4) Signal group 1 output slew rate for falling edge is measured between VIHD(DC) to VILD(AC).
(5) Signal group 1: See Figure 1.
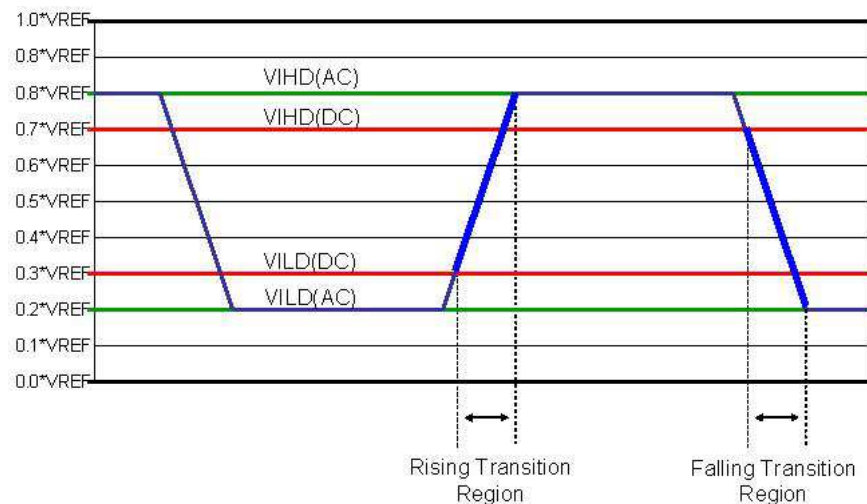(6) Signal groups 2 and 3 output slew rate for rising edge is measured between VILD(AC) to VIHD(AC).

Figure 1. Low Speed (LS) I/O Input Thresholds

6.9 System Oscillators Timing Requirements[1]

NUMBER		PARAMETER		MIN	MAX	UNIT
1a	f_{clock}	Clock frequency, MOSC[2]	Option 1: 24-MHz oscillator	23.998	24.002	MHz
1a	t_c	Cycle time, MOSC[2]	Option 1: 24-MHz oscillator	41.670	41.663	ns
1b	f_{clock}	Clock frequency, MOSC[2]	Option 2: 16-MHz oscillator	15.998	16.002	MHz
1b	t_c	Cycle time, MOSC[2]	Option 2: 16-MHz oscillator	62.508	62.492	ns
2	$t_{w(H)}$	Pulse duration[3], MOSC, high	50% to 50% reference points (signal)		40 t_c%	
3	$t_{w(L)}$	Pulse duration[3], MOSC, low	50% to 50% reference points (signal)		40 t_c%	
4	t_t	Transition time[3], MOSC, $t_t = t_f / t_r$	20% to 80% reference points (signal)		10	ns
5	t_{jp}	Long-term, peak-to-peak, period jitter[3], MOSC (that is the deviation in period from ideal period due solely to high frequency jitter)			2%	

(1) The I/O pin TSTPT_6 enables the ASIC to use two different oscillator frequencies through a pullup control at initial ASIC power-up. If a pullup is applied to this pin then a 16.0-MHz oscillator option must be used instead of the 24-MHz option shown.
(2) The frequency accuracy for MOSC is ±200 PPM. (This includes impact to accuracy due to aging, temperature, and trim sensitivity.) The MOSC input cannot support spread spectrum clock spreading.
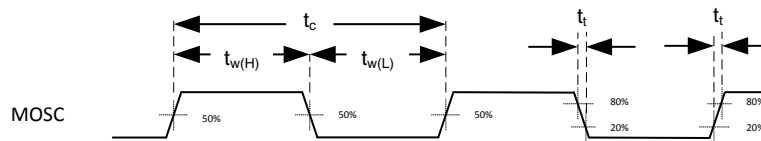(3) Applies only when driven through an external digital oscillator.

Figure 2. System Oscillators

6.10 Power-Up and Reset Timing Requirements

NUMBER		PARAMETER		MIN	MAX	UNIT
1	$t_{w(L)}$	Pulse duration, inactive low, RESETZ	50% to 50% reference points (signal)	1.25		µs
2	t_t	Transition time, RESETZ[1], $t_t = t_f / t_r$	20% to 80% reference points (signal)		0.5	µs

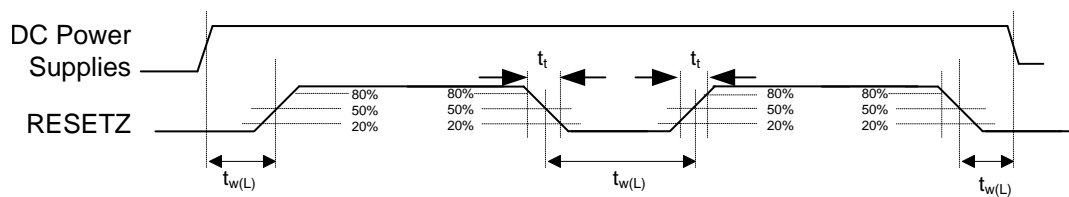(1) For more information on RESETZ, see *Pin Configuration and Functions*.

Figure 3. Power-Up and Power-Down RESETZ Timing

Product Folder Links: *DLPC3430 DLPC3435*

6.11 Parallel Interface Frame Timing Requirements

PARAMETER			MIN	MAX	UNIT
t_{p_vsw}	Pulse duration – VSYNC_WE high	50% reference points	1		lines
t_{p_vbp}	Vertical back porch (VBP) – time from the leading edge of VSYNC_WE to the leading edge HSYNC_CS for the first active line (see [1])	50% reference points	2		lines
t_{p_vfp}	Vertical front porch (VFP) – time from the leading edge of the HSYNC_CS following the last active line in a frame to the leading edge of VSYNC_WE (see [1])	50% reference points	1		lines
t_{p_tvb}	Total vertical blanking – time from the leading edge of HSYNC_CS following the last active line of one frame to the leading edge of HSYNC_CS for the first active line in the next frame. (This is equal to the sum of VBP (t_{p_vbp}) + VFP (t_{p_vfp}).)	50% reference points	See [1]		lines
t_{p_hsw}	Pulse duration – HSYNC_CS high	50% reference points	4	128	PCLKs
t_{p_hbp}	Horizontal back porch – time from rising edge of HSYNC_CS to rising edge of DATAEN_CMD	50% reference points	4		PCLKs
t_{p_hfp}	Horizontal front porch – time from falling edge of DATAEN_CMD to rising edge of HSYNC_CS	50% reference points	8		PCLKs
t_{p_thb}	Total horizontal blanking – sum of horizontal front and back porches	50% reference points	See [2]		PCLKs

(1) The minimum total vertical blanking is defined by the following equation: $t_{p\_tvb}(min) = 6 + [6 \times Max(1, Source\_ALPF/ DMD\_ALPF)]$ lines
   where:
   (a) SOURCE_ALPF = Input source active lines per frame
   (b) DMD_ALPF = Actual DMD used lines per frame supported
(2) Total horizontal blanking is driven by the max line rate for a given source which will be a function of resolution and orientation. The following equation can be applied for this: $t_{p\_thb} = Roundup[(1000 \times f_{clock})/ LR] – APPL$
   where:
   (a) f_{clock} = Pixel clock rate in MHz
   (b) LR = Line rate in kHz
   (c) APPL is the number of active pixels per (horizontal) line.
   (d) If t_{p_thb} is calculated to be less than $t_{p\_hbp} + t_{p\_hfp}$ then the pixel clock rate is too low or the line rate is too high, and one or both must be adjusted.
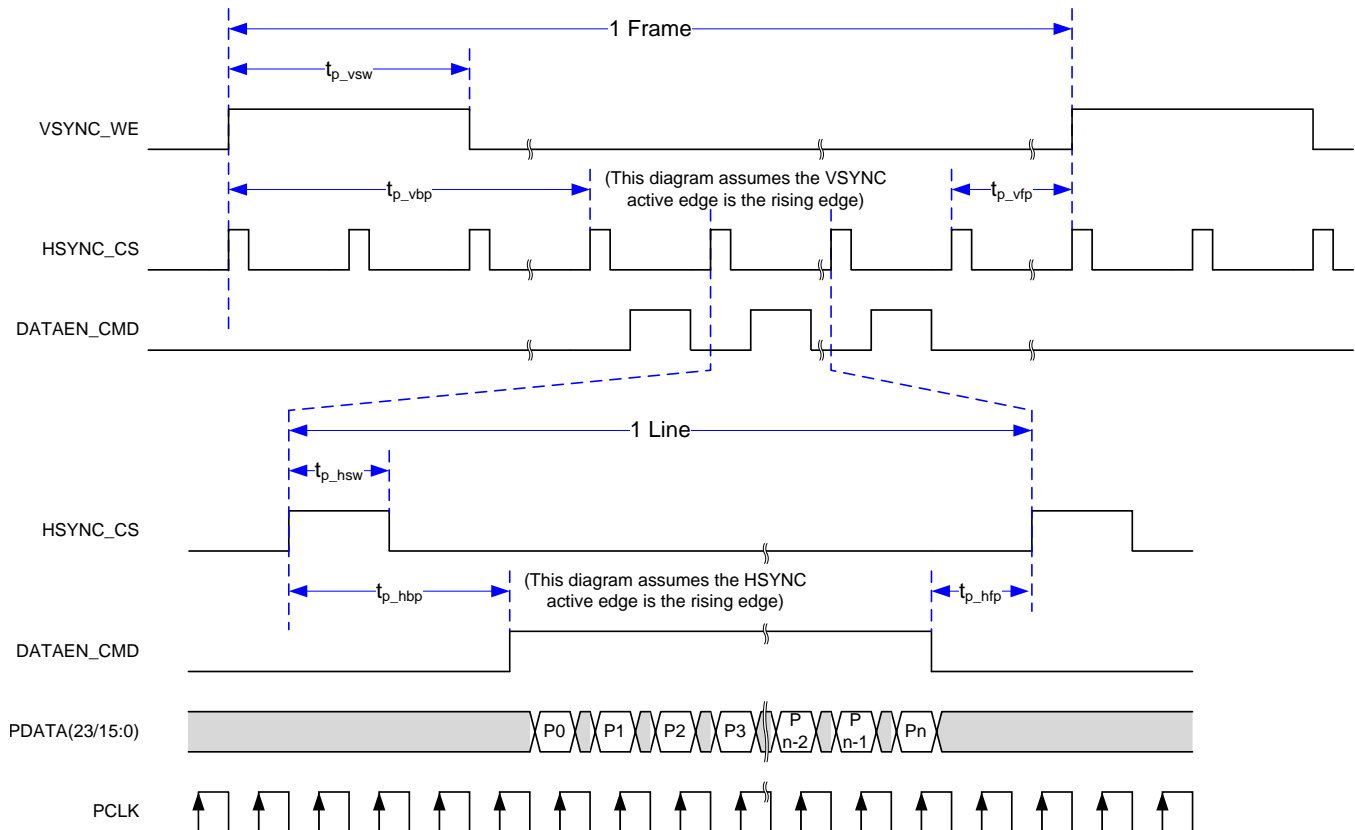
Figure 4. Parallel Interface Frame Timing

6.12 Parallel Interface General Timing Requirements[1]

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1.0	150.0	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	6.66	1000	ns
t_{p_clkjit}	Clock jitter, PCLK	Max f_{clock}	see [2]	see [2]	
t_{p_wh}	Pulse duration low, PCLK	50% reference points	2.43		ns
t_{p_wl}	Pulse duration high, PCLK	50% reference points	2.43		ns
t_{p_su}	Setup time – HSYNC_CS, DATEN_CMD, PDATA(23:0) valid before the active edge of PCLK	50% reference points	0.9		ns
t_{p_h}	Hold time – HSYNC_CS, DATEN_CMD, PDATA(23:0) valid after the active edge of PCLK	50% reference points	0.9		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	2.0	ns

(1) The active (capture) edge of PCLK for HSYNC_CS, DATEN_CMD and PDATA(23:0) is software programmable, but defaults to the rising edge.
(2) Clock jitter (in ns) should be calculated using this formula: Jitter = [1 / f_{clock} – 5.76 ns]. Setup and hold times must be met during clock jitter.
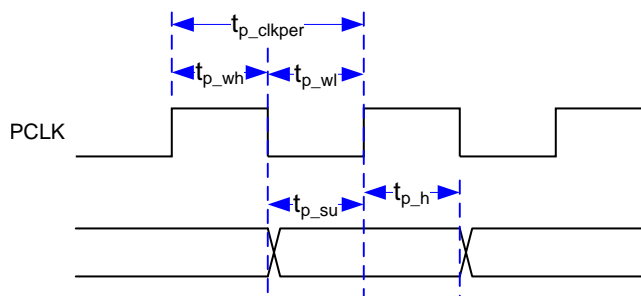

Figure 5. Parallel Interface General Timing

Product Folder Links: *DLPC3430 DLPC3435*

6.13 BT656 Interface General Timing Requirements[(1)]

The DLPC343x ASIC input interface supports the industry standard BT.656 parallel video interface. See the appropriate ITU-R BT.656 specification for detailed interface timing requirements.

	PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		1.0	33.5	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	29.85	1,000	ns
t_{p_clkjit}	Clock jitter, PCLK	Max f_{clock}	See [(2)]	See [(2)]	
t_{p_wh}	Pulse duration low, PCLK	50% reference points	10.0		ns
t_{p_wl}	Pulse duration high, PCLK	50% reference points	10.0		ns
t_{p_su}	Setup time – PDATA(7:0) before the active edge of PCLK	50% reference points	3.0		ns
t_{p_h}	Hold time – PDATA(7:0) after the active edge of PCLK	50% reference points	0.9		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	3.0	ns

(1)   The BT.656 interface accepts 8-bits per color, 4:2:2 YCb/Cr data encoded per the industry standard through PDATA(7:0) on the active edge of PCLK (that is programmable). See Figure 6.

(2)   Clock jitter should be calculated using this formula: Jitter = [1 / f_{clock} – 5.76 ns]. Setup and hold times must be met during clock jitter.

BT.656 Bus Mode – YCrCb 4:2:2 Source

PDATA(23:0) – BT.656 Mapping

A.   BT.656 data bits should be mapped to the DLPC343x PDATA bus as shown.

Figure 6. DLPC343x PDATA Bus – BT.656 Interface Mode Bit Mapping

6.14 Flash Interface Timing Requirements[1][2]

The DLPC343x ASIC flash memory interface consists of a SPI flash serial interface with a programmable clock rate. The DLPC343x can support 1- to 16-Mb flash memories.

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency, SPI_CLK	See [3]	1.42	36.0	MHz
t_{p_clkper}	Clock period, SPI_CLK	50% reference points	704	27.7	ns
t_{p_wh}	Pulse duration low, SPI_CLK	50% reference points	352		ns
t_{p_wl}	Pulse duration high, SPI_CLK	50% reference points	352		ns
t_t	Transition time – all signals	20% to 80% reference points	0.2	3.0	ns
t_{p_su}	Setup time – SPI_DIN valid before SPI_CLK falling edge	50% reference points	10.0		ns
t_{p_h}	Hold time – SPI_DIN valid after SPI_CLK falling edge	50% reference points	0.0		ns
t_{p_clqv}	SPI_CLK clock falling edge to output valid time – SPI_DOUT and SPI_CSZ	50% reference points		1.0	ns
t_{p_clqx}	SPI_CLK clock falling edge output hold time – SPI_DOUT and SPI_CSZ	50% reference points	–3.0	3.0	ns

(1) Standard SPI protocol is to transmit data on the falling edge of SPI_CLK and capture data on the rising edge. The DLPC343x does transmit data on the falling edge, but it also captures data on the falling edge rather than the rising edge. This provides support for SPI devices with long clock-to-Q timing. DLPC343x hold capture timing has been set to facilitate reliable operation with standard external SPI protocol devices.
(2) With the above output timing, DLPC343x provides the external SPI device 8.2-ns input set-up and 8.2-ns input hold, relative to the rising edge of SPI_CLK.
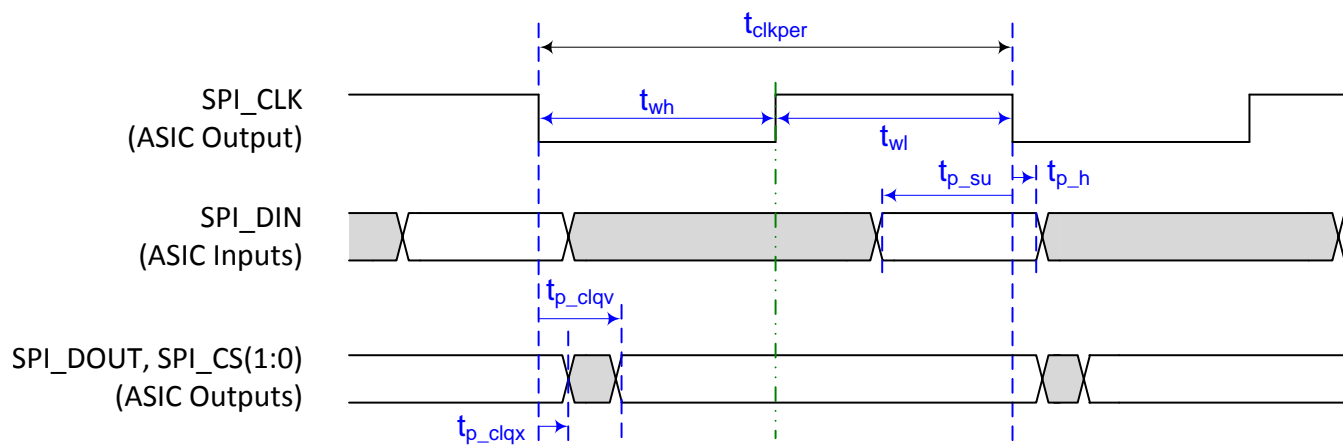(3) This range include the 200 ppm of the external oscillator (but no jitter).

Figure 7. Flash Interface Timing

7 Parameter Measurement Information

7.1 HOST_IRQ Usage Model

- While reset is applied HOST_IRQ will reset to tri-state (an external pullup pulls the line high).
- HOST_IRQ will remain tri-state (pulled high externally) until the microprocessor boot completes. While the signal is pulled high, this indicates that the ASIC is performing boot-up and auto-initialization.
- As soon as possible after boot-up, the microprocessor will drive HOST_IRQ to a logic high state to indicate that the ASIC is continuing to perform auto-initialization (no real state change occurs on the external signal)
- Upon completion of auto-initialization, software will set HOST_IRQ to a logic low state to indicate the completion of auto-initialization. (At the falling edge, the system is said to enter the INIT_DONE state.)
- After auto-initialization completes, HOST_IRQ is used to generate a logic high interrupt pulse to the host through software control. (This interrupt indicates that the ASIC has detected an error condition or otherwise requires service.)
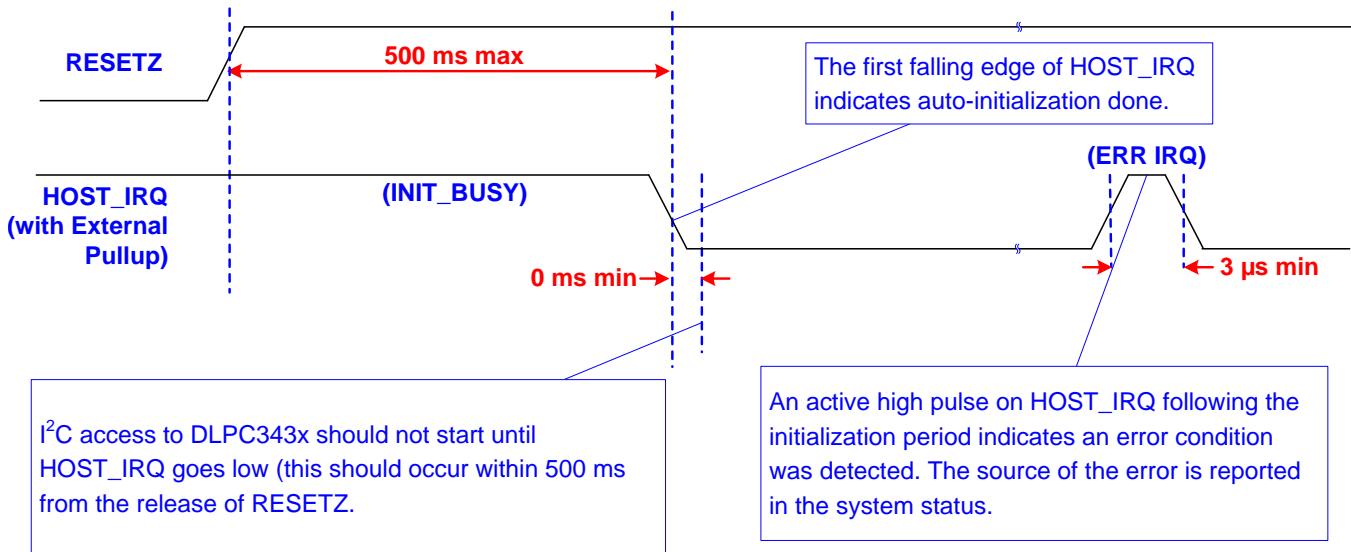
RESETZ

500 ms max

The first falling edge of HOST_IRQ indicates auto-initialization done.

HOST_IRQ
(with External Pullup)

(INIT_BUSY)

(ERR IRQ)

0 ms min

3 µs min

I^{2}C access to DLPC343x should not start until HOST_IRQ goes low (this should occur within 500 ms from the release of RESETZ.

An active high pulse on HOST_IRQ following the initialization period indicates an error condition was detected. The source of the error is reported in the system status.

Figure 8. Host IRQ Timing

Product Folder Links: *DLPC3430 DLPC3435*

7.2 Input Source

Table 3. Supported Input Source Ranges[(1)(2)(3)(4)]

Interface	Bits / Pixel [(5)]	Image Type	Source Resolution Range		Frame Rate Range
			Horizontal	Vertical	
Parallel	24 max	2D only	320 to 1280	200 to 800	4.75 to 94.00 Hz [(6)]
Parallel	24 max	3D only	320 to 1280	200 to 720	94.00 to 122.4 Hz
BT.656-NTSC [(7)]	[(8)]	2D only	720	240	60 ±3 Hz
BT.656-PAL [(7)]	[(8)]	2D only	720	288	50 ±3 Hz

(1) The user must stay within specifications for all source interface parameters such as max clock rate and max line rate.
(2) The max DMD size for all rows in the table is 854 × 480.
(3) To achieve the ranges stated, the composer-created firmware used must be defined to support the source parameters used.
(4) These interfaces are supported with the DMD sequencer sync mode command (3Bh) set to auto.
(5) Bits / Pixel does not necessarily equal the number of data pins used on the DLPC343x. Fewer pins are used if multiple clocks are used per pixel transfer.
(6) Frame rates below 10.00 Hz have not been tested by TI.
(7) All parameters in this row follow the BT.656 standard.
(8) BT.656 uses 16-bit 4:2:2 YCr/Cb.

7.2.1 Parallel Interface Supports Six Data Transfer Formats

- 24-bit RGB888 or 24-bit YCrCb888 on a 24 data wire interface
- 18-bit RGB666 or 18-bit YCrCb666 on a 18 data wire interface
- 16-bit RGB565 or 16-bit YCrCb565 on a 16 data wire interface
- 16-bit YCrCb 4:2:2 (standard sampling assumed to be Y0Cb0, Y1Cr0, Y2Cb2, Y3Cr2, Y4Cb4, Y5Cr4, …)
- 8-bit RGB888 or 8-bit YCrCb888 serial (1 color per clock input; 3 clocks per displayed pixel)
  - On an 8 wire interface
- 8-bit YCrCb 4:2:2 serial (1 color per clock input; 2 clocks per displayed pixel)
  - On an 8 wire interface

PDATA Bus – Parallel Interface Bit Mapping Modes shows the required PDATA(23:0) bus mapping for these six data transfer formats.
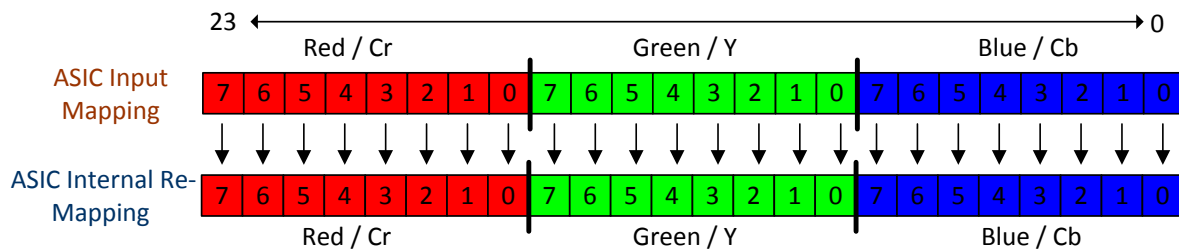
7.2.1.1 PDATA Bus – Parallel Interface Bit Mapping Modes

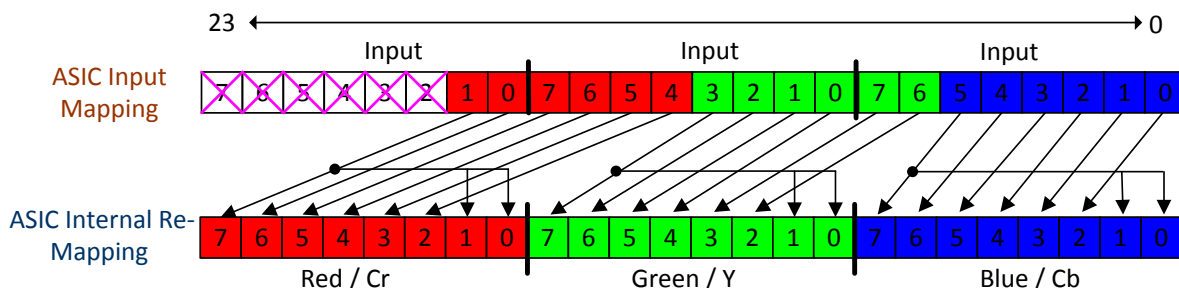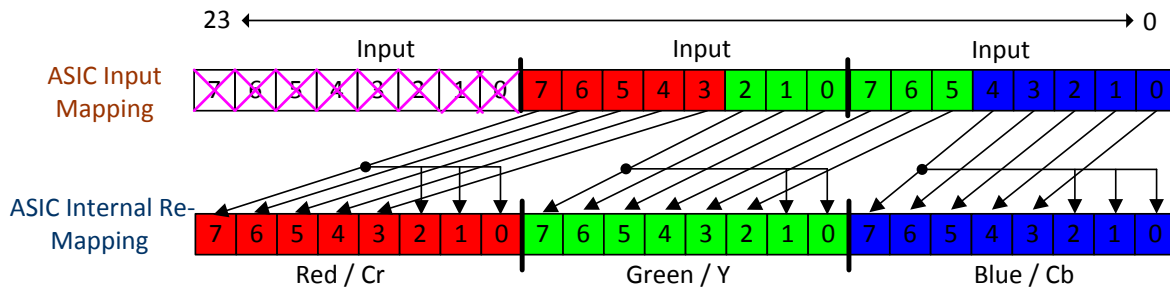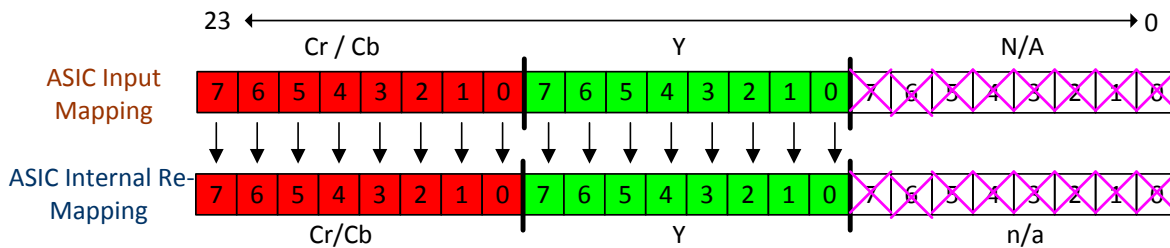Figure 9. RGB-888 / YCrCb-888 I/O Mapping

Figure 10. RGB-666 / YCrCb-666 I/O Mapping

Product Folder Links: DLPC3430 DLPC3435

**Figure 11. RGB-565 / YCrCb-565 I/O Mapping**

Figure 12. 16-Bit YCrCb-880 I/O Mapping
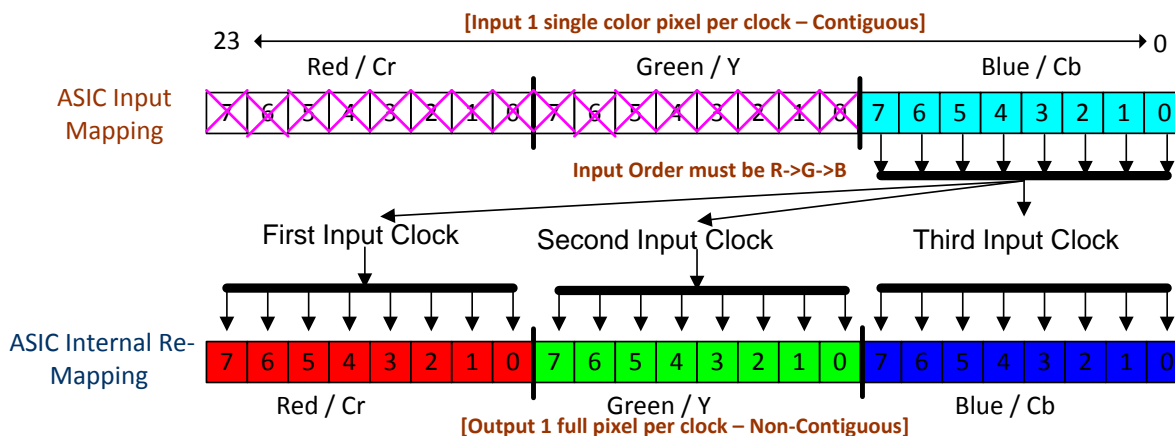
Figure 13. 8-Bit RGB-888 or YCrCb-888 I/O Mapping
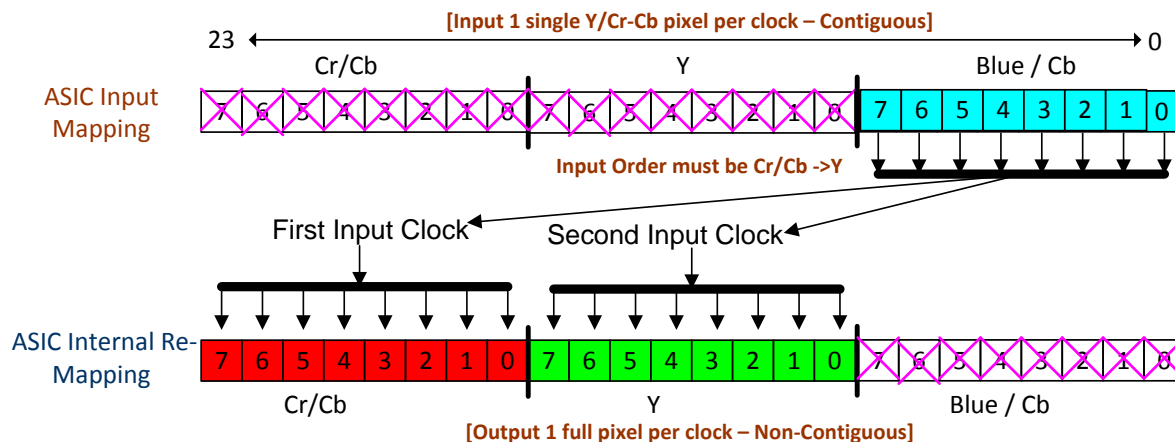
Figure 14. 8-Bit Serial YCrCb-422 I/O Mapping

Product Folder Links: *DLPC3430   DLPC3435*

8 Detailed Description

8.1 Overview

The DLPC343x is the display controller for the DLP2010 (.2 WVGA) DMD. DLPC343x is part of the chipset comprising DLPC343x controller, DLP2010 (.2 WVGA) DMD, and DLPA2000 PMIC/LED driver. All three components of the chipset must be used in conjunction with each other for reliable operation of the DLP2010 (.2 WVGA) DMD. The DLPC343x display controller provides interfaces and data/image processing functions that are optimized for small form factor and power-constrained display applications. Applications include projection within cell phones, camera, camcorders and tablets, pico projectors, wearable displays, and digital signage. Standalone projectors must include a separate front-end chip to interface to the outside world (for example, video decoder, HDMI receiver, triple ADC, or USB I/F chip).

8.2 Functional Block Diagram
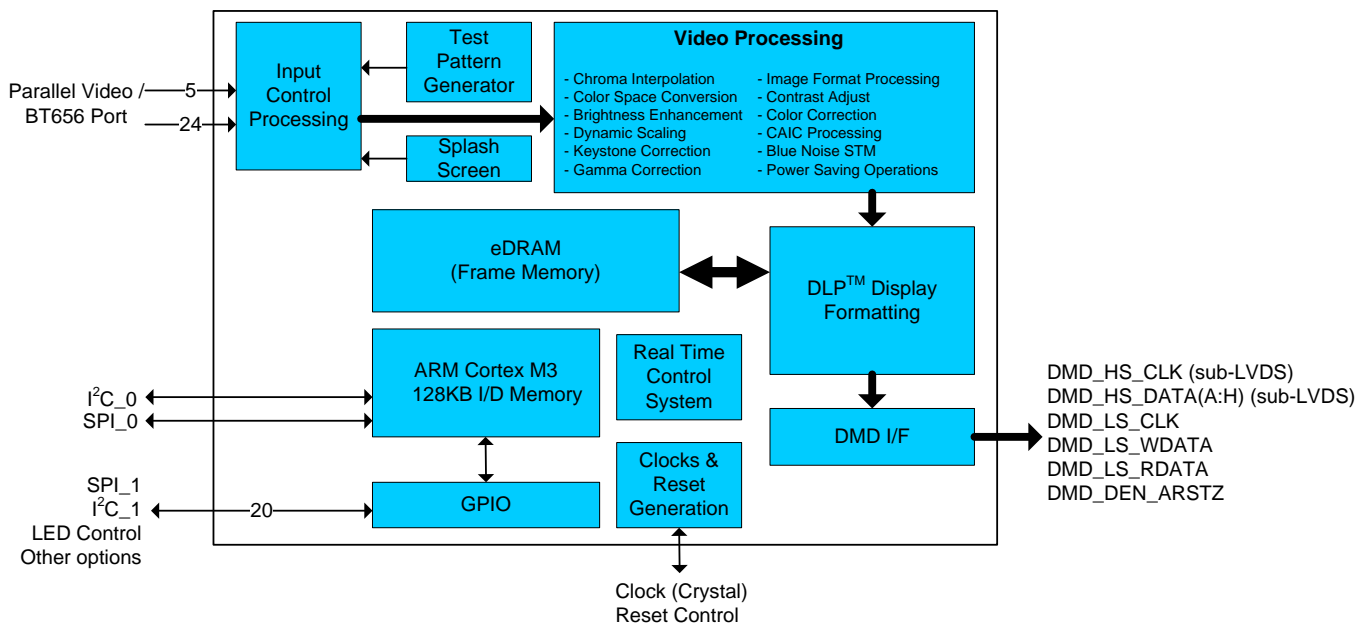
8.3 Feature Description

8.3.1 Interface Timing Requirements

This section defines the timing requirements for the external interfaces for the DLPC343x ASIC.

8.3.1.1 Parallel Interface

The parallel interface complies with standard graphics interface protocol, which includes a vertical sync signal (VSYNC_WE), horizontal sync signal (HSYNC_CS), optional data valid signal (DATAEN_CMD), a 24-bit data bus (PDATA), and a pixel clock (PCLK). The polarity of both syncs and the active edge of the clock are programmable. Figure 4 shows the relationship of these signals. The data valid signal (DATAEN_CMD) is optional in that the DLPC343x provides auto-framing parameters that can be programmed to define the data valid window based on pixel and line counting relative to the horizontal and vertical syncs.

In addition to these standard signals, an optional side-band signal (PDM_CVS_TE) is available, which allows periodic frame updates to be stopped without losing the displayed image. When PDM_CVS_TE is active, it acts as a data mask and does not allow the source image to be propagated to the display. A programmable PDM polarity parameter determines if it is active high or active low. This parameter defaults to make PDM_CVS_TE active high; if this function is not desired, then it should be tied to a logic low on the PCB. PDM_CVS_TE is restricted to change only during vertical blanking.

Feature Description (continued)

> **NOTE**
> VSYNC_WE must remain active at all times (in lock-to-VSYNC mode) or the display sequencer will stop and cause the LEDs to be turned off.

8.3.2 Serial Flash Interface

DLPC343x uses an external SPI serial flash memory device for configuration support. The minimum required size is dependent on the desired minimum number of sequences, CMT tables, and splash options while the maximum supported is 16 Mb.

For access to flash, the DLPC343x uses a single SPI interface operating at a programmable frequency complying to industry standard SPI flash protocol. The programmable SPI frequency is defined to be equal to 180 MHz/N, where N is a programmable value between 5 to 127 providing a range from 36.0 to 1.41732 MHz. Note that this results in a relatively large frequency step size in the upper range (for example, 36 MHz, 30 MHz, 25.7 MHz, 22.5 MHz, and so forth) and thus this must be taken into account when choosing a flash device.

The DLPC343x supports two independent SPI chip selects; however, the flash must be connected to SPI chip select zero (SPI0_CSZ0) because the boot routine is only executed from the device connected to chip select zero (SPI0_CSZ0). The boot routine uploads program code from flash to program memory, then transfers control to an auto-initialization routine within program memory. The DLPC343x asserts the HOST_IRQ output signal high while auto-initialization is in progress, then drives it low to signal its completion to the host processor. Only after auto-initialization is complete will the DLPC343x be ready to receive commands through I^{2}C.

The DLPC343x should support any flash device that is compatible with the modes of operation, features, and performance as defined in Table 4 and Table 5.

Table 4. SPI Flash Required Features or Modes of Operation

Feature	DLPC343x Requirement
SPI interface width	Single
SPI protocol	SPI mode 0
Fast READ addressing	Auto-incrementing
Programming mode	Page mode
Page size	256 B
Sector size	4 KB sector
Block size	any
Block protection bits	0 = Disabled
Status register bit(0)	Write in progress (WIP) {also called flash busy}
Status register bit(1)	Write enable latch (WEN)
Status register bits(6:2)	A value of 0 disables programming protection
Status register bit(7)	Status register write protect (SRWP)
Status register bits(15:8) (that is expansion status byte)	The DLPC343x only supports single-byte status register R/W command execution, and thus may not be compatible with flash devices that contain an expansion status byte. However, as long as expansion status byte is considered optional in the byte 3 position and any write protection control in this expansion status byte defaults to unprotected, then the device should be compatible with DLPC343x.

To support flash devices with program protection defaults of either enabled or disabled, the DLPC343x always assumes the device default is enabled and goes through the process of disabling protection as part of the boot-up process. This process consists of:
- A write enable (WREN) instruction executed to request write enable, followed by
- A read status register (RDSR) instruction is then executed (repeatedly as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, a write status register (WRSR) instruction is executed that writes 0 to all 8-bits (this disables all programming protection)

Prior to each program or erase instruction, the DLPC343x issues:
- A write enable (WREN) instruction to request write enable, followed by

Product Folder Links: *DLPC3430 DLPC3435*

- A read status register (RDSR) instruction (repeated as needed) to poll the write enable latch (WEL) bit
- After the write enable latch (WEL) bit is set, the program or erase instruction is executed
- Note the flash automatically clears the write enable status after each program and erase instruction

The specific instruction OpCode and timing compatibility requirements are listed in Table 7 and Table 6. Note however that DLPC343x does not read the flash's electronic signature ID and thus cannot automatically adapt protocol and clock rate based on the ID.

Table 5. SPI Flash Instruction OpCode and Access Profile Compatibility Requirements

SPI Flash Command	First Byte (OPCODE)	Second Byte	Third Byte	Fourth Byte	Fifth Byte	Sixth Byte
Fast READ (1 Output)	0x0B	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0)[1]
Read status	0x05	n/a	n/a	STATUS(0)		
Write status	0x01	STATUS(0)	[2]			
Write enable	0x06					
Page program	0x02	ADDRS(0)	ADDRS(1)	ADDRS(2)	DATA(0)[3]	
Sector erase (4KB)	0x20	ADDRS(0)	ADDRS(1)	ADDRS(2)		
Chip erase	0xC7					

(1) Only the first data byte is show, data continues
(2) DLPC343x does not support access to a second/ expansion Write Status byte
(3) Only the first data byte is show, data continues

The specific and timing compatibility requirements for a DLPC343x compatible flash are listed in Table 6 and Table 7.

Table 6. SPI Flash Key Timing Parameter Compatibility Requirements[1][2]

SPI Flash Timing Parameter	Symbol	Alternate Symbol	Min	Max	Unit
Access frequency (all commands)	FR	f_C	≤1.42		MHz
Chip select high time (also called chip select deselect time)	t_{SHSL}	t_{CSH}	≤200		ns
Output hold time	t_{CLQX}	t_{HO}	≥0		ns
Clock low to output valid time	t_{CLQV}	t_V		≤ 11	ns
Data in set-up time	t_{DVCH}	t_{DSU}	≤5		ns
Data in hold time	t_{CHDX}	t_{DH}	≤5		ns

(1) The timing values are related to the specification of the flash device itself, not the DLPC343x.
(2) The DLPC343x does not drive the HOLD or WP (active low write protect) pins on the flash device, and thus these pins should be tied to a logic high on the PCB through an external pullup.

The DLPC343x supports 1.8-, 2.5-, or 3.3-V serial flash devices. To do so, VCC_FLSH must be supplied with the corresponding voltage. Table 7 contains a list of 1.8-, 2.5-, and 3.3-V compatible SPI serial flash devices supported by DLPC343x.

Table 7. DLPC343x Compatible SPI Flash Device Options [(1)] [(2)]

DVT[(3)]	Density (M-bits)	Vendor	Part Number	Package Size
1.8-V Compatible Devices				
Yes	4 Mb	Winbond	W25Q40BWUXIG	2 × 3 mm USON
Yes	4 Mb	Macronix	MX25U4033EBAI-12G	1.43 × 1.94 mm WLCSP
Yes	4 Mb	Macronix	MX25U4033EBAI-12G	1.68 × 1.99 mm WLCSP
2.5- or 3.3-V Compatible Devices				
Yes	16 Mb	Winbond	W25Q16CLZPIG	5 × 6 mm WSON

(1) The flash supply voltage must match VCC_FLSH on the DLPC343x. Special attention needs to be paid when ordering devices to be sure the desired supply voltage is attained as multiple voltage options are often available under the same base part number.
(2) Beware when considering Numonyx (Micron) serial flash devices as they typically do not have the 4KB sector size needed to be DLPC343x compatible.
(3) All of these flash devices appear compatible with the DLPC343x, but only those marked with yes in the DVT column have been validated on the EVM3430 reference design. Those marked with no can be used at the ODM's own risk.

8.3.3 Serial Flash Programming

Note that the flash can be programmed through the DLPC343x over I^{2}C or by driving the SPI pins of the flash directly while the DLPC343x I/O are tri-stated. SPI0_CLK, SPI0_DOUT, and SPI0_CSZ0 I/O can be tri-stated by holding RESETZ in a logic low state while power is applied to the DLPC343x. Note that SPI0_CSZ1 is not tri-stated by this same action.

8.3.4 SPI Signal Routing

The DLPC343x is designed to support two SPI slave devices on the SPI0 interface, specifically, a serial flash and the DLPA2000. This requires routing associated SPI signals to two locations while attempting to operate up to 36 MHz. Take special care to ensure that reflections do not compromise signal integrity. To this end, the following recommendations are provided:

- The SPI0_CLK PCB signal trace from the DLPC343x source to each slave device should be split into separate routes as close to the DLPC343x as possible. In addition, the SPI0_CLK trace length to each device should be equal in total length.
- The SPI0_DOUT PCB signal trace from the DLPC343x source to each slave device should be split into separate routes as close to the DLPC343x as possible. In addition, the SPI0_DOUT trace length to each device should be equal in total length(use the same strategy as SPI0_CLK).
- The SPI0_DIN PCB signal trace from each slave device to the point where they intersect on their way back to the DLPC343x should be made equal in length and as short as possible. They should then share a common trace back to the DLPC343x.
- SPI0_CSZ0 and SPI0_CSZ1 need no special treatment because they are dedicated signals which drive only one device.

8.3.5 I^{2}C Interface Performance

Both DLPC343x I^{2}C interface ports support 100-kHz baud rate. By definition, I^{2}C transactions operate at the speed of the slowest device on the bus, thus there is no requirement to match the speed grade of all devices in the system.

8.3.6 Content-Adaptive Illumination Control

Content-adaptive illumination control (CAIC) is an image processing algorithm that takes advantage of the fact that in common real-world image content most pixels in the images are well below full scale for the for the R, G, and B digital channels being input to the DLPC343x. As a result of this the average picture level (APL) for the overall image is also well below full scale, and the system's dynamic range for the collective set of pixel values is not fully utilized. CAIC takes advantage of this headroom between the source image APL and the top of the available dynamic range of the display system.

CAIC evaluates images frame by frame and derives three unique digital gains, one for each of the R, G, and B color channels. During CAIC image processing, each gain is applied to all pixels in the associated color channel. CAIC derives each color channel's gain that is applied to all pixels in that channel so that the pixels as a group collectively shift upward and as close to full scale as possible. To prevent any image quality degradation, the gains are set at the point where just a few pixels in each color channel are clipped. Figure 15 and Figure 16 show an example of the application of CAIC for one color channel.
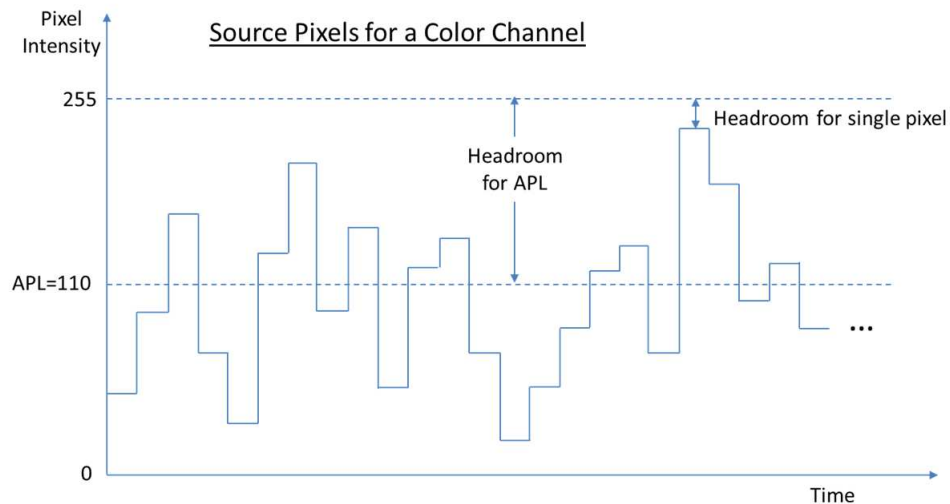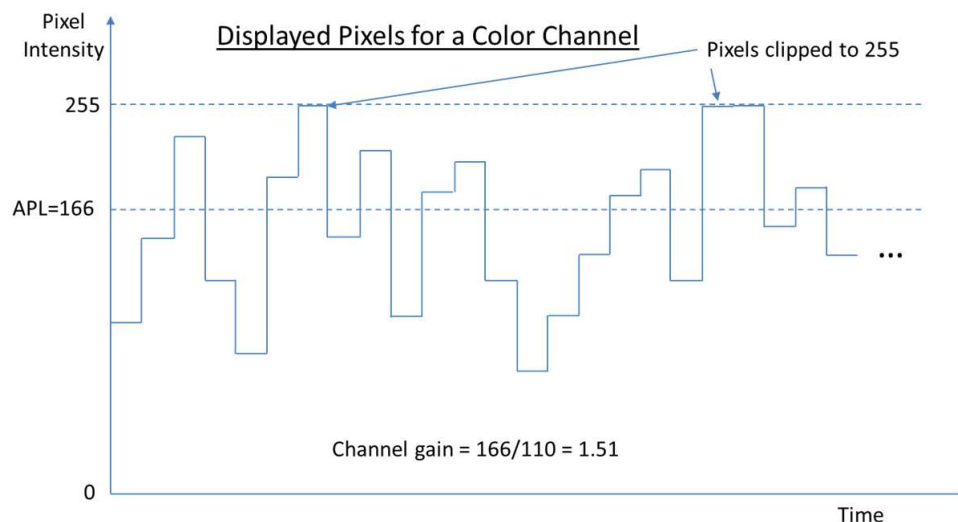

Figure 15. Input Pixels Example

Figure 16. Displayed Pixels After CAIC Processing

Figure 16 shows the gain that is applied to a color processing channel inside the DLPC343x. CAIC will also adjust the power for the R, G, and B LED. For each color channel of an individual frame, CAIC will intelligently determine the optimal combination of digital gain and LED power. The decision regarding how much digital gain to apply to a color channel and how much to adjust the LED power for that color is heavily influenced by the software command settings sent to the DLPC343x for configuring CAIC.

As CAIC applies a digital gain to each color channel independently, and adjusts each LED's power independently, CAIC also makes sure that the resulting color balance in the final image matches the target color balance for the projector system. Thus, the effective displayed white point of images is held constant by CAIC from frame to frame.

Since the R, G, and B channels can be gained up by CAIC inside the DLPC343x, the LED power can be turned down for any color channel until the brightness of the color on the screen is unchanged. Thus, CAIC can achieve an overall LED power reduction while maintaining the same overall image brightness as if CAIC was not used. Figure 17 shows an example of LED power reduction by CAIC for an image where the R and B LEDs can be turned down in power.

CAIC can alternatively be used to increase the overall brightness of an image while holding the total power for all LEDs constant. In summary, when CAIC is enabled CAIC can operate in one of two distinct modes:

- Power Reduction Mode – holds overall image brightness constant while reducing LED power
- Enhanced Brightness Mode – holds overall LED power constant while enhancing image brightness
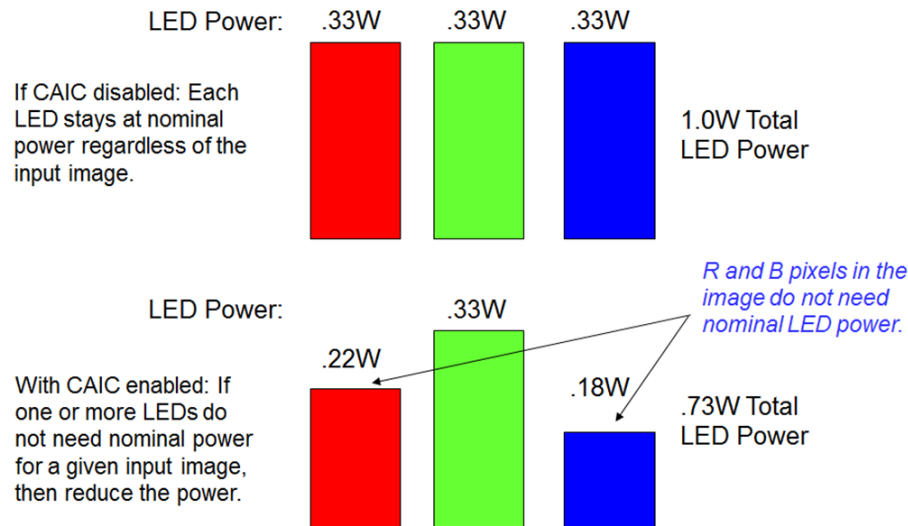

Figure 17. CAIC Power Reduction Mode (for Constant Brightness)

8.3.7 Local Area Brightness Boost

Local area brightness boost (LABB), is an image processing algorithm that adaptively gains up regions of an image that are dim relative to the average picture level. Some regions of the image will have significant gain applied, and some regions will have little or no gain applied. LABB evaluates images frame by frame and derives the local area gains to be used uniquely for each image. Since many images have a net overall boost in gain even if some parts of the image get no gain, the overall perceived brightness of the image is boosted.

Figure 18 shows a split screen example of the impact of the LABB algorithm for an image that includes dark areas.
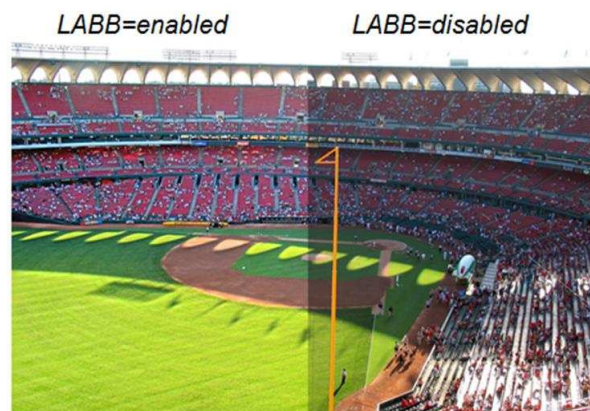

Figure 18. Boosting Brightness in Local Areas of an Image

Product Folder Links: *DLPC3430 DLPC3435*

LABB works best when the decision about the strength of gains used is determined by ambient light conditions. For this reason, there is an option to add an ambient light sensor which can be read by the DLPC343x during each frame. Based on the sensor readings, LABB will apply higher gains for bright rooms to help overcome any washing out of images. LABB will apply lower gains in dark rooms to prevent over-punching of images.

8.3.8 94- to 120-Hz 3-D Display Operation

The DLPC343x supports 94- to 120-Hz 3-D display operation, but is limited to:

- Only parallel interfaces (all pixel formats are supported)
- Only non-interlaced image inputs
- 122.4 Hz is maximum supported frame rate
- Un-packed, frame sequential, 3-D format (that is each 100- or 120-Hz source frame contains a single, full resolution, eye frame separated by VSYNCs, where an eye frame contains image data for a single left or right eye; not both)

Each DMD frame is displayed at the source frame rate in the order it is received. It is assumed that a front-end device ahead of the DLPC343x will convert all 3-D sources to the 3-D format defined previously and will provide any needed left or right eye selection control directly to the DLPC343x 3DR input pin.

8.3.9 DMD (Sub-LVDS) Interface

The DLPC343x ASIC DMD interface consists of a HS 1.8-V sub-LVDS output only interface with a maximum clock speed of 600-MHz DDR and a LS SDR (1.8-V LVCMOS) interface with a fixed clock speed of 120 MHz. The DLPC343x sub-LVDS interface supports a number of DMD display sizes, and as a function of resolution, not all output data lanes are needed as DMD display resolutions decrease in size. With internal software selection, the DLPC343x also supports a limited number of DMD interface swap configurations that can help board layout by remapping specific combinations of DMD interface lines to other DMD interface lines as needed. Table 8 shows the four options available for the DLP2010 (.2 WVGA) DMD specifically. Any unused DMD signal pairs should be left unconnected on the final board design.

Table 8. DLP2010 (.2 WVGA) DMD – ASIC to 4-Lane DMD Pin Mapping Options

| DLPC343x ASIC 4 Lane DMD Routing Options				DMD Pins
Option 1 Swap Control = x0	Option 2 Swap Control = x2	Option 3 Swap Control = x1	Option 4 Swap Control = x3	
HS_WDATA_D_P HS_WDATA_D_N	HS_WDATA_E_P HS_WDATA_E_N	HS_WDATA_H_P HS_WDATA_H_N	HS_WDATA_A_P HS_WDATA_A_N	Input DATA_p_0 Input DATA_n_0
HS_WDATA_C_P HS_WDATA_C_N	HS_WDATA_F_P HS_WDATA_F_N	HS_WDATA_G_P HS_WDATA_G_N	HS_WDATA_B_P HS_WDATA_B_N	Input DATA_p_1 Input DATA_n_1
HS_WDATA_F_P HS_WDATA_F_N	HS_WDATA_C_P HS_WDATA_C_N	HS_WDATA_B_P HS_WDATA_B_N	HS_WDATA_G_P HS_WDATA_G_N	Input DATA_p_2 Input DATA_n_2
HS_WDATA_E_P HS_WDATA_E_N	HS_WDATA_D_P HS_WDATA_D_N	HS_WDATA_A_P HS_WDATA_A_N	HS_WDATA_H_P HS_WDATA_H_N	Input DATA_p_3 Input DATA_n_3
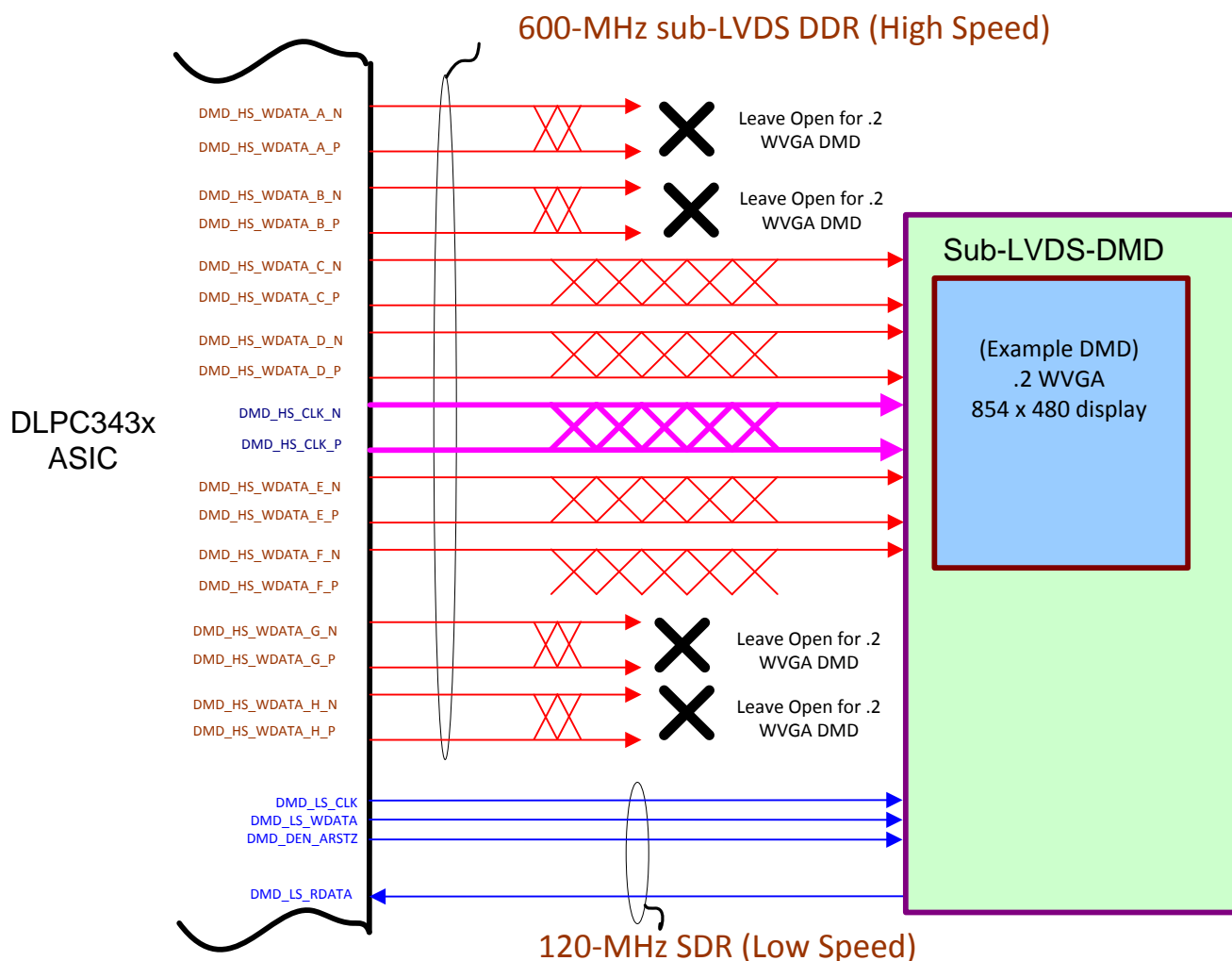
Figure 19. DLP2010 (.2 WVGA) DMD Interface Example (Mapping Option 1 Shown)

8.3.10   DLPC343x System Design Consideration – Application Notes

System power regulation: It is acceptable for VDD_PLLD and VDD_PLLM to be derived from the same regulator as the core VDD, but to minimize the AC noise component they should be filtered as recommended in the *PCB Layout Guidelines for Internal ASIC PLL Power*.

8.3.11   Calibration and Debug Support

The DLPC343x contains a test point output port, TSTPT_(7:0), which provides selected system calibration support as well as ASIC debug support. These test points are inputs while reset is applied and switch to outputs when reset is released. The state of these signals is sampled upon the release of system reset and the captured value configures the test mode until the next time reset is applied. Each test point includes an internal pulldown resistor, thus external pullups must be used to modify the default test configuration. The default configuration (x000) corresponds to the TSTPT_(7:0) outputs remaining tri-stated to reduce switching activity during normal operation. For maximum flexibility, an option to jumper to an external pullup is recommended for TSTPT_(2:0). Pullups on TSTPT_(6:3) are used to configure the ASIC for a specific mode or option. TI does not recommend adding pullups to TSTPT_(7:3) because this has adverse affects for normal operation. This external pullup is only sampled upon a 0-to-1 transition on the RESETZ input, thus changing their configuration after reset is released will not have any effect until the next time reset is asserted and released. Table 9 defines the test mode selection for one programmable scenario defined by TSTPT(2:0).

Table 9. Test Mode Selection Scenario Defined by TSTPT(2:0)[1]

TSTPT(2:0) Capture Value	No Switching Activity	Clock Debug Output
	x000	x010
TSTPT(0)	HI-Z	60 MHz
TSTPT(1)	HI-Z	30 MHz
TSTPT(2)	HI-Z	0.7 to 22.5MHz
TSTPT(3)	HI-Z	HIGH
TSTPT(4)	HI-Z	LOW
TSTPT(5)	HI-Z	HIGH
TSTPT(6)	HI-Z	HIGH
TSTPT(7)	HI-Z	7.5 MHz

(1) These are only the default output selections. Software can reprogram the selection at any time.

8.3.12 DMD Interface Considerations

The sub-LVDS HS interface waveform quality and timing on the DLPC343x ASIC is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

Setup Margin = (DLPC343x output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation)   (1)

Hold-time Margin = (DLPC343x output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

where PCB SI degradation is signal integrity degradation due to PCB affects which includes such things as Simultaneously Switching Output (SSO) noise, cross-talk and Inter-symbol Interference (ISI) noise.   (2)

DLPC343x I/O timing parameters as well as DMD I/O timing parameters can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be budgeted and met through controlled PCB routing. However, PCB SI degradation is a more complicated adjustment.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that will satisfy both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations may also work, but should be confirmed with PCB signal integrity analysis or lab measurements.
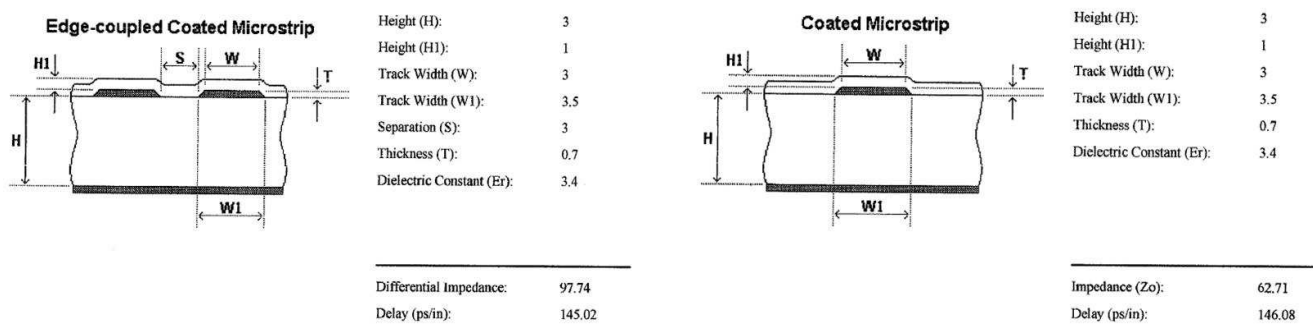
DMD_HS Differential Signals

DMD_LS Signals

Figure 20. DMD Interface Board Stack-Up Details

8.4 Device Functional Modes

DLPC343x has two functional modes (ON/OFF) controlled by a single pin PROJ_ON:

- When pin PROJ_ON is set high, the projector automatically powers up and an image is projected from the DMD.
- When pin PROJ_ON is set low, the projector automatically powers down and only microwatts of power are consumed.

Product Folder Links: *DLPC3430 DLPC3435*

9 Application and Implementation

9.1 Application Information

The DLPC343x controller requires to be coupled with DLP2010 DMD to provide a reliable display solution for many data and video display applications. The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC343x. Applications of interest include projection embedded in display devices like smart phones, tablets, cameras, and camcorders. Other applications include wearable (near-eye) displays, battery powered mobile accessory, interactive display, low latency gaming display, and digital signage.

9.2 Typical Application

A common application when using DLPC343x controller with DLP2010 DMD and DLPA2000 PMIC/LED driver is for creating a Pico projector embedded in a handheld product. For example, a Pico projector may be embedded in a smart phone, a tablet, a camera, or camcorder. The DLPC343x in the Pico projector embedded module typically receives images from a host processor within the product.
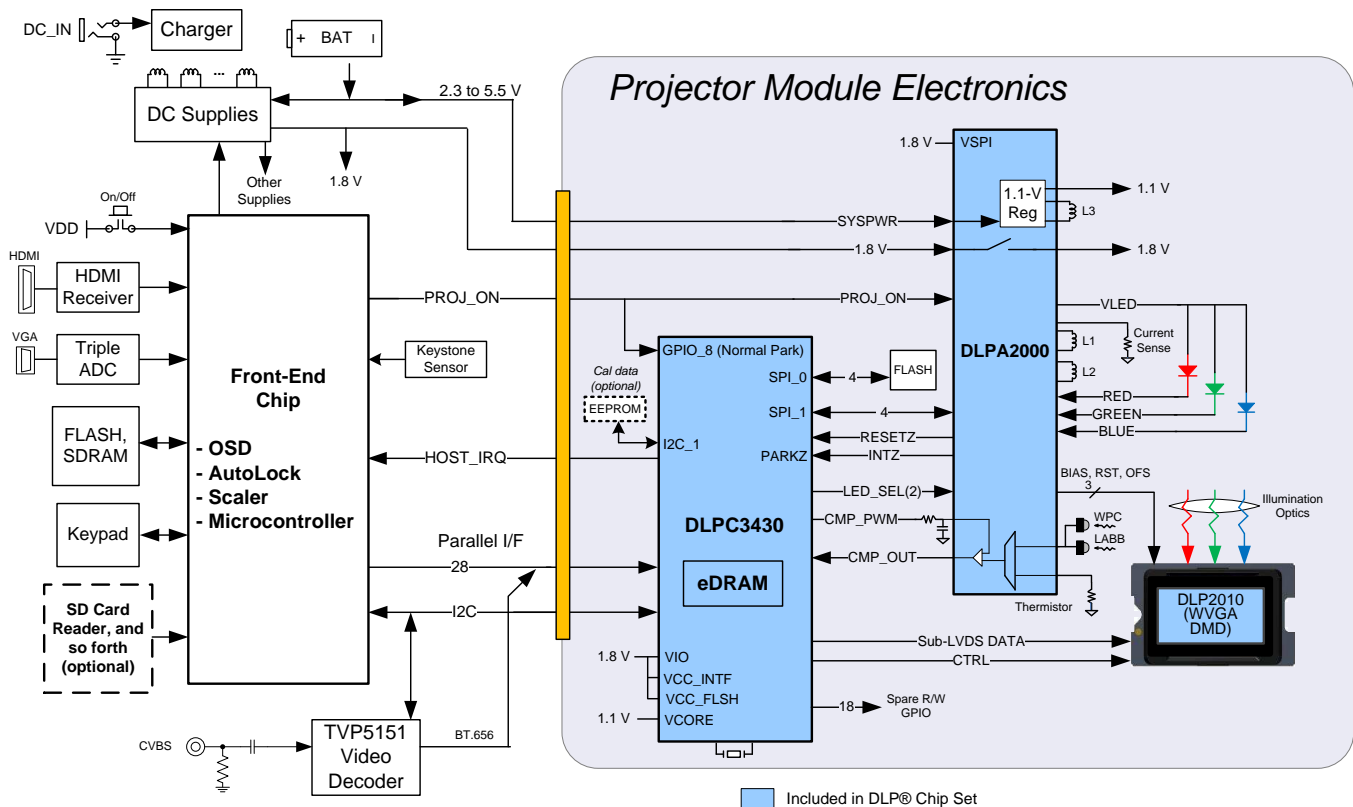
9.2.1 Design Requirements

A Pico projector is created by using a DLP chipset comprised of DLP2010 (.2 WVGA) DMD, DLPC343x controller and DLPA2000 PMIC/LED driver. The DLPC343x does the digital image processing, the DLPA2000 provides the needed analog functions for the projector, and DMD is the display device for producing the projected image.

In addition to the three DLP chips in the chipset, other chips may be needed. At a minimum a flash part is needed to store the software and firmware to control the DLPC343x.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector.

Typical Application (continued)

For connecting the DLPC343x to the host processing for receiving images, parallel interface is used. I^{2}C should be connected to the host processor for sending commands to the DLPC3430.

The only power supplies needed external to the projector are the battery (SYSPWR) and a regulated 1.8-V supply.

The entire pico-projector can be turned on and off by using a single signal called PROJ_ON. When PROJ_ON is high, the projector turns on and begins displaying images. When PROJ_ON is set low, the projector turns off and draws just microamps of current on SYSPWR. When PROJ_ON is set low, the 1.8V supply can continue to be left at 1.8 V and used by other non-projector sections of the product. If PROJ_ON is low, the DLPA2000 will not draw current on the 1.8-V supply.

9.2.2 Detailed Design Procedure

For connecting together the DLP2010 (.2 WVGA) DMD, DLPC343x controller and DLPA2000 PMIC/LED Driver see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Follow the layout guidelines to achieve a reliable projector.

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

9.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is shown in Figure 21. For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue LEDs.
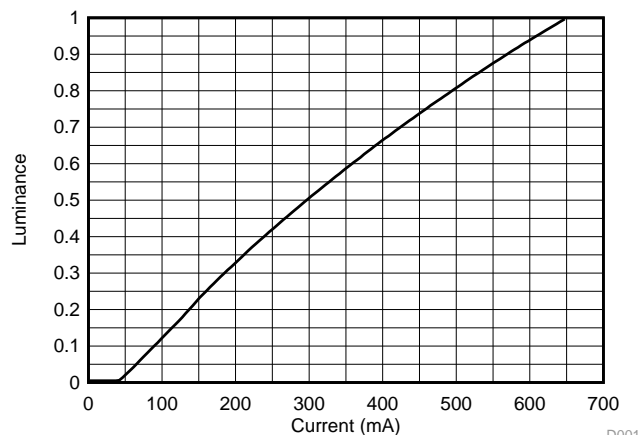

Figure 21. Luminance vs Current

Product Folder Links: *DLPC3430 DLPC3435*

10 Power Supply Recommendations

10.1 System Power-Up and Power-Down Sequence

Although the DLPC343x requires an array of power supply voltages, (for example, VDD, VDDLP12, VDD_PLLM/D, VCC18, VCC_FLSH, VCC_INTF), if VDDLP12 is tied to the 1.1-V VDD supply (which is assumed to be the typical configuration), then there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC343x. (This is true for both power-up and power-down scenarios). Similarly, there is no minimum time between powering-up or powering-down the different supplies if VDDLP12 is tied to the 1.1-V VDD supply.

If however VDDLP12 is not tied to the VDD supply, then VDDLP12 must be powered-on after the VDD supply is powered-on, and powered-off before the VDD supply is powered-off. In addition, if VDDLP12 is not tied to VDD, then VDDLP12 and VDD supplies should be powered on or powered off within 100 ms of each other.

Although there is no risk of damaging the DLPC343x if the above power sequencing rules are followed, the following additional power sequencing recommendations must be considered to ensure proper system operation.

- To ensure that DLPC343x output signal states behave as expected, all DLPC343x I/O supplies should remain applied while VDD core power is applied. If VDD core power is removed while the I/O supply (VCC_INTF) is applied, then the output signal state associated with the inactive I/O supply will go to a high impedance state.
- Additional power sequencing rules may exist for devices that share the supplies with the DLPC343x, and thus these devices may force additional system power sequencing requirements.

Note that when VDD core power is applied, but I/O power is not applied, additional leakage current may be drawn. This added leakage does not affect normal DLPC343x operation or reliability.

Figure 22 and Figure 23 show the DLPC343x power-up and power-down sequence for both the normal PARK and fast PARK operations of the DLPC343x ASIC.

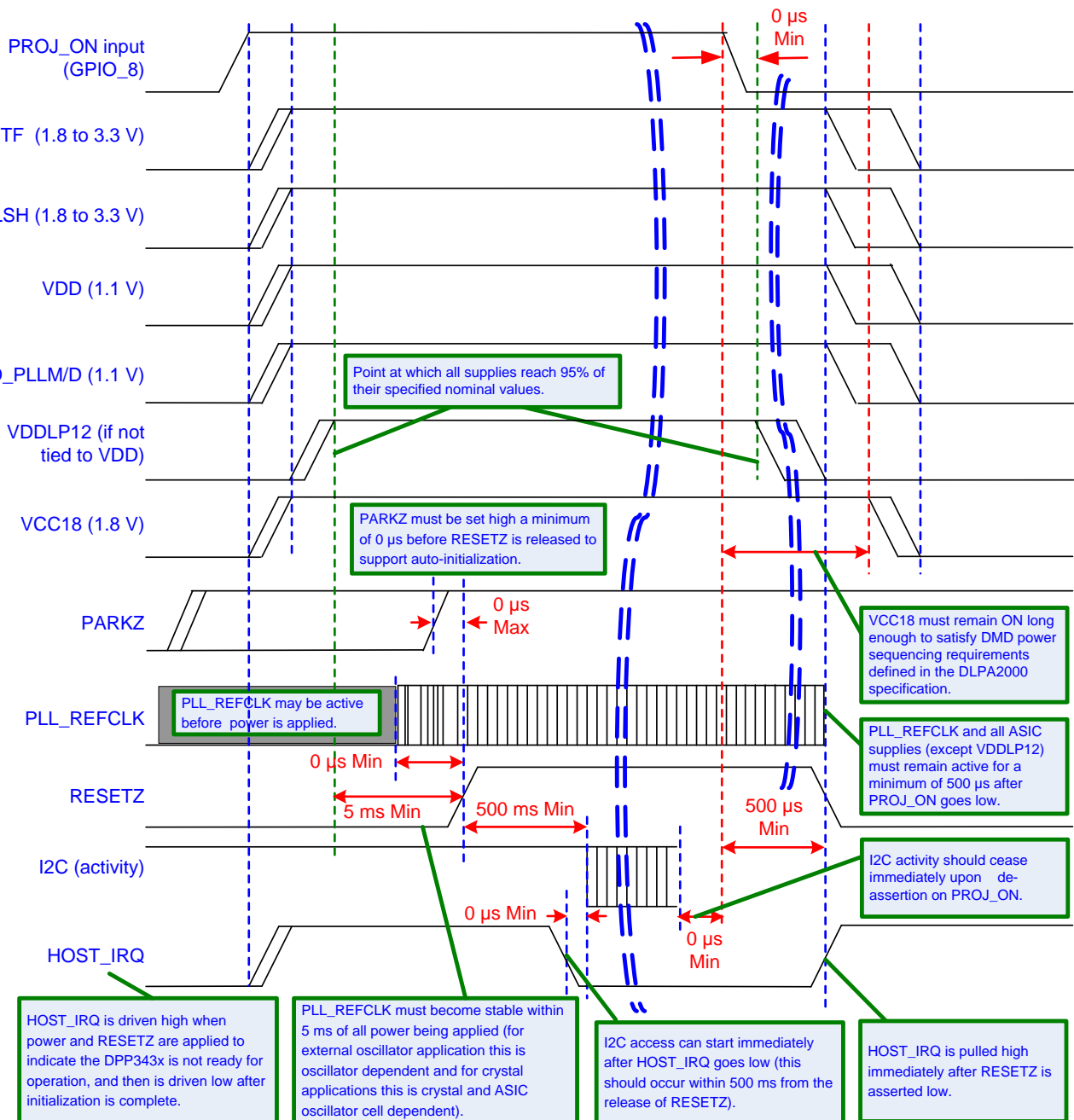## System Power-Up and Power-Down Sequence (continued)

Figure 22. DLPC343x Power-Up / PROJ_ON = 0 Initiated Normal PARK and Power-Down

System Power-Up and Power-Down Sequence (continued)

PROJ_ON input (GPIO_8)

VCC_INTF (1.8 to 3.3 V)

VCC_FLSH (1.8 to 3.3 V)

VDD (1.1 V)

VDD_PLLM/D (1.1 V)

VDDLP12 (if not tied to VDD)

VCC18 (1.8 V)

PARKZ

PLL_REFCLK

RESETZ

I2C (activity)

HOST_IRQ

Point at which all supplies reach 95% of their specified nominal values.

PARKZ must be set high a minimum of 0 µs before RESETZ is released to support auto-initialization.

0 µs Min

0 µs Max

VCC18 must remain ON long enough to satisfy DMD power sequencing requirements defined in the DLPA2000 specification.

32 µs Min

PARKZ must be set low a minimum of 32 µs before any power is removed (except VDDLP12), before PLL_REFCLK is stopped and before RESETZ is asserted low to allow time for the DMD mirrors to be parked.

PLL_REFCLK may be active before power is applied.

0 µs Min

5 ms Min

500 ms Min

I2C activity should cease immediately upon active low assertion of PARKZ.

0 µs Min

0 µs Min

HOST_IRQ is driven high when power and RESETZ are applied to indicate the DPP343x is not ready for operation, and then is driven low after initialization is complete.

PLL_REFCLK must become stable within 5 ms of all power being applied (for external oscillator application this is oscillator dependent and for crystal applications this is crystal and ASIC oscillator cell dependent).

I2C access can start immediately after HOST_IRQ goes low (this should occur within 500 ms from the release of RESETZ)

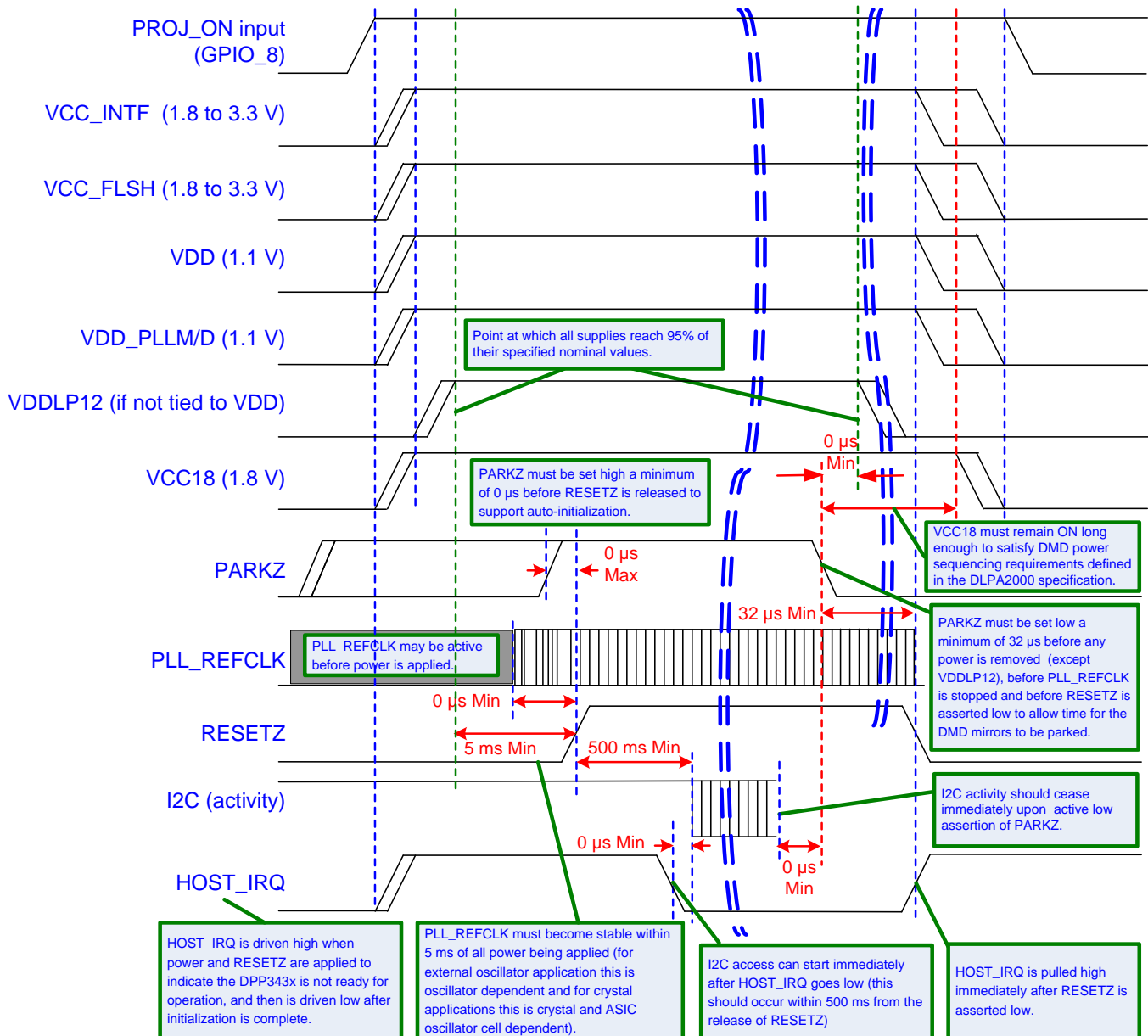HOST_IRQ is pulled high immediately after RESETZ is asserted low.

Figure 23. DLPC343x Power-Up / PARKZ = 0 initiated Fast PARK and Power-Down

10.2 DLPC343x Power-Up Initialization Sequence

It is assumed that an external power monitor will hold the DLPC343x in system reset during power-up. It must do this by driving RESETZ to a logic low state. It should continue to assert system reset until all ASIC voltages have reached minimum specified voltage levels, PARKZ is asserted high, and input clocks are stable. During this time, most ASIC outputs will be driven to an inactive state and all bidirectional signals will be configured as inputs to avoid contention. ASIC outputs that are not driven to an inactive state are tri-stated. These include LED_SEL_0, LED_SEL_1, SPICLK, SPIDOUT, and SPICSZ0 (see RESETZ pin description for full signal descriptions in *Pin Configuration and Functions*. After power is stable and the PLL_REFCLK_I clock input to the DLPC343x is stable, then RESETZ should be deactivated (set to a logic high). The DLPC343x then performs a power-up initialization routine that first locks its PLL followed by loading self configuration data from the external flash.

DLPC343x Power-Up Initialization Sequence (continued)

Upon release of RESETZ all DLPC343x I/Os will become active. Immediately following the release of RESETZ, the HOST_IRQ signal will be driven high to indicate that the auto initialization routine is in progress. However, since a pullup resistor is connected to signal HOST_IRQ, this signal will have already gone high before the DLPC343x actively drives it high. Upon completion of the auto-initialization routine, the DLPC343x will drive HOST_IRQ low to indicate the initialization done state of the DLPC343x has been reached.

Note that the host processor can start sending I^{2}C commands after HOST_IRQ goes low.

10.3 DMD Fast PARK Control (PARKZ)

The PARKZ signal is defined to be an early warning signal that should alert the ASIC 40 µs before DC supply voltages have dropped below specifications in fast PARK operation. This allows the ASIC time to park the DMD, ensuring the integrity of future operation. Note that the reference clock should continue to run and RESETZ should remain deactivated for at least 40 µs after PARKZ has been deactivated (set to a logic low) to allow the park operation to complete.

10.4 Hot Plug Usage

The DLPC343x provides fail-safe I/O on all host interface signals (signals powered by VCC_INTF). This allows these inputs to be driven high even when no I/O power is applied. Under this condition, the DLPC343x will not load the input signal nor draw excessive current that could degrade ASIC reliability. For example, the I^{2}C bus from the host to other components would not be affected by powering off VCC_INTF to the DLPC343x. TI recommends weak pullups or pulldowns on signals feeding back to the host to avoid floating inputs.

If the I/O supply (VCC_INTF) is powered off, but the core supply (VDD) is powered on, then the corresponding input buffer may experience added leakage current, but this does not damage the DLPC343x.

10.5 Maximum Signal Transition Time

Unless otherwise noted, 10 ns is the maximum recommended 20 to 80% rise or fall time to avoid input buffer oscillation. This applies to all DLPC343x input signals. However, the PARKZ input signal includes an additional small digital filter that ignores any input buffer transitions caused by a slower rise or fall time for up to 150 ns.

Product Folder Links: *DLPC3430 DLPC3435*
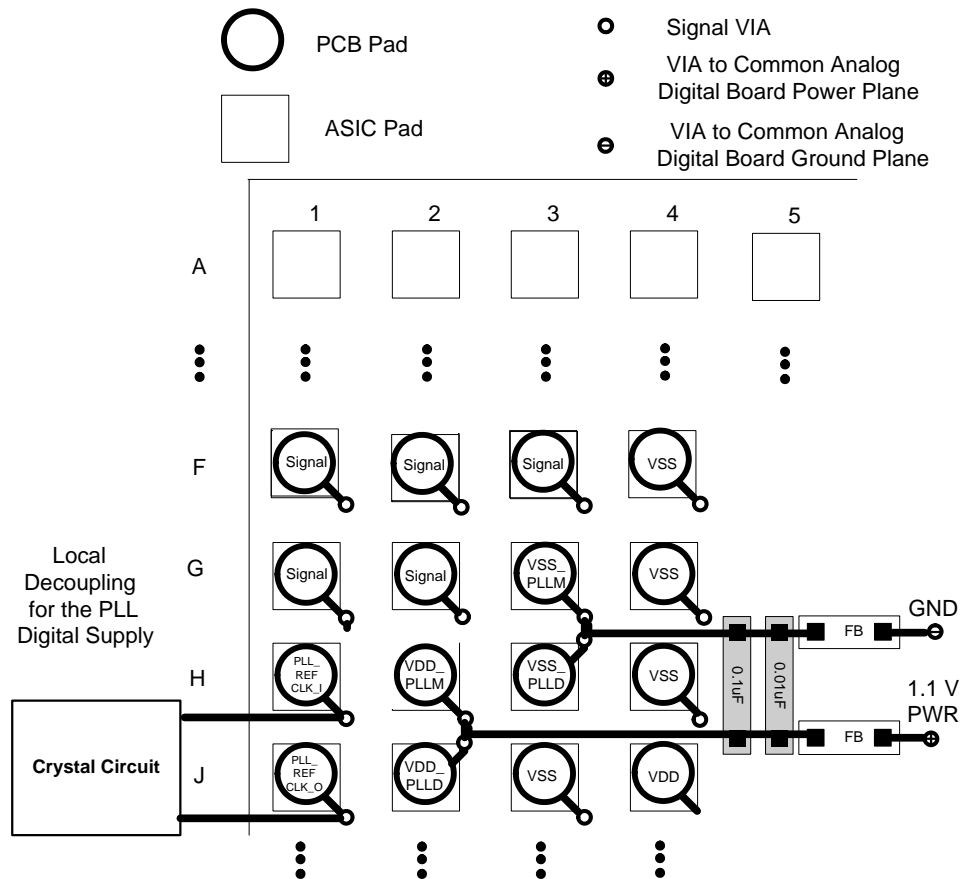
11 Layout

11.1 Layout Guidelines

11.1.1 PCB Layout Guidelines for Internal ASIC PLL Power

The following guidelines are recommended to achieve desired ASIC performance relative to the internal PLL. The DLPC343x contains 2 internal PLLs which have dedicated analog supplies (VDD_PLLM , VSS_PLLM, VDD_PLLD, VSS_PLLD). As a minimum, VDD_PLLx power and VSS_PLLx ground pins should be isolated using a simple passive filter consisting of two series Ferrites and two shunt capacitors (to widen the spectrum of noise absorption). It's recommended that one capacitor be a 0.1uf capacitor and the other be a 0.01uf capacitor. All four components should be placed as close to the ASIC as possible but it's especially important to keep the leads of the high frequency capacitors as short as possible. Note that both capacitors should be connected across VDD_PLLM and VSS_PLLM / VDD_PLLD and VSS_PLLD respectfully on the ASIC side of the Ferrites.

For the ferrite beads used, their respective characteristics should be as follows:
• DC resistance less than 0.40 Ω
• Impedance at 10 MHz equal to or greater than 180 Ω
• Impedance at 100 MHz equal to or greater than 600 Ω

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD_PLLM and VDD_PLLD must be a single trace from the DLPC343x to both capacitors and then through the series ferrites to the power source. The power and ground traces should be as short as possible, parallel to each other, and as close as possible to each other.

Figure 24. PLL Filter Layout

Layout Guidelines (continued)

11.1.2 DLPC343x Reference Clock

The DLPC343x requires an external reference clock to feed its internal PLL. A crystal or oscillator can supply this reference. For flexibility, the DLPC343x accepts either of two reference clock frequencies (see Table 11), but both must have a maximum frequency variation of ±200 ppm (including aging, temperature, and trim component variation). When a crystal is used, several discrete components are also required as shown in Figure 25.
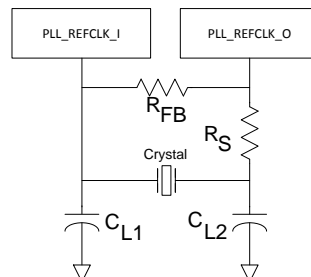
A. CL = Crystal load capacitance (farads)

B. CL1 = 2 × (CL − Cstray_pll_refclk_i)

C. CL2 = 2 × (CL − Cstray_pll_refclk_o)

D. Where: Cstray_pll_refclk_i = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_i. Cstray_pll_refclk_o = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_o.

Figure 25.

11.1.2.1 Recommended Crystal Oscillator Configuration

Table 10. Crystal Port Characteristics

Parameter	Nominal	Unit
PLL_REFCLK_I TO GND capacitance	1.5	pF
PLL_REFCLK_O TO GND capacitance	1.5	pF

Table 11. Recommended Crystal Configuration[1][2]

Parameter	Recommended	Unit
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	24 or 16	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	±200	PPM
Maximum startup time	1.0	ms
Crystal equivalent series resistance (ESR)	120 max	Ω
Crystal load	6	pF
RS drive resistor (nominal)	100	Ω
RFB feedback resistor (nominal)	1Meg	Ω
CL1 external crystal load capacitor	See equation in Figure 25 notes	pF
CL2 external crystal load capacitor	See equation in Figure 25 notes	pF
PCB layout	A ground isolation ring around the crystal is recommended	

(1) Temperature range of –30°C to +85°C
(2) The crystal bias is determined by the ASIC's VCC_INTF voltage rail, which is variable (not the VCC18 rail).

If an external oscillator is used, then the oscillator output must drive the PLL_REFCLK_I pin on the DLPC343x ASIC and the PLL_REFCLK_O pins should be left unconnected.

Table 12. DLPC343x Recommended Crystal Parts[1][2][3]

Passed DVT	Manufacturer	Part Number	Speed	Temperature and Aging	ESR	Load Capacitance
Yes	KDS	DSX211G-24.000M-8pF-50-50	24 MHz	±50 ppm	120-Ω max	8 pF
No	Muratta	XRCGB24M000F0L11R0	24 MHz	±100 ppm	120-Ω max	6 pF
No	NDK	NX2016SA 24M EXS00A-CS05733	24 MHz	±145 ppm	120-Ω max	6 pF

(1)   These crystal devices appear compatible with the DLPC343x, but only those marked with yes in the DVT column have been validated.
(2)   Crystal package sizes: 2.0 × 1.6 mm for both crystals
(3)   Operating temperature range: –30°C to +85°C for all crystals

11.1.3 General PCB Recommendations

TI recommends 1-oz. copper planes in the PCB design to achieve needed thermal connectivity.

11.1.4 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends that unused ASIC input pins be tied through a pullup resistor to its associated power supply or a pulldown to ground. For ASIC inputs with an internal pullup or pulldown resistors, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Note that internal pullup and pulldown resistors are weak and should not be expected to drive the external line. The DLPC343x implements very few internal resistors and these are noted in the pin list. When external pullup or pulldown resistors are needed for pins that have built-in weak pullups or pulldowns, use the value 8 kΩ (max).

Unused output-only pins should never be tied directly to power or ground, but can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled-up (or pulled-down) using an appropriate, dedicated resistor.

11.1.5 Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

Table 13. Max Pin-to-Pin PCB Interconnect Recommendations[1][2]

DMD Bus Signal	Signal Interconnect Topology		Unit
	Single Board Signal Routing Length	Multi-Board Signal Routing Length	
DMD_HS_CLK_P DMD_HS_CLK_N	6.0 152.4	See [3]	inch (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	6.0 152.4	See [3]	inch (mm)
DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD_LS_CLK	6.5 165.1	See [3]	inch (mm)
DMD_LS_WDATA	6.5 165.1	See [3]	inch (mm)
DMD_LS_RDATA	6.5 165.1	See [3]	inch (mm)
DMD_DEN_ARSTZ	7.0 177.8	See [3]	inch (mm)

(1) Max signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.
(3) Due to board variations, these are impossible to define. Any board designs should SPICE simulate with the ASIC IBIS models to ensure single routing lengths do not exceed requirements.

Product Folder Links: *DLPC3430 DLPC3435*

Table 14. High Speed PCB Signal Routing Matching Requirements[1][2][3][4]

Signal Group Length Matching				
Interface	Signal Group	Reference Signal	Max Mismatch[5]	Unit
DMD	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N	DMD_HS_CLK_P DMD_HS_CLK_N	±0.1 (±25.4)	inch (mm)
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	inch (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

(1) These values apply to PCB routing only. They do not include any internal package routing mismatch associated with the DLPC343x, the DMD.
(2) DMD HS data lines are differential, thus these specifications are pair-to-pair.
(3) Training is applied to DMD HS data lines, so defined matching requirements are slightly relaxed.
(4) DMD LS signals are single ended.
(5) Mismatch variance applies to high-speed data pairs. For all high-speed data pairs, the maximum mismatch between pairs should be 1 mm or less.

11.1.6 Number of Layer Changes

• Single-ended signals: Minimize the number of layer changes
• Differential signals: Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.

11.1.7 Stubs

• Stubs should be avoided

11.1.8 Terminations

• No external termination resistors are required on DMD_HS differential signals.
• The DMD_LS_CLK and DMD_LS_WDATA signal paths should include a 43-Ω series termination resistor located as close as possible to the corresponding ASIC pins.
• The DMD_LS_RDATA signal path should include a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
• DMD_DEN_ARSTZ does not require a series resistor.

11.1.9 Routing Vias

• The number of vias on DMD_HS signals should be minimized and should not exceed two.
• Any and all vias on DMD_HS signals should be located as close to the ASIC as possible.
• The number of vias on the DMD_LS_CLK and DMD_LS_WDATA signals should be minimized and not exceed two.
• Any and all vias on the DMD_LS_CLK and DMD_LS_WDATA signals should be located as close to the ASIC as possible.

11.1.10 Thermal Considerations

The underlying thermal limitation for the DLPC343x is that the maximum operating junction temperature (T_J) not be exceeded (this is defined in the *Recommended Operating Conditions*). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC343x, and power dissipation of surrounding components. The DLPC343x's package is designed primarily to extract heat through the power and ground planes of the PCB. Thus, copper content and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature (T_A) is provided primarily as a design target and is based on maximum DLPC343x power dissipation and $R_{\theta JA}$ at 0 m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using a glater test PCB with two, 1-oz power planes. This JEDEC test PCB is not necessarily representative of the DLPC343x PCB; the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. However, after the PCB is designed and the product is built, TI highly recommended that thermal performance be measured and validated.

To do this, measure the top center case temperature under the worse case product scenario (max power dissipation, max voltage, max ambient temperature) and validated not to exceed the maximum recommended case temperature (T_C). This specification is based on the measured φ_{JT} for the DLPC343x package and provides a relatively accurate correlation to junction temperature. Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40 gauge) thermocouple. The bead and thermocouple wire should contact the top of the package and be covered with a minimal amount of thermally conductive epoxy. The wires should be routed closely along the package and the board surface to avoid cooling the bead through the wires.

11.2 Layout Example
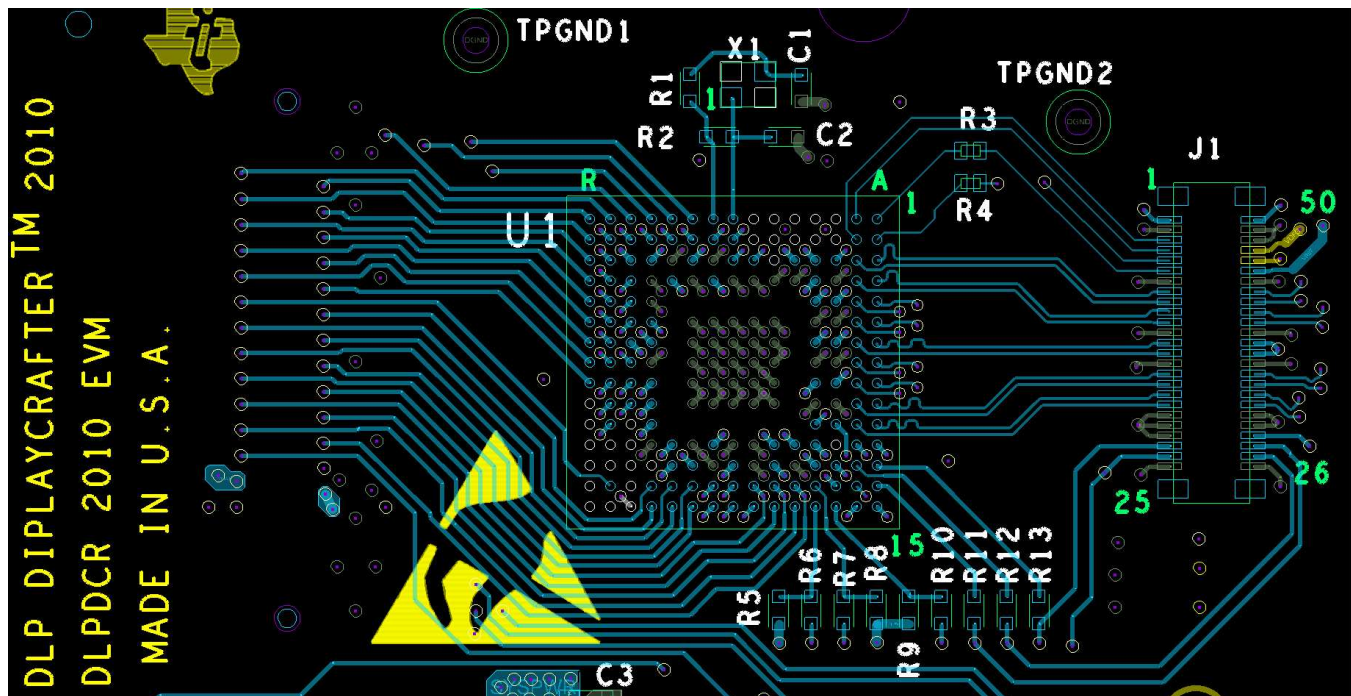
12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 Device Nomenclature

12.1.2.1 Device Markings
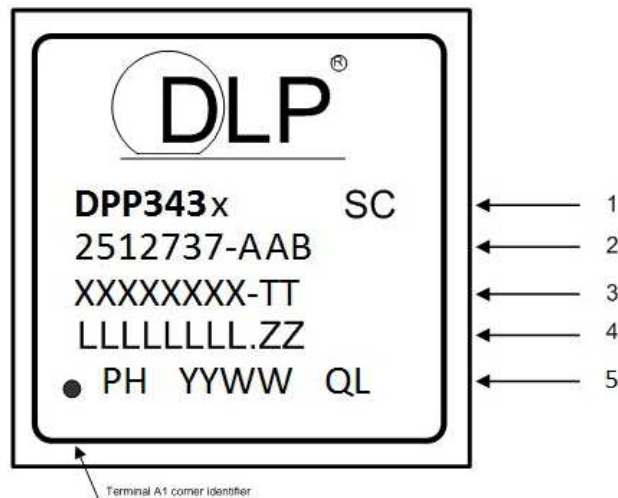
Marking Definitions:

Line 1:   DLP Device Name: DLPC343x = **x** indicates a 0 or 5 device name ID.
SC: Solder ball composition
   e1: Indicates lead-free solder balls consisting of SnAgCu
   G8: Indicates lead-free solder balls consisting of tin-silver-copper (SnAgCu) with silver content less than or equal to 1.5% and that the mold compound meets TI's definition of green.

Line 2:   TI Part Number
AAB (1 → 4 alphanumeric) = **AA** corresponds to the TI device dash number. **B** is reserved for unqualified device marking. All unqualified device, including prototypes and skew lot samples, are labeled with the letter **X** in the **B** marking location (following the TI part number). **B** is left blank for qualified devices.

Line 3:   XXXXXXXX-TT manufacturer part number

Line 4:   LLLLLLLL.ZZZ Foundry lot code for semiconductor wafers and lead-free solder ball marking
LLLLLLLL: Fab lot number
ZZZ: Lot split number

Line 5:   PH YYWW ES : Package assembly information
PH: Manufacturing site
YYWW: Date code (YY = Year :: WW = Week)
QL: Qualification level option – Engineering samples are marked in this field with an ES suffix.
   For example, PH 1314 ES is for engineering samples built in Philippines the 14th week of 2013

Device Support (continued)

NOTE

1. Engineering prototype samples are marked with an **X** suffix appended to the TI part number. For example, 2512737-0001X.
2. See Table 3, for DLPC343x resolutions on the DMD supported per part number.

12.1.3 Video Timing Parameter Definitions

Active Lines Per Frame (ALPF) Defines the number of lines in a frame containing displayable data: ALPF is a subset of the TLPF.

Active Pixels Per Line (APPL) Defines the number of pixel clocks in a line containing displayable data: APPL is a subset of the TPPL.

Horizontal Back Porch (HBP) Blanking Number of blank pixel clocks after horizontal sync but before the first active pixel. Note: HBP times are reference to the leading (active) edge of the respective sync signal.

Horizontal Front Porch (HFP) Blanking Number of blank pixel clocks after the last active pixel but before Horizontal Sync.

Horizontal Sync (HS) Timing reference point that defines the start of each horizontal interval (line). The absolute reference point is defined by the active edge of the HS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.

Total Lines Per Frame (TLPF) Defines the vertical period (or frame time) in lines: TLPF = Total number of lines per frame (active and inactive).

Total Pixel Per Line (TPPL) Defines the horizontal line period in pixel clocks: TPPL = Total number of pixel clocks per line (active and inactive).

Vertical Sync (VS) Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured.

Vertical Back Porch (VBP) Blanking Number of blank lines after vertical sync but before the first active line.

Vertical Front Porch (VFP) Blanking Number of blank lines after the last active line but before vertical sync.
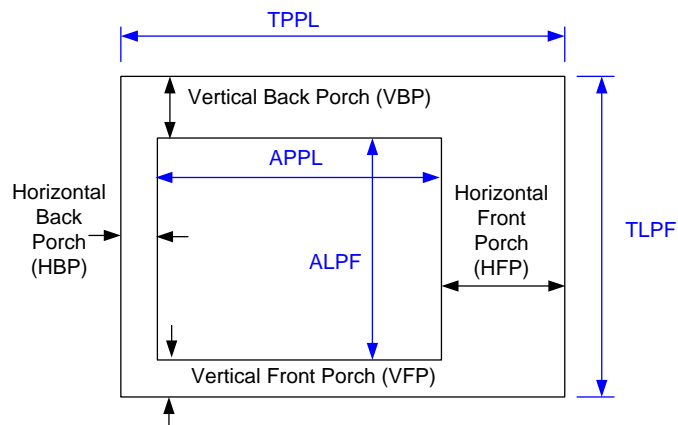
12.2 Related Links

The following table lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 15. Related Links

PARTS	PRODUCT FOLDER	SAMPLE and BUY	TECHNICAL DOCUMENTS	TOOLS and SOFTWARE	SUPPORT and COMMUNITY
DLPC3430	Click here	Click here	Click here	Click here	Click here
DLPC3435	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

IntelliBright is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

   This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 DLPC3430 Mechanical Data

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	DMD_LS_CLK	DMD_LS_WDATA	DMD_HS_WDATAH_P	DMD_HS_WDATAG_P	DMD_HS_WDATAF_P	DMD_HS_WDATAE_P	DMD_HS_CLK_P	DMD_HS_WDATAD_P	DMD_HS_WDATAC_P	DMD_HS_WDATAB_P	DMD_HS_WDATAA_P	CMP_OUT	SPI0_CLK	SPI0_CSZ0	CMP_PWM
B	DMD_DEN_ARSTZ	DMD_LS_RDATA	DMD_HS_WDATAH_N	DMD_HS_WDATAG_N	DMD_HS_WDATAF_N	DMD_HS_WDATAE_N	DMD_HS_CLK_N	DMD_HS_WDATAD_N	DMD_HS_WDATAC_N	DMD_HS_WDATAB_N	DMD_HS_WDATAA_N	SPI0_DIN	SPI0_DOUT	LED_SEL_1	LED_SEL_0
C	DD3P	DD3N	VDDLP12	VSS	VDD	VSS	VCC	VSS	VCC	HWTEST_EN	RESETZ	SPI0_CSZ1	PARKZ	GPIO_00	GPIO_01
D	DD2P	DD2N	VDD	VCC	VDD	VSS	VDD	VSS	VDD	VSS	VCC_FLSH	VDD	VDD	GPIO_02	GPIO_03
E	DCLKP	DCLKN	VDD	VSS								VCC	VSS	GPIO_04	GPIO_05
F	DD1P	DD1N	RREF	VSS								VCC	VDD	GPIO_06	GPIO_07
G	DD0P	DD0N	VSS_PLLM	VSS								VSS	VSS	GPIO_08	GPIO_09
H	PLL_REFCLK_I	VDD_PLLM	VSS_PLLD	VSS								VSS	VDD	GPIO_10	GPIO_11
J	PLL_REFCLK_O	VDD_PLLD	VSS	VDD								VDD	VSS	GPIO_12	GPIO_13
K	PDATA_1	PDATA_0	VDD	VSS								VSS	VCC	GPIO_14	GPIO_15
L	PDATA_3	PDATA_2	VSS	VDD								VDD	VDD	GPIO_16	GPIO_17
M	PDATA_5	PDATA_4	VCC_INTF	VSS	VSS	VDD	VCC_INTF	VSS	VDD	VDD	VCC	VSS	JTAGTMS1	GPIO_18	GPIO_19
N	PDATA_7	PDATA_6	VCC_INTF	PDM_CVS_TE	HSYNC_CS	3DR	VCC_INTF	HOST_IRQ	IIC0_SDA	IIC0_SCL	JTAGTMS2	JTAGTDO2	JTAGTDO1	TSTPT_6	TSTPT_7
P	VSYNC_WE	DATEN_CMD	PCLK	PDATA_11	PDATA_13	PDATA_15	PDATA_17	PDATA_19	PDATA_21	PDATA_23	JTAGTRSTZ	JTAGTCK	JTAGTDI	TSTPT_4	TSTPT_5
R	PDATA_8	PDATA_9	PDATA_10	PDATA_12	PDATA_14	PDATA_16	PDATA_18	PDATA_20	PDATA_22	IIC1_SDA	IIC1_SCL	TSTPT_0	TSTPT_1	TSTPT_2	TSTPT_3

Figure 26. 7- × 7-mm Package – VF Ball Grid Array

Product Folder Links: *DLPC3430 DLPC3435*

13.2 DLPC3435 Mechanical Data

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	DMD_LS_CLK	DMD_LS_WDATA	DMD_HS_WDATAH_P	DMD_HS_WDATAG_P	DMD_HS_WDATAF_P	DMD_HS_WDATAE_P	DMD_HS_WCLK_P	DMD_HS_WDATAD_P	DMD_HS_WDATAC_P	DMD_HS_WDATAB_P	DMD_HS_WDATAA_P	CMP_OUT	SPI0_CLK	SPI0_CSZ0	CMP_PWM
B	DMD_DEN_ARSTZ	DMD_LS_RDATA	DMD_HS_WDATAH_N	DMD_HS_WDATAG_N	DMD_HS_WDATAF_N	DMD_HS_WDATAE_N	DMD_HS_WCLK_N	DMD_HS_WDATAD_N	DMD_HS_WDATAC_N	DMD_HS_WDATAB_N	DMD_HS_WDATAA_N	SPI0_DIN	SPI0_DOUT	LED_SEL_1	LED_SEL_0
C	DD3P	DD3N	VDDLP12	VSS	VDD	VSS	VCC	VSS	VCC	HWTEST_EN	RESETZ	SPI0_CSZ1	PARKZ	GPIO_00	GPIO_01
D	DD2P	DD2N	VDD	VCC	VDD	VSS	VDD	VSS	VDD	VSS	VCC_FLSH	VDD	VDD	GPIO_02	GPIO_03
E	DCLKP	DCLKN	VDD	VSS								VCC	VSS	GPIO_04	GPIO_05
F	DD1P	DD1N	RREF	VSS		VSS	VSS	VSS	VSS	VSS		VCC	VDD	GPIO_06	GPIO_07
G	DD0P	DD0N	VSS_PLLM	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VSS	GPIO_08	GPIO_09
H	PLL_REFCLK_I	VDD_PLLM	VSS_PLLD	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VDD	GPIO_10	GPIO_11
J	PLL_REFCLK_O	VDD_PLLD	VSS	VDD		VSS	VSS	VSS	VSS	VSS		VDD	VSS	GPIO_12	GPIO_13
K	PDATA_1	PDATA_0	VDD	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VCC	GPIO_14	GPIO_15
L	PDATA_3	PDATA_2	VSS	VDD								VDD	VDD	GPIO_16	GPIO_17
M	PDATA_5	PDATA_4	VCC_INTF	VSS	VSS	VDD	VCC_INTF	VSS	VDD	VDD	VCC	VSS	JTAGTMS1	GPIO_18	GPIO_19
N	PDATA_7	PDATA_6	VCC_INTF	PDM_CVS_TE	HSYNC_CS	3DR	VCC_INTF	HOST_IRQ	IIC0_SDA	IIC0_SCL	JTAGTMS2	JTAGTDO2	JTAGTDO1	TSTPT_6	TSTPT_7
P	VSYNC_WE	DATEN_CMD	PCLK	PDATA_11	PDATA_13	PDATA_15	PDATA_17	PDATA_19	PDATA_21	PDATA_23	JTAGTRSTZ	JTAGTCK	JTAGTDI	TSTPT_4	TSTPT_5
R	PDATA_8	PDATA_9	PDATA_10	PDATA_12	PDATA_14	PDATA_16	PDATA_18	PDATA_20	PDATA_22	IIC1_SDA	IIC1_SCL	TSTPT_0	TSTPT_1	TSTPT_2	TSTPT_3

Figure 27. 7- × 7-mm Package – VF Ball Grid Array

Product Folder Links: DLPC3430 DLPC3435

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC3430ZVB	ACTIVE			176		Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR			Samples
DLPC3430ZVBR	ACTIVE			176	3000	TBD	Call TI	Call TI			Samples
DLPC3435ZEZ	ACTIVE			201	260	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and the leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
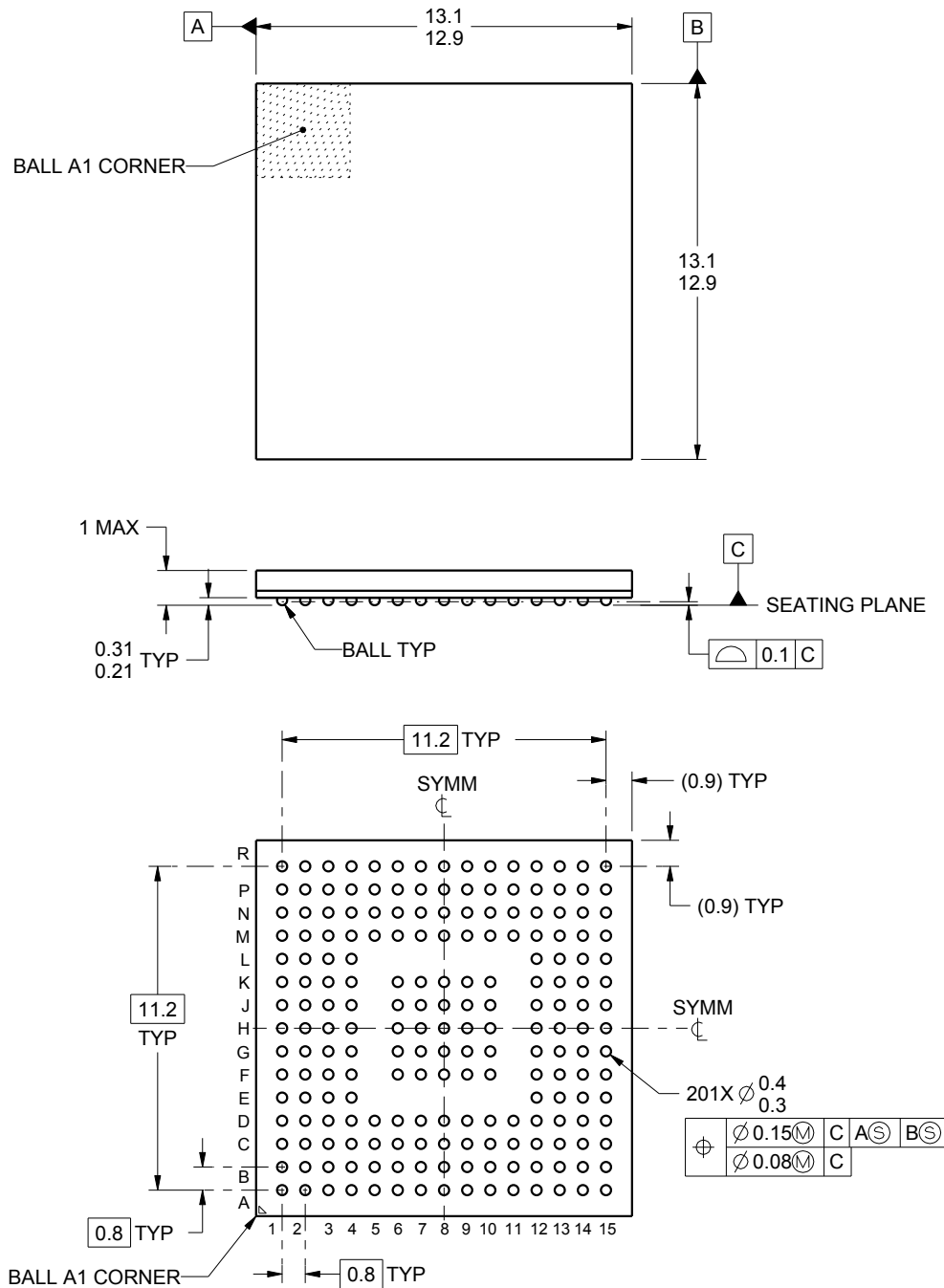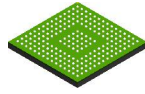
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

A | 13.1 / 12.9 | B

BALL A1 CORNER

13.1
12.9

1 MAX

C

SEATING PLANE

0.31
0.21 TYP

BALL TYP

⌒ 0.1 C

11.2 TYP

SYMM ℄

(0.9) TYP

(0.9) TYP

11.2
TYP

SYMM ℄

R P N M L K J H G F E D C B A

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

201X ⌀ 0.4 / 0.3

⊕ | ⌀ 0.15 Ⓜ | C | A Ⓢ | B Ⓢ
| ⌀ 0.08 Ⓜ | C |

0.8 TYP

BALL A1 CORNER
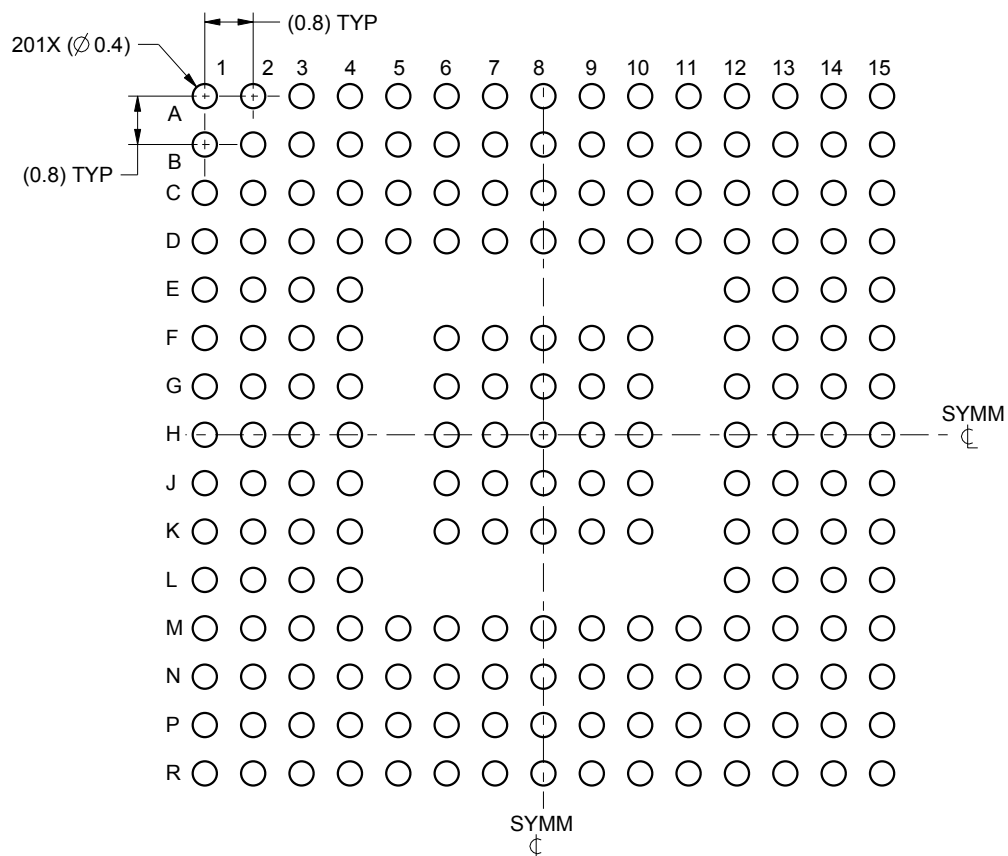
0.8 TYP

4221521/A 03/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
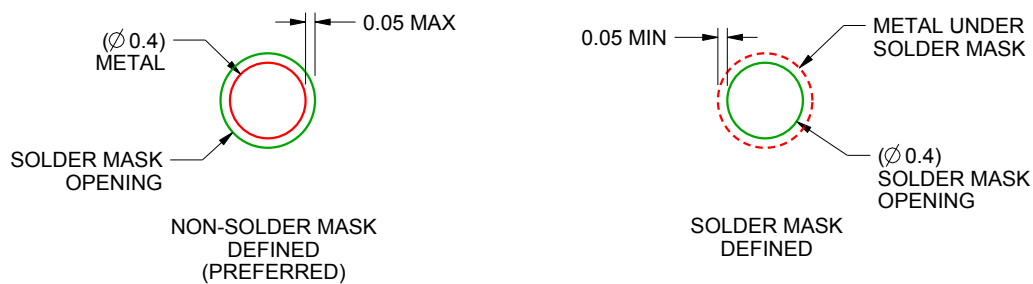2. This drawing is subject to change without notice.

ZEZ0201A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY

201X (∅ 0.4)

(0.8) TYP

(0.8) TYP

SYMM
₵

SYMM
₵

LAND PATTERN EXAMPLE
SCALE:8X

(∅ 0.4)
METAL

0.05 MAX

SOLDER MASK
OPENING

**NON-SOLDER MASK
DEFINED
(PREFERRED)**

0.05 MIN

METAL UNDER
SOLDER MASK

(∅ 0.4)
SOLDER MASK
OPENING

**SOLDER MASK
DEFINED**

SOLDER MASK DETAILS
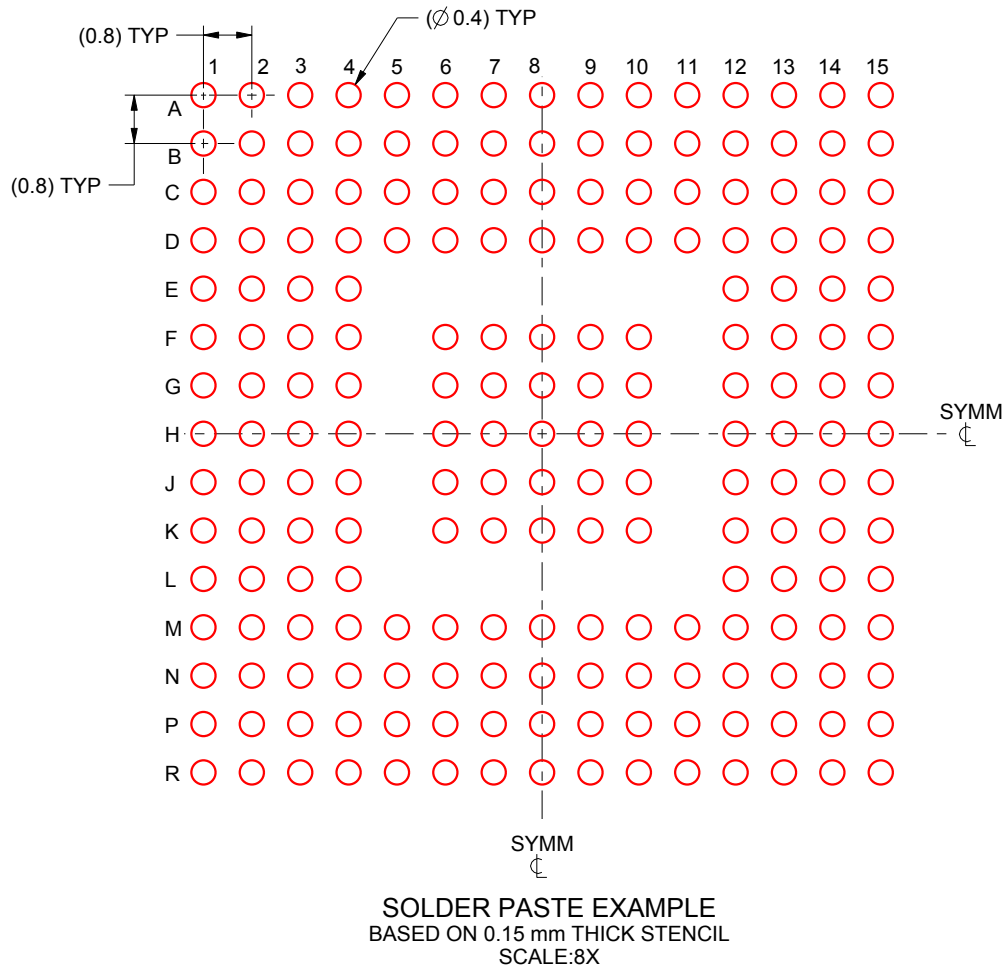NOT TO SCALE

4221521/A   03/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

ZEZ0201A

PLASTIC BALL GRID ARRAY

SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4221521/A   03/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC3430ZVB	ACTIVE	NFBGA	ZVB	176		TBD	Call TI	Call TI			Samples
DLPC3430ZVBR	ACTIVE	NFBGA	ZVB	176	3000	TBD	Call TI	Call TI			Samples
DLPC3435ZEZ	ACTIVE	NFBGA	ZEZ	201	260	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR			Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
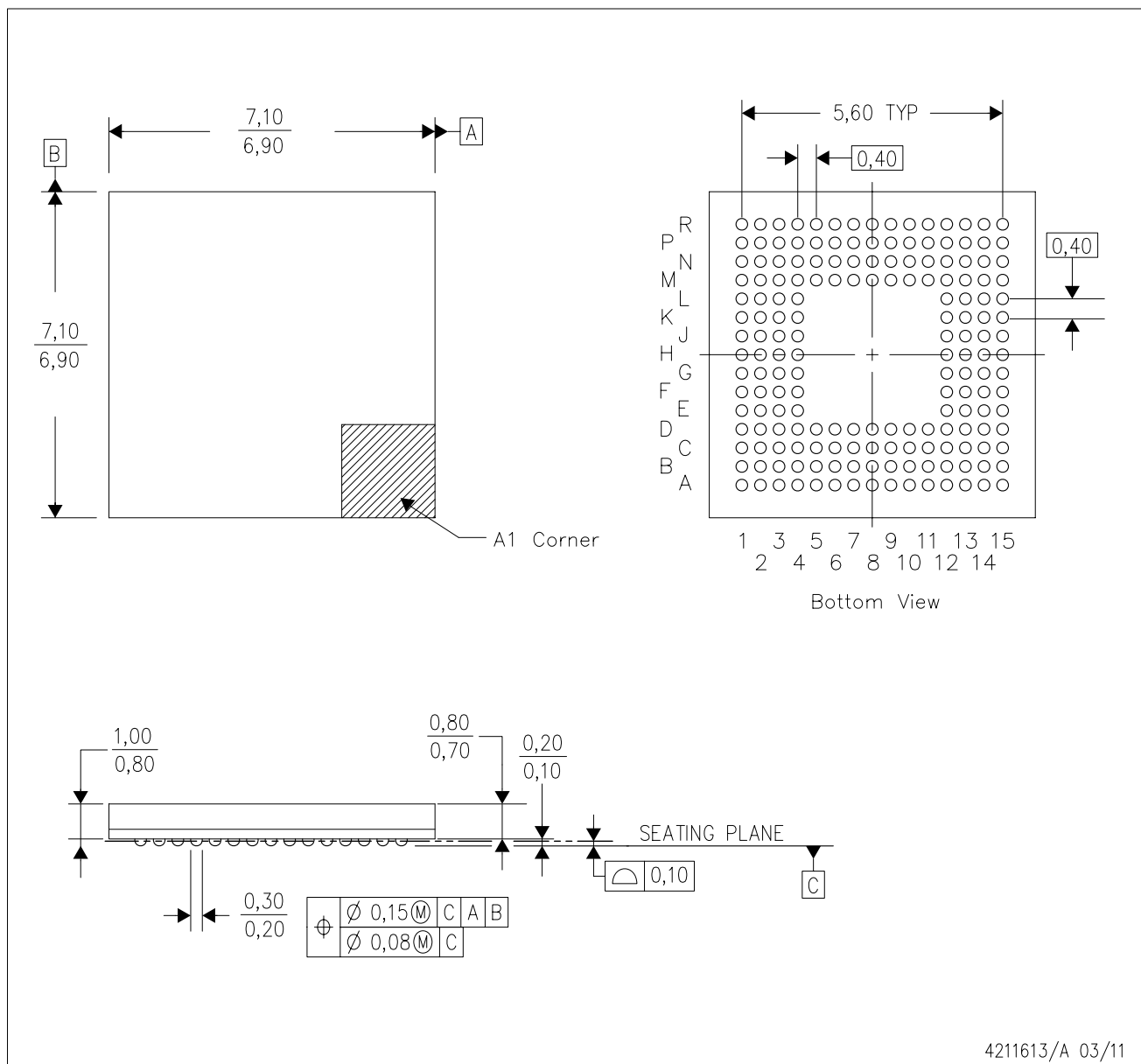
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
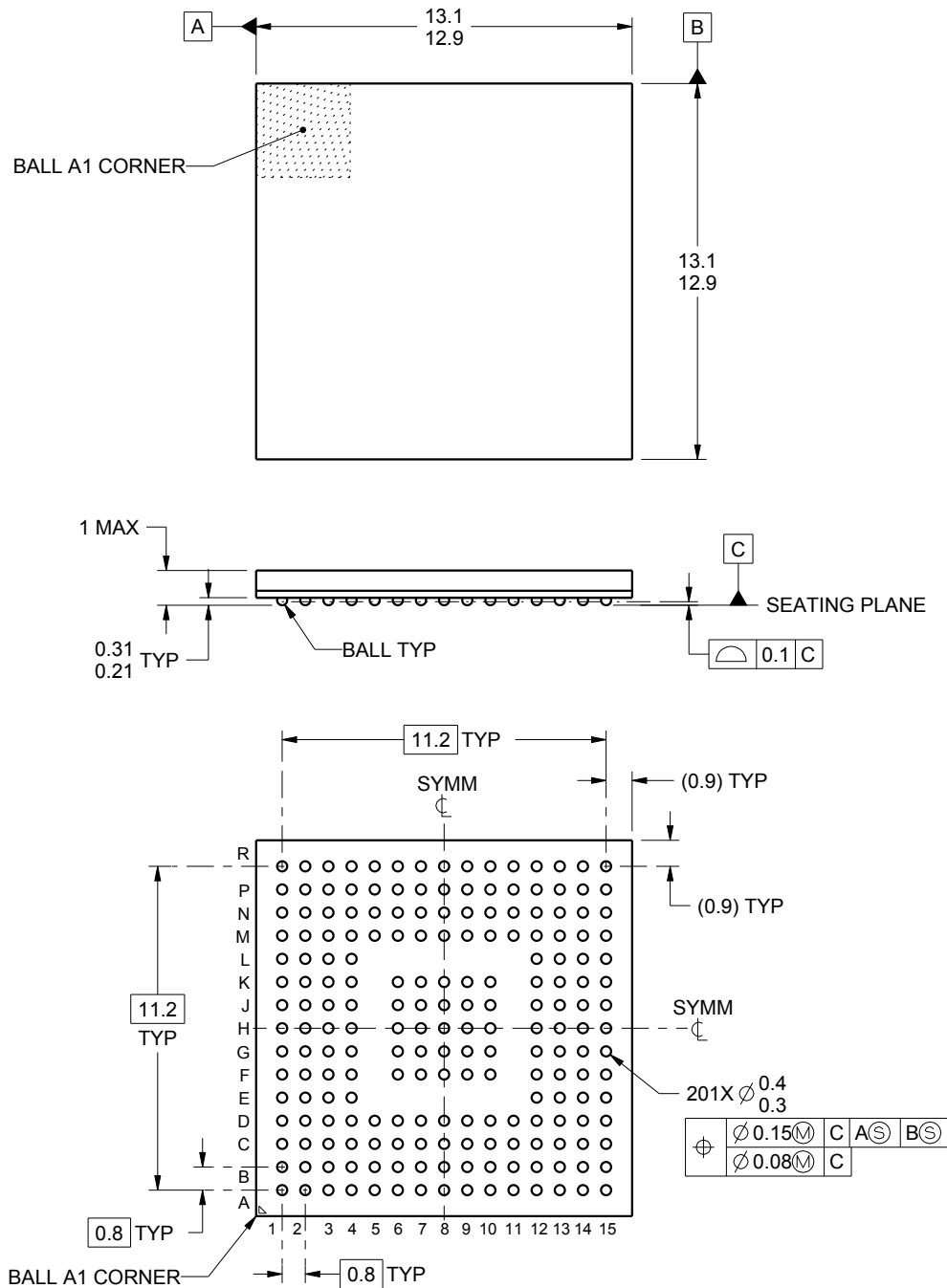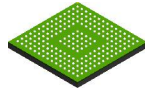
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

ZVB (S–PBGA–N176)   PLASTIC BALL GRID ARRAY

7,10
6,90

[B]   [A]

7,10
6,90

A1 Corner

5,60 TYP

0,40

0,40

R P N M L K J H G F E D C B A

1 3 5 7 9 11 13 15
 2 4 6 8 10 12 14

Bottom View

1,00
0,80

0,80
0,70

0,20
0,10

SEATING PLANE

0,10

[C]

0,30
0,20

⌖ | Ø 0,15 Ⓜ | C | A | B
  | Ø 0,08 Ⓜ | C

4211613/A 03/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
         B. This drawing is subject to change without notice.
         C. This package is Pb–free.

A

13.1
12.9

B

BALL A1 CORNER

13.1
12.9

1 MAX

C

SEATING PLANE

0.31
0.21 TYP

BALL TYP

⌒ 0.1 C

11.2 TYP

SYMM
₵

(0.9) TYP

(0.9) TYP

R
P
N
M
L
K
J
H
G
F
E
D
C
B
A

11.2
TYP

SYMM
₵

201X ⌀ 0.4
0.3

⊕ ⌀ 0.15Ⓜ C AⓈ BⓈ
⌀ 0.08Ⓜ C

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

0.8 TYP

BALL A1 CORNER
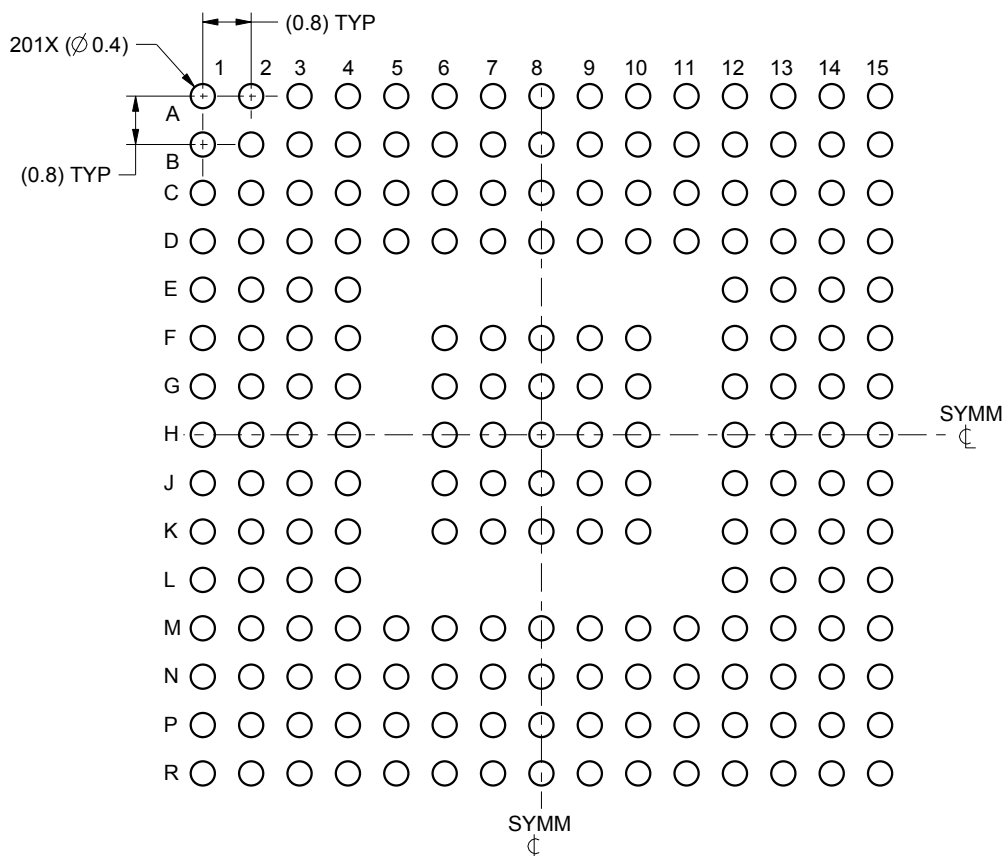
0.8 TYP

4221521/A   03/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
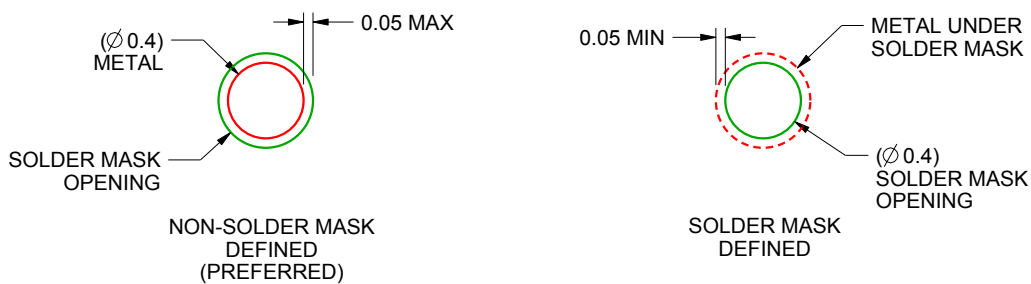2. This drawing is subject to change without notice.

ZEZ0201A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY

LAND PATTERN EXAMPLE
SCALE:8X

(0.8) TYP

201X (⌀ 0.4)

(0.8) TYP

SYMM ₡

SYMM ₡

(⌀ 0.4) METAL

SOLDER MASK OPENING

0.05 MAX

NON-SOLDER MASK DEFINED (PREFERRED)

0.05 MIN

METAL UNDER SOLDER MASK

(⌀ 0.4) SOLDER MASK OPENING

SOLDER MASK DEFINED

SOLDER MASK DETAILS
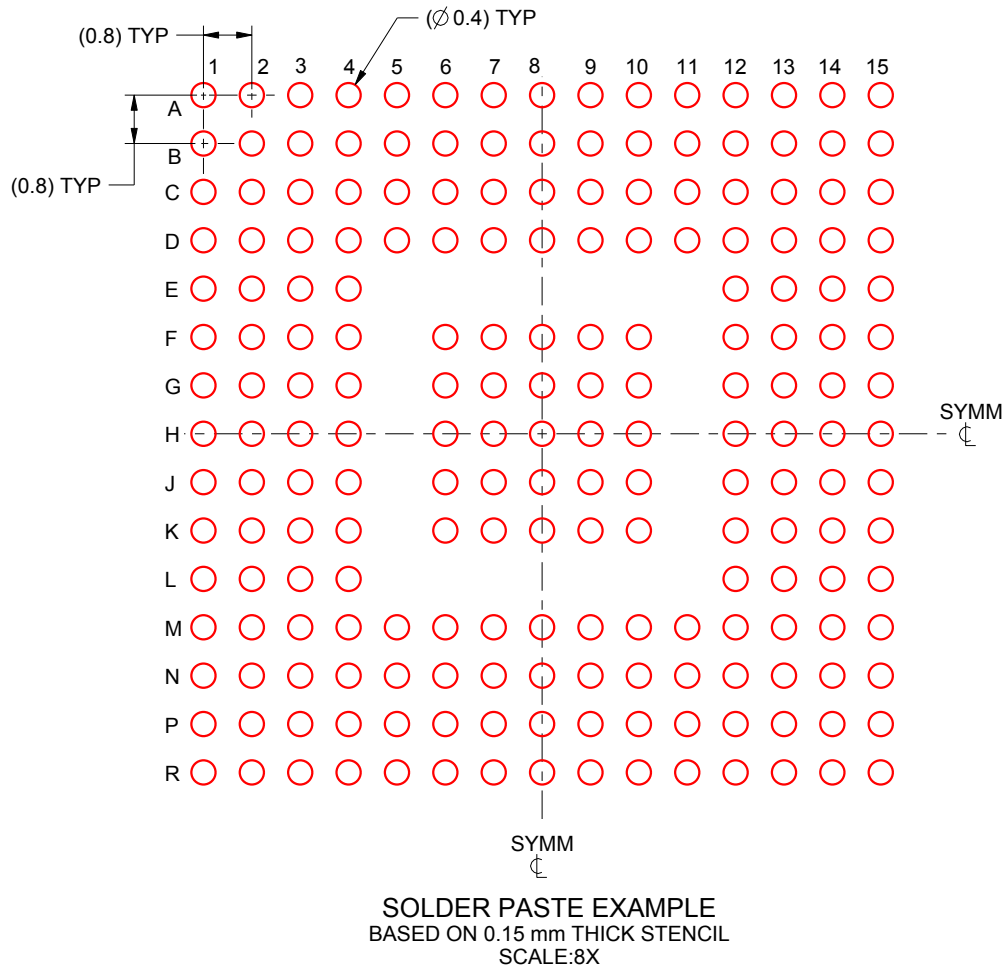NOT TO SCALE

4221521/A   03/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

ZEZ0201A

PLASTIC BALL GRID ARRAY

SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4221521/A   03/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video
TI E2E Community	e2e.ti.com