DS1077L
3V EconOscillator/Divider

www.maxim-ic.com

FEATURES

- Processor-controlled or stand-alone solid-state oscillator
- Frequency changes on the fly
- Dual, low-jitter, synchronous fixed-frequency outputs
- 2-wire serial interface
- Frequency outputs 4.87kHz to 66.666MHz ±1.25% variation over temperature and voltage
- ±0.5% initial tolerance
- Nonvolatile frequency settings
- Single 2.7V to 3.6V supply
- No external components
- Power-down mode
- Synchronous output gating

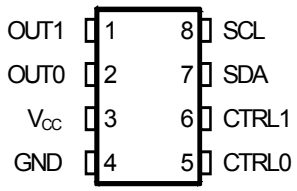
STANDARD FREQUENCY OPTION

Note: x denotes package option

DS1077Lx-40	40.000MHz	to	4.87kHz
DS1077Lx-50	50.000MHz	to	6.09kHz
DS1077Lx-60	60.000MHz	to	7.32kHz
DS1077Lx-66	66.666MHz	to	8.13kHz

Contact the factory for the availability of additional frequencies.

PIN ASSIGNMENTS



150mil SO
118mil µSOP*

PIN DESCRIPTIONS

OUT1	- Main Oscillator Output
OUT0	- Reference Output
V_{CC}	- Power-Supply Voltage
GND	- Ground
CTRL1	- Control Pin for OUT1
CTRL0	- Control Pin for OUT0
SDA	- 2-Wire Serial Data Input/Output
SCL	- 2-Wire Serial Clock

ORDERING INFORMATION

Note: XXX denotes frequency option

DS1077LZ-XXX	8-pin 150mil SO
DS1077LU-XXX*	8-pin 118mil µSOP

DESCRIPTION

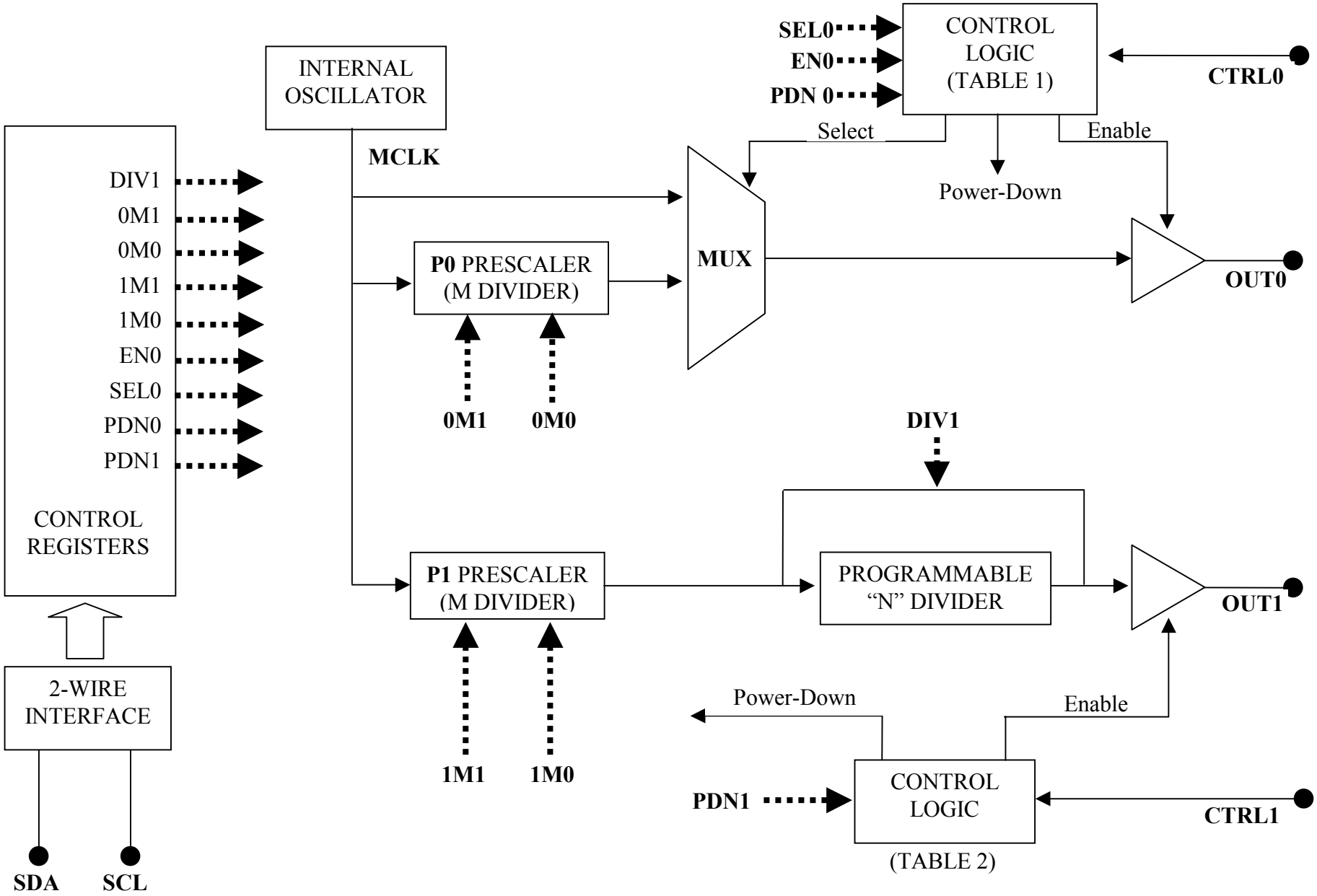
The DS1077L is a dual-output, programmable, fixed-frequency oscillator requiring no external components for operation. The DS1077L can be used as a processor-controlled frequency synthesizer or as a stand-alone oscillator. The two synchronous output operating frequencies are user-adjustable in submultiples of the master frequency through the use of two on-chip programmable prescalers and dividers. The specific output frequencies chosen are stored in nonvolatile (EEPROM) memory. The DS1077L defaults to these values upon power-up.

The DS1077L features a 2-wire serial interface that allows in-circuit on-the-fly programming of the programmable prescalers (P0 & P1) and divider (N) with the desired values being stored in nonvolatile (EEPROM) memory. Design changes can be accommodated in-circuit, on-the-fly by simply programming different values into the device (or reprogramming previously programmed devices). Alternatively, for fixed-frequency applications previously programmed devices can be used and no connection to the serial interface is required. Preprogrammed devices can be ordered in customer-requested frequencies.

The DS1077L is available in SO or µSOP packages, allowing the generation of a clock signal easily, economically, and using minimal board area. Chip-scale packaging is also available on request.

**Future product. Contact factory for availability.*

BLOCK DIAGRAM DS1077L Figure 1



OVERVIEW

A block diagram of the DS1077L is shown in Figure 1. The DS1077L consists of four major components: 1) internal master oscillator, 2) prescalers, 3) programmable divider, and 4) control registers.

The internal oscillator is factory trimmed to provide a master frequency (master clk) that can be routed directly to the outputs (OUT0 & OUT1) or through separate prescalers (P0 & P1). OUT1 can also be routed through an additional divider (N).

The prescaler (P0) divides the master clock by 1, 2, 4, or 8 to be routed directly to the OUT0 pin.

The prescaler (P1) divides the master clock by 1, 2, 4, or 8 that can be routed to the OUT1 pin or to the divider (N) input, which is then routed to the OUT1 pin.

The programmable divider (N) divides the prescaler output (P1) by any number selected between 2 and 1025 to provide the main output (OUT1) or it can be bypassed altogether by use of the DIV1 register bit. The value of N is stored in the N register.

The control registers are user-programmable through a 2-wire serial interface to determine operating frequency (values of P0, P1, and N) and modes of operation. The register values are stored in EEPROM and, therefore, only need to be programmed to alter frequencies and operating modes.

PIN DESCRIPTIONS

OUTPUT 1 (OUT1) – This pin is the main oscillator output; its frequency is determined by the control register settings for the prescaler P1 (mode bits 1M1 and 1M0) and divider N (DIV WORD).

OUTPUT 0 (OUT0) – A reference output, OUT0, is taken from the output of the reference-select MUX. Its frequency is determined by the control register settings for CTRL0 and values of prescaler P0 (mode bits 0M1 and 0M0). (See Table 1.)

CONTROL PIN 0 (CTRL0) – A multifunctional input pin that can be selected as a MUX select, output enable, and/or a power-down. The user-programmable control register values EN0, SEL0, and PDN0 determine its function. (See Table 1.)

TABLE 1

EN0 (BIT)	SEL0 (BIT)	PDN0 (BIT)	CTRL0 (PIN)	OUT0 (PIN)	CTRL0 FUNCTION	DEVICE MODE
0	0	0	1	Hi-Z (OUT1 and OUT2)	Power-Down*	Power-Down
			0	Hi-Z		Active
0	1	0	1	Master Clk/M	MUX Select	Active
			0	Master Clk		
1	0	0	1	Hi-Z	Output Enable	Active
			0	Master Clk		
1	1	0	1	Hi-Z	Output Enable	Active**
			0	Master Clk/M		
X	0	1	1	Hi-Z (OUT1 and OUT2)	Power-Down	Power-Down
			0	Master Clk		Active
X	1	1	1	Hi-Z	Power-Down	Power-Down
			0	Master Clk/M		Active

*This mode is for applications where OUT0 is not used, but CTRL0 is used as a device shutdown.
**Default Condition

CONTROL PIN 1 (CTRL1) – A multifunctional input pin that can be selected as an output enable and/or a power-down. Its function is determined by the user-programmable control register value of PDN1. (See Table 2.)

TABLE 2

PDN1 (BIT)	CTRL1 (PIN)	CTRL1 FUNCTION	OUT 1	DEVICE MODE
0	0	Output Enable	Out Clk	Active*
0	1	Output Enable	Hi-Z	Active*
1	0	Power-Down	Out Clk	Active
1	1	Power-Down	Hi-Z (OUT1 and OUT2)	Power-Down

*Default Condition

NOTE:

Both CTRL0 and CTRL1 can be configured as power-downs, they are internally "OR" connected so that either of the control pins may be used to provide a power-down function for the whole device, subject to appropriate settings of the PDN0 and PDN1 register bits. (See Table 3.)

TABLE 3

PDN0 (BIT)	PDN1 (BIT)	SHUTDOWN CONTROL
0	0	None*
0	1	CTRL1
1	0	CTRL0
1	1	CTRL0 or CTRL1

*CTRL0 performs a power-down if SEL0 and EN0 are both 0. (See Table 1.)

Serial Data Input/Output (SDA) – Input/output pin for the 2-wire serial interface used for data transfer.

Serial Clock Input (SCL) – Input pin for the 2-wire serial interface used to synchronize data movement on the serial interface.

REGISTER FUNCTIONS

The user-programmable registers can be programmed by the user to determine the mode of operation (MUX), operating frequency (DIV) and bus settings (BUS). Details of how these registers are programmed can be found in a later section; in this section the functions of the registers are described. The register setting are nonvolatile, the values are stored automatically or as required in EEPROM when the registers are programmed via the SDA and SCL pins.

MUX WORD

	MSB							LSB	MSB						LSB
Name	*	**PDN1**	**PDN0**	**SEL0**	**EN0**	**0M1**	**0M0**	**1M1**	**1M0**	**DIV1**	-	-	-	-	-	-
Default setting	0	0	0	1	1	0	0	0	0	0	x	x	x	x	x	x
						first data byte					second data byte					

*This bit must be set to zero.

DIV1 (bit)

This bit allows the output of the prescaler P1 to be routed directly to the OUT1 pin (DIV1 = 1). The N divider is bypassed so the programmed value of N is ignored. If DIV1 = 0 (default) the N divider functions normally.

0M1, 0M0, 1M1, 1M0 (bits)

These bits set the prescalers P0 and P1, to divide by 1, 2, 4, or 8. (See Table 4.)

TABLE 4

0M1	0M0	PRESCALER P0 DIVISOR "M"	1M1	1M0	PRESCALER P1 DIVISOR "M"
0	0	1*	0	0	1*
0	1	2	0	1	2
1	0	4	1	0	4
1	1	8	1	1	8

*Default Condition

EN0 (bit) (Default EN0 = 1)

If EN0 = 1 and PDN0 = 0, the CTRL0 pin functions as an output enable for OUT0, the frequency of the output is determined by the SEL0 bit.
If PDN0 = 1, the EN0 bit is ignored, CTRL0 will function as a power-down, output OUT0 will always be enabled on power-up, and its frequency is determined by the SEL0 bit.
If EN0 = 0, the function of CTRL0 is determined by the SEL0 and PDN0 bits. (See Table 1.)

SEL0 (Default SEL0 = 1)

If SEL0 = 1 and EN0 = PDN0 = 0, the CTRL0 pin determines the state of the MUX, (i.e., the output frequency of OUT0).
If CTRL0 = 0, the output will be the master clock frequency.
If CTRL0 = 1, the output will be the output frequency of the M prescaler.
If either EN0 or PDN0 = 1, then SEL0 determines the frequency of OUT0 when it is enabled.
If SEL0 = 0, the output will be the master clock frequency.
If SEL0 = 1, the output will be the output frequency of the M prescaler. (See Table 1.)

PDN0 (Default PDN0 = 0)

This bit (if set to 1) causes CTRL0 to perform a power-down function, regardless of the setting of the other bits.
If PDN0 = 0, the function of CTRL0 is determined by the values of EN0 and SEL0.

NOTE:

When EN0 = SEL0 = PDN0 = 0, CTRL0 also functions as a power-down. This is a special case where all the OUT0 circuitry is disabled even when the device is powered up. This feature can be used to save power when OUT0 is not used. (See Table 1.)

PDN1 (Default PDN1 = 0)

If PDN1 = 1, CTRL1 will function as a power-down.
If PDN1 = 0, CTRL1 functions as an output enable for OUT1 only. (See Table 2.)

NOTES (ON OUTPUT ENABLE AND POWER-DOWN):

1. Both enables are “smart” and wait for the output to be low before going to Hi-Z.
2. Power-down sequence first disables both outputs before powering down the device.
3. On power-up, the outputs are disabled until the clock has stabilized (~8000 cycles).
4. The device cannot be programmed in power-down mode.
5. A power-down command must persist for at least 2 cycles of the lowest output frequency plus 10µs.

DIV WORD

MSB							LSB	MSB							LSB
N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	X	X	X	X	X	X
first data byte								second data byte							

N

These ten bits determine the value of the programmable divider (N). The range of divisor values is from 2 to 1025, and is equal to the programmed value of N plus 2. (See Table 5.)

TABLE 5

BIT VALUE	DIVISOR (N)
0 000 000 000*	2
0 0 00 0 00 001	3
—	—
—	—
—	—
—	—
1 111 111 111	1025

*Default Condition

BUS WORD

NAME	—	—	—	—	WC	A2	A1	A0
Factory Default	0*	0*	0*	0*	0	0	0	0

*These bits are reserved and must be set to zero.

A0, A1, A2 (Default Setting = 000)

These are the device select bits that determine the address of the device.

WC (Default Setting WC = 0)

This bit determines when/if the EEPROM is written to after register contents have been changed.
If WC = 0, the EEPROM is automatically written after a write register command.
If WC = 1, the EEPROM is only written when the WRITE command is issued.
Regardless of the value of the WC bit, the value of the BUS register (A0, A1, and A2) is always immediately written to the EEPROM.

2-WIRE SERIAL DATA BUS

The DS1077L supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a “master.” The devices that are controlled by the master are “slaves.” The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1077L operates as a slave on the 2-wire bus. Connections to the bus are made via the open-drain I/O lines, SDA and SCL. A pullup resistor (5k) is connected to SDA.

The following bus protocol has been defined (see Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain high.

Start data transfer: A change in the state of the data line from high to low while the clock is high defines a START condition.

Stop data transfer: A change in the state of the data line from low to high while the clock line is high defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Within the bus specifications, a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The DS1077L works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. When the DS1077L EEPROM is being written to, it will not be able to perform additional responses. In this case, the slave DS1077L will send a ‘not acknowledge’ to any data transfer request made by the master. It will resume normal operation when the EEPROM operation is complete.

A master must signal an end-of-data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.

DATA TRANSFER ON 2-WIRE SERIAL BUS Figure 2

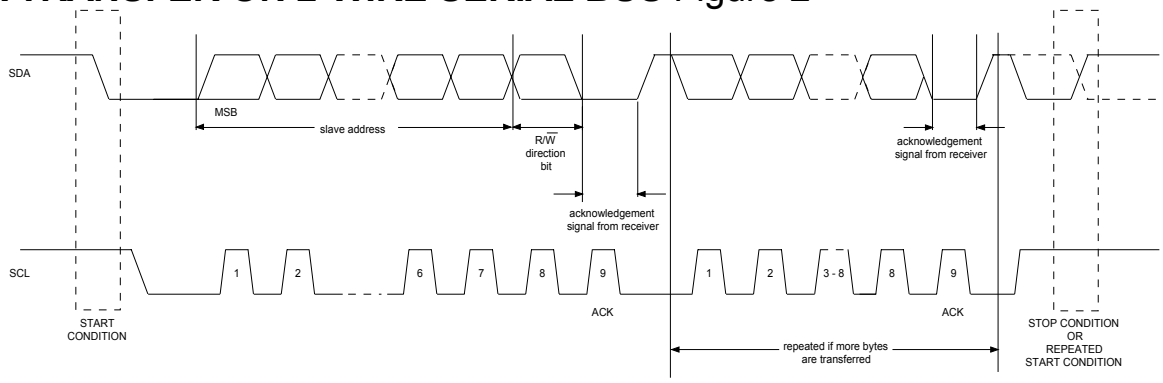


Figure 2 details how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1) **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next, follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

2) **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next, follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DS1077L can operate in the following two modes:

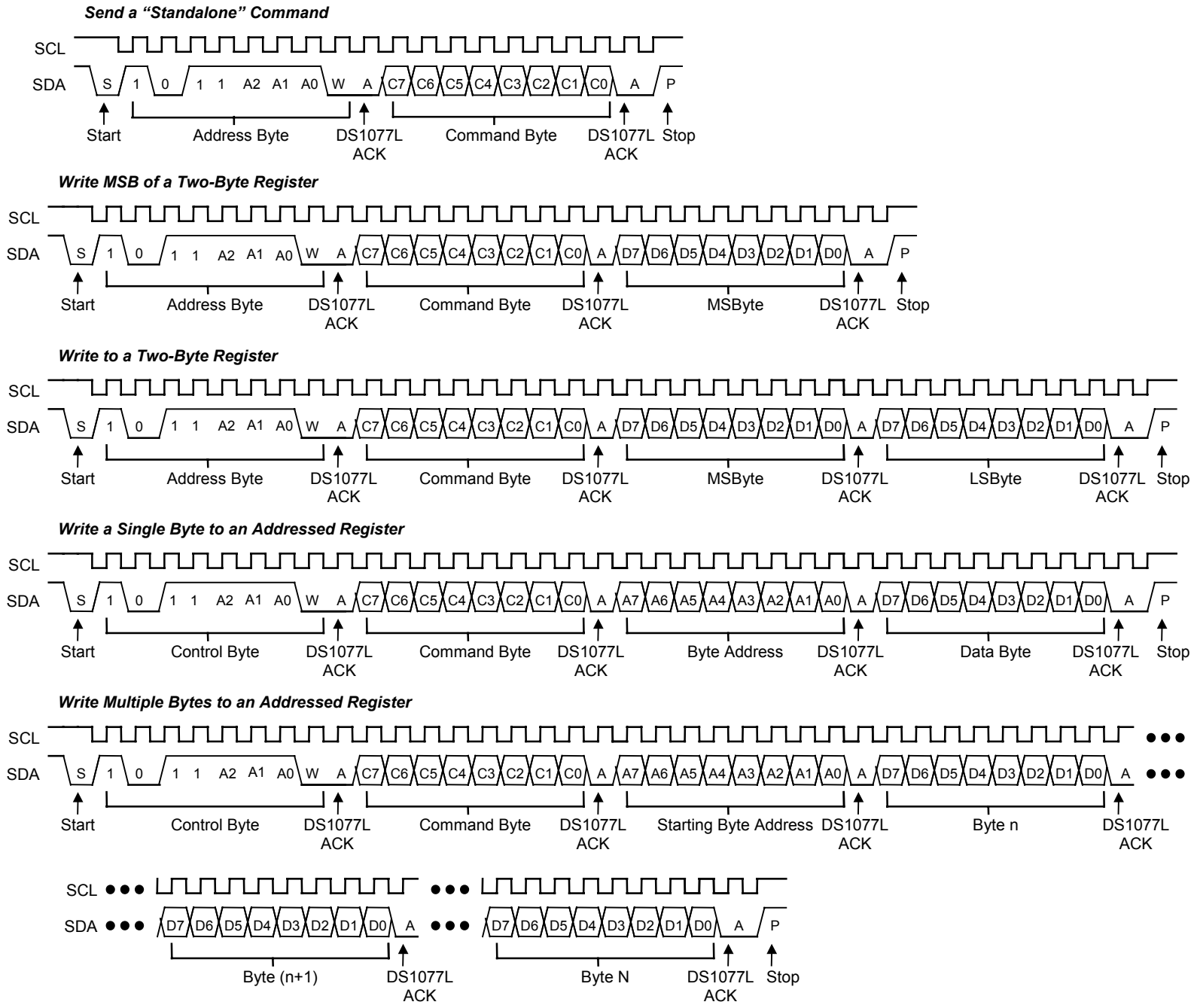
1) **Slave receiver mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

2) **Slave transmitter mode:** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1077L while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

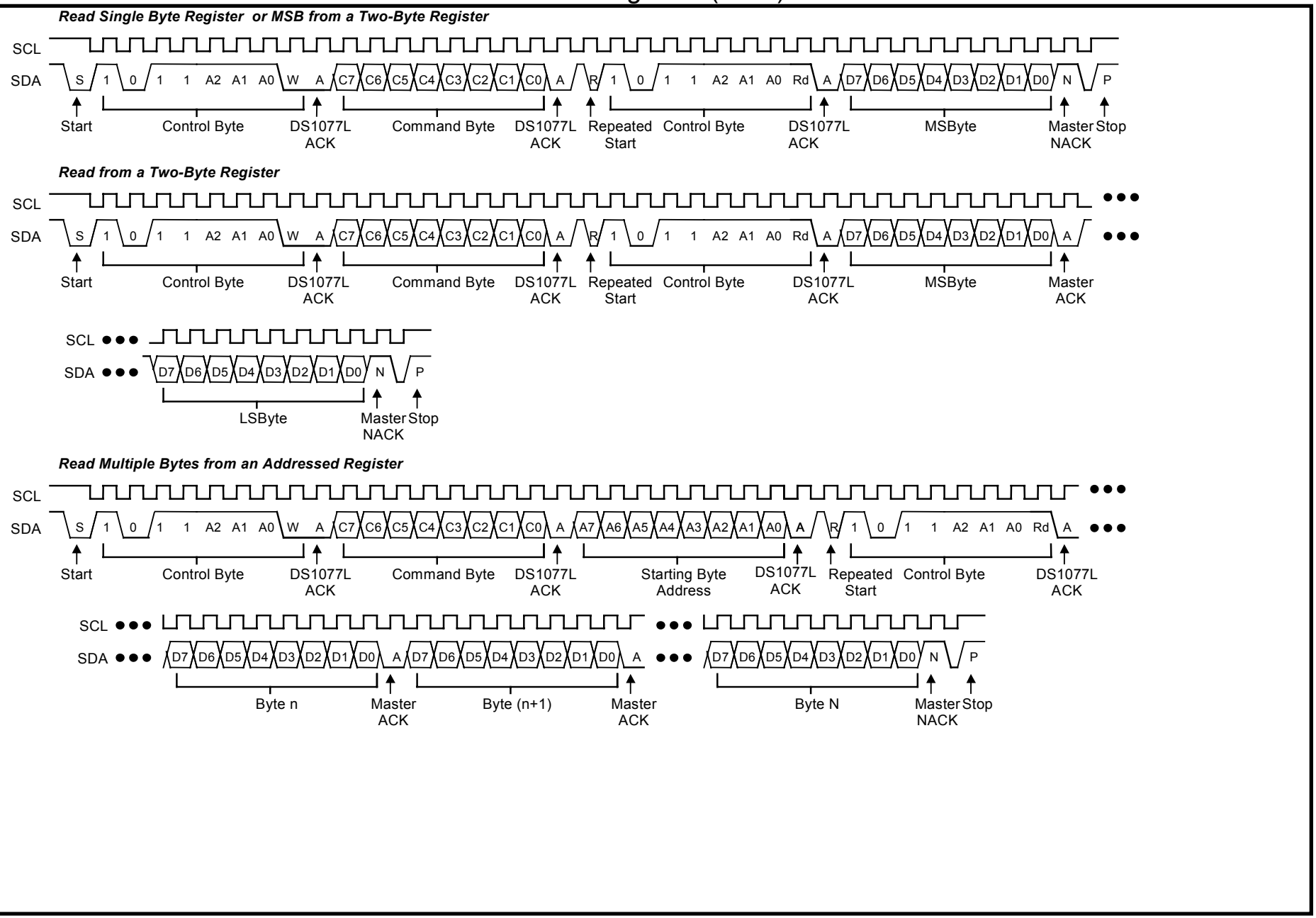
SLAVE ADDRESS

A control byte is the first byte received following the START condition from the master device. The control byte consists of a four-bit control code; for the DS1077L, this is set as 1011 binary for read and write operations. The next three bits of the control byte are the device select bits (A2, A1, and A0) and can be written to the EEPROM. They are used by the master device to select which of eight devices are to be accessed. The select bits are in effect the three least significant bits of the slave address. The last bit of the control byte (R/$\overline{W}$) defines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. Following the START condition, the DS1077L monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the 1011 code (changeable with one mask) and appropriate device select bits, the slave device outputs an acknowledge signal on the SDA line.

2-WIRE SERIAL COMMUNICATION WITH DS1077L Figure 3



2-WIRE SERIAL COMMUNICATION WITH DS1077L Figure 3 (cont.)



COMMAND SET

Data and control information is read from and written to the DS1077L in the format shown in Figure 3. To write to the DS1077L, the master will issue the slave address of the DS1077L and the R/$\overline{W}$ bit will be set to 0. After receiving an acknowledge, the bus master provides a command protocol. After receiving this protocol, the DS1077L will issue an acknowledge, and then the master can send data to the DS1077L. If the DS1077L is to be read, the master must send the command protocol as before, and then issue a repeat START condition and then the control byte again, this time with the R/$\overline{W}$ bit set to one to allow reading of the data from the DS1077L.

The command set for the DS1077L is as follows:

Access DIV [01]

If R/$\overline{W}$ = 0, this command writes to the DIV register. After issuing this command, the next data byte value is to be written into the DIV register.

If R/$\overline{W}$ = 1, the next data byte read is the value stored in the DIV register.

Access MUX [02]

If R/$\overline{W}$ = 0, this command writes to the MUX register. After issuing this command, the next data byte value is to be written into the MUX register.

If R/$\overline{W}$ = 1, the next data byte read is the value stored in the MUX register.

Access BUS [0D]

If R/$\overline{W}$ = 0, this command writes to the BUS register. After issuing this command, the next data byte value is to be written into the BUS register.

If R/$\overline{W}$ = 1, the next data byte read is the value stored in the BUS register.

Write E2 [3F]

If WC = 0, the EEPROM is automatically written to at the end of each command, this is a DEFAULT condition. In this case the command WRITE E2 is not needed

If WC = 1, the EEPROM is only written when the WRITE E2 command is issued. On receipt of the WRITE E2 command the contents of the DIV and MUX registers are written into the EEPROM, thus locking in the register settings.

EXCEPTION: The BUS register is always automatically written to EEPROM after a write, regardless of the value of WC.

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Ground -0.5V to 6.0V
Operating Temperature Range 0°C to +70°C
Storage Temperature Range -55°C to 125°C
Soldering Temperature See J-STD-020A Specification

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 2.7V to 3.6V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		2.7		3.6	V	1
High-Level Output Voltage (OUT1, OUT0)	V_{OH}	I_{OH} = -4mA, V_{CC} = MIN	2.4			V	
Low-Level Output Voltage (OUT1, OUT0)	V_{OL}	I_{OL} = 4mA			0.4	V	
High-Level Input Voltage	V_{IH}	SDA and SCL CTRL0 and CTRL1	$0.7V_{CC}$ 1.4		V_{CC} + 0.3	V	
Low-Level Input Voltage	V_{IL}	SDA and SCL CTRL0 and CTRL1	V_{CC} - 0.3		$0.3V_{CC}$ 0.6	V	
High-Level Input Current (CTRL1, CTRL0, SDA, SCL)	I_{IH}	$V_{IH} = V_{CC}$ = 3.6V			1	µA	
Low-Level Input Current (CTRL1, CTRL0, SDA, SCL)	I_{IL}	V_{CC} = 3.6V, V_{IL} = 0	-1			µA	
Supply Current (Active) DS1077L-66 DS1077L-60 DS1077L-50 DS1077L-40	I_{CC}	C_L = 15pF (both outputs)			 30 25 20 15	mA	
Standby Current (Power-Down)	I_{CCQ}	Power-Down Mode		1	5	µA	

AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 2.7V to 3.6V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Output Frequency Tolerance (from Nominal)	Δf_O	V_{CC} = 3.3V T_A = +25°C	-0.5	0	+0.5	%	
Combined Freq. Variation (from Nominal)	Δf_O	Over temp & voltage	-1.25		+1.25	%	
Output Frequency Min Output Frequency Max	f_{OUT}		4.87		66.66	kHz MHz	2
Power-Up Time	t_{POR} + t_{STAB}			0.1	1	ms	4
Enable OUT1 from CTRL1	t_{STAB}			0.1	1	ms	
Enable OUT0 from CTRL0	t_{STAB}			0.1	1	ms	
OUT1 Hi-Z from CTRL1	t_{STAB}				1	ms	
OUT0 Hi-Z from CTRL0	t_{STAB}				1	ms	
Load Capacitance	C_L			15	50	pF	3
Output Duty Cycle (OUT1, OUT0)			40		60	%	
Output Jitter		F_{OUT} = 66MHz M = 1; DIV1 =1 C_L = 12pF 3 sigma pk-to-pk		50		psec	9

AC ELECTRICAL CHARACTERISTICS: 2-WIRE INTERFACE

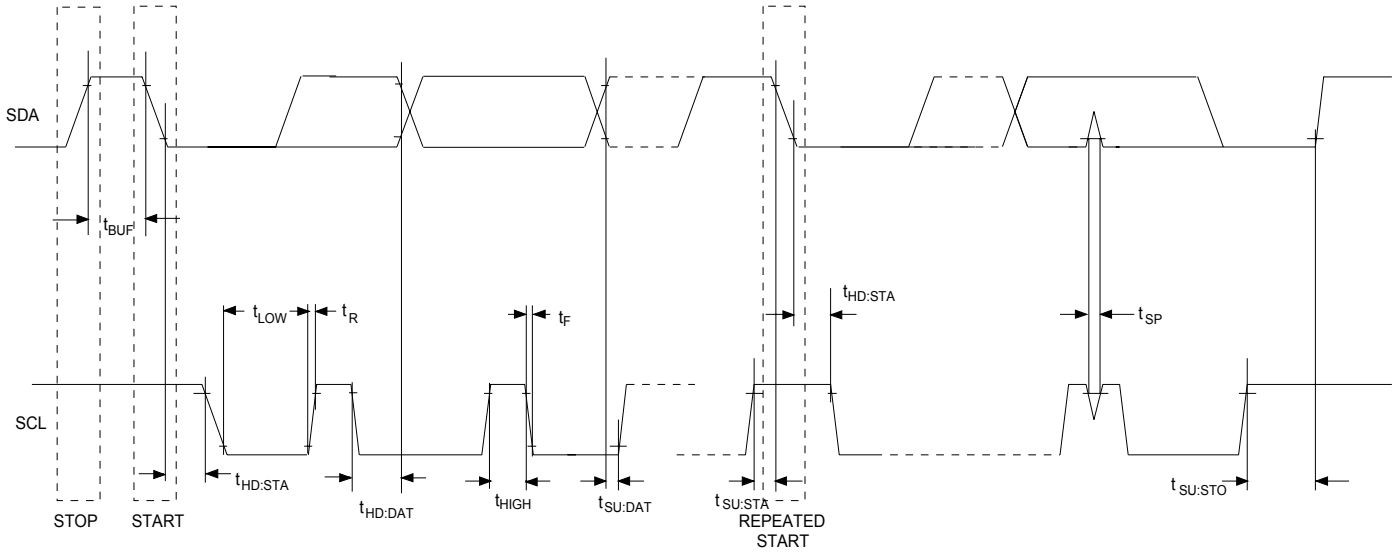
(0°C to +70°C, V_{CC} = 2.7V to 3.6V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	f_{SCL}	Fast Mode			400	kHz	
		Standard Mode			100		
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast Mode	1.3			µs	
		Standard Mode	4.7				
Hold Time (Repeated) START Condition.	$t_{HD:STA}$	Fast Mode	0.6			µs	5
		Standard Mode	4.0				
LOW Period of SCL	t_{LOW}	Fast Mode	1.3			µs	
		Standard Mode	4.7				
HIGH Period of SCL	t_{HIGH}	Fast Mode	0.6			µs	
		Standard Mode	4.0				
Setup Time for a Repeated START	$t_{SU:STA}$	Fast Mode	0.6			µs	
		Standard Mode	4.7				
Data Hold Time	$t_{HD:DAT}$	Fast Mode	0		0.9	µs	6, 7
		Standard Mode	0				
Data Setup Time	$t_{SU:DAT}$	Fast Mode	100			ns	
		Standard Mode	250				
Rise Time of Both SDA and SCL Signals	t_R	Fast Mode	$20 + 0.1C_B$		300	ns	8
		Standard Mode			1000		
Fall Time of Both SDA and SCL Signals	t_F	Fast Mode	$20 + 0.1C_B$		300	ns	8
		Standard Mode					
Setup Time for STOP	$t_{SU:STO}$	Fast Mode	0.6			µs	
		Standard Mode	4.0				
Capacitive Load for Each Bus Line	C_B				400	pF	8
Input Capacitance	C_I			5		pF	

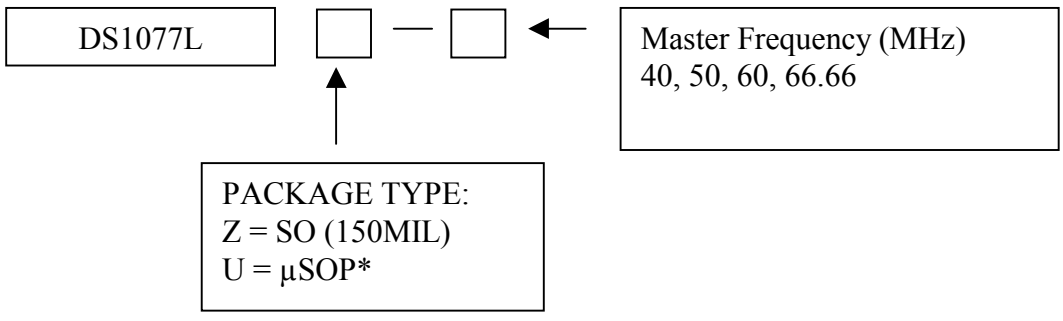
NOTES:

1. All voltages are referenced to ground.
2. 4.87kHz is obtained from a -40MHz standard part.
3. Output voltage swings may be impaired at high frequencies combined with high output loading.
4. After this period, the first clock pulse is generated.
5. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH\ MIN}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
6. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
7. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R\ MAX} + t_{SU:DAT} = 1000 + 250 = 1250ns$ before the SCL line is released.
8. C_B — Total capacitance of one bus line in pF.
9. Jitter accumulates over N clock cycles as: (3 sigma jitter)(no. of cycles)$^{0.65}$.

TIMING DIAGRAM



ORDERING INFORMATION:

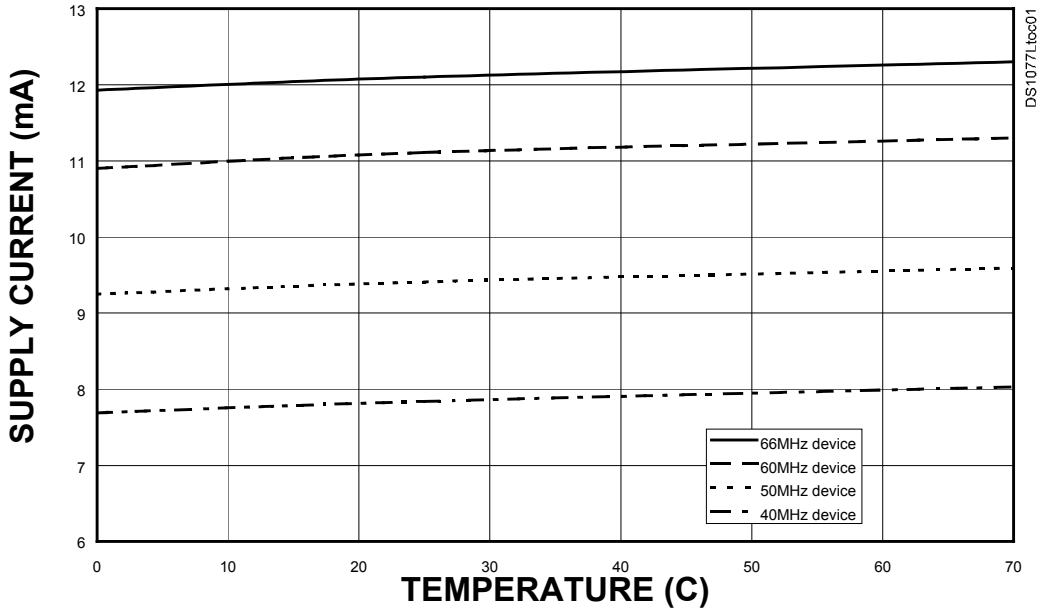


**Future product. Contact factory for availability.*

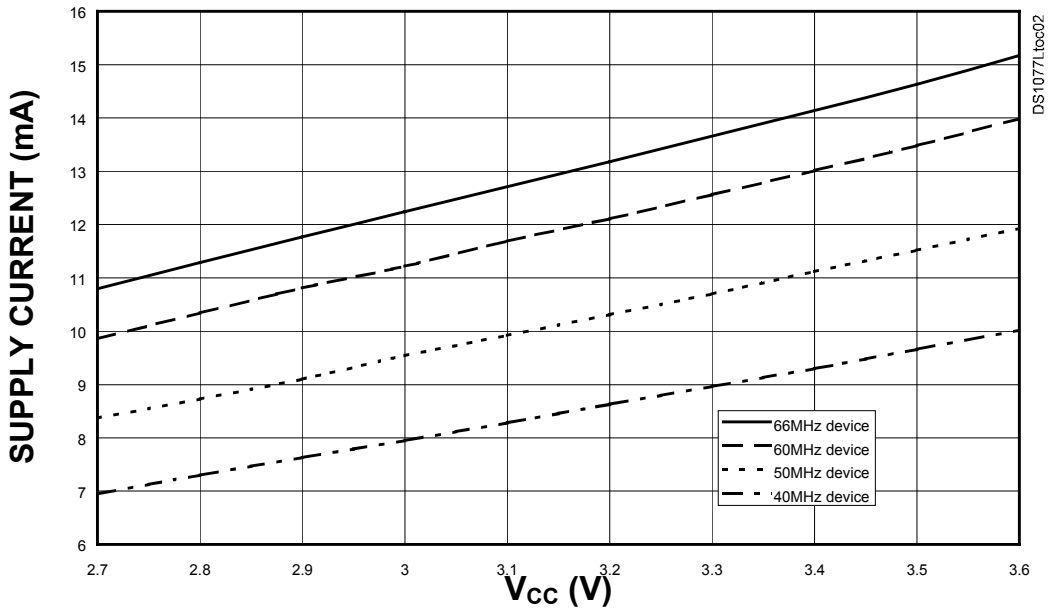
TYPICAL OPERATING CHARACTERISTICS

(V_{CC} = 3.3V, T_A = +25ºC, unless otherwise specified)

SUPPLY CURRENT vs. TEMPERATURE



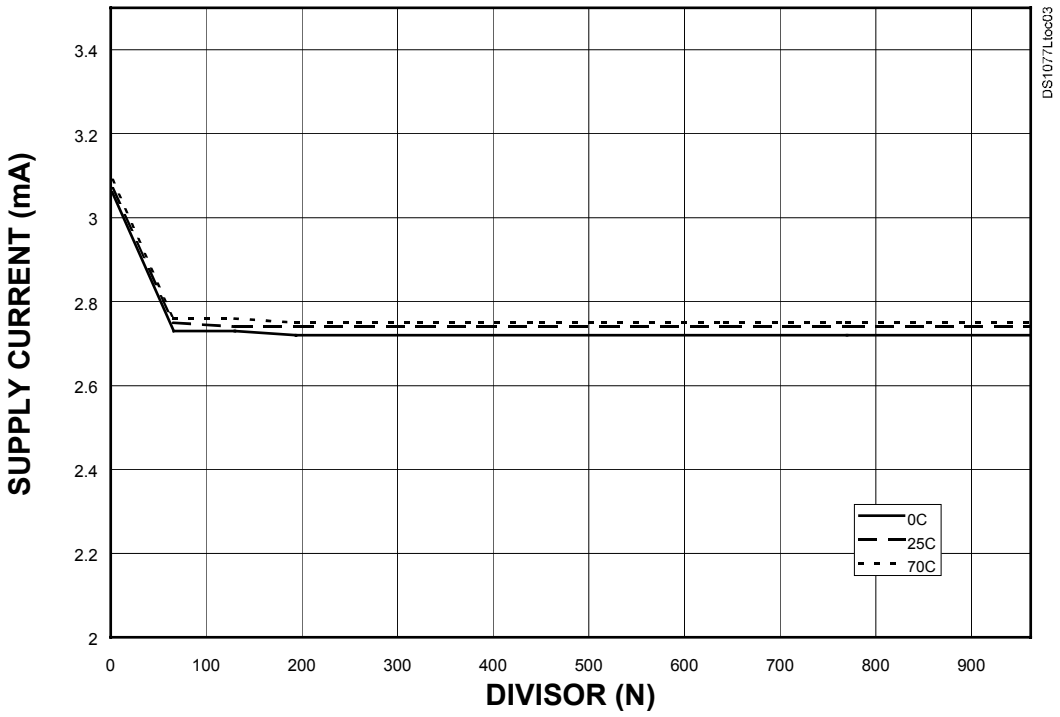
SUPPLY CURRENT vs. VOLTAGE



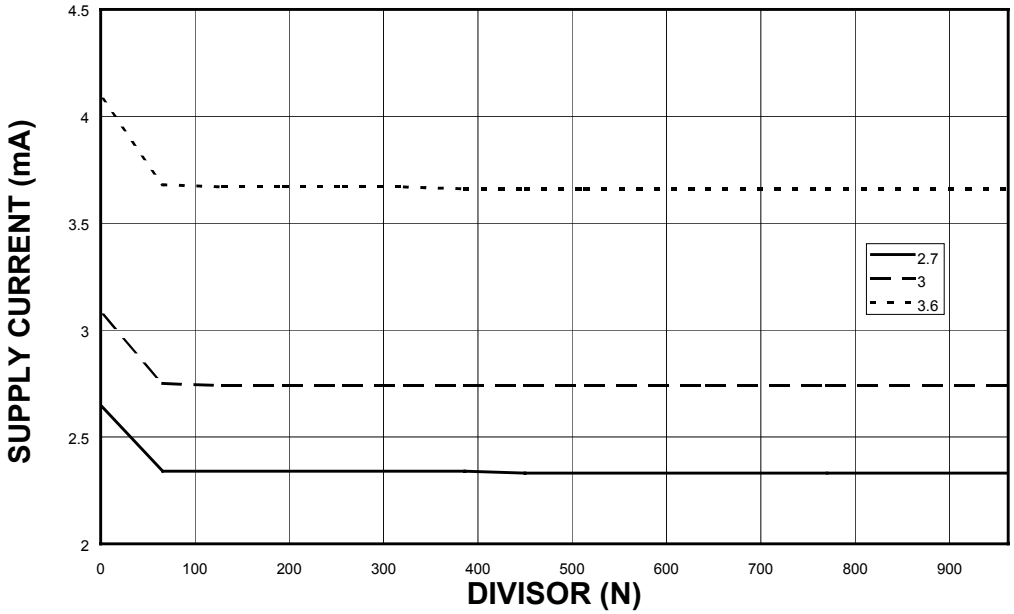
TYPICAL OPERATING CHARACTERISTICS (cont.)

(V_{CC} = 3.3V, T_A = +25ºC, unless otherwise specified)

SUPPLY CURRENT vs. DIVISOR (FREQUENCY)



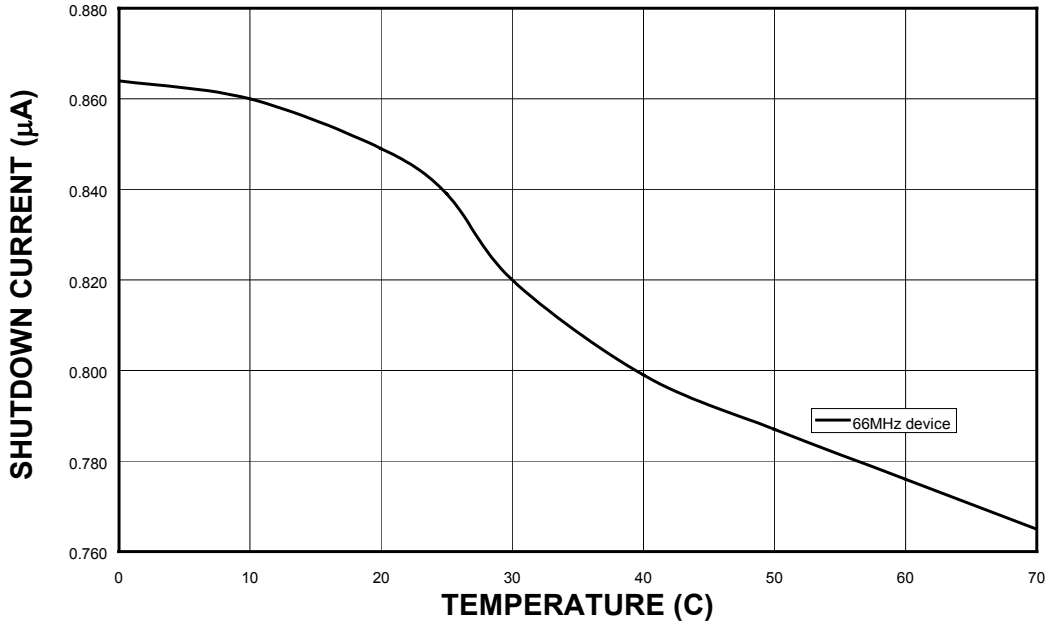
SUPPLY CURRENT vs. DIVISOR (FREQUENCY)



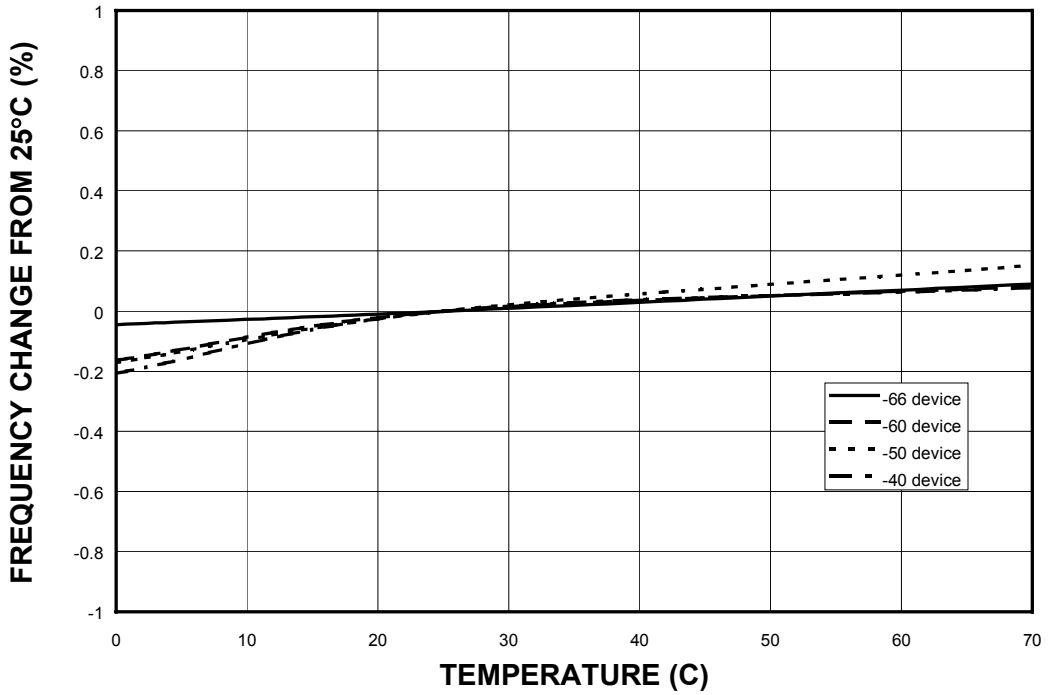
TYPICAL OPERATING CHARACTERISTICS (cont.)

(V_{CC} = 3.3V, T_A = +25ºC, unless otherwise specified)

DS1077L SHUTDOWN CURRENT vs. TEMPERATURE



DS1077L TEMPCO



TYPICAL OPERATING CHARACTERISTICS (cont.)

(V_{CC} = 3.3V, T_A = +25ºC, unless otherwise specified)