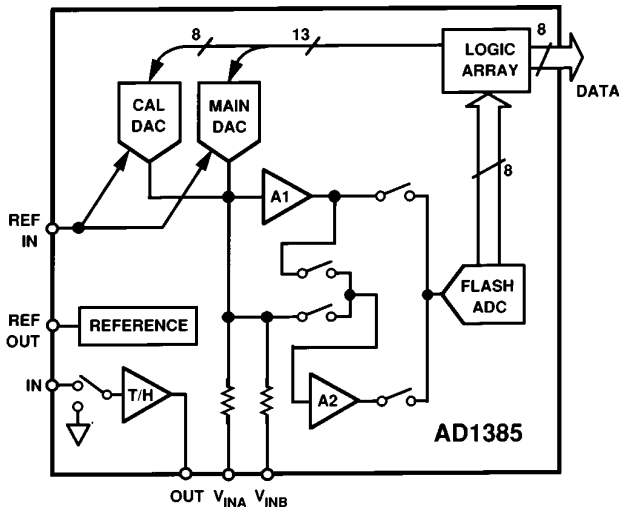
16-Bit 500 kHz Wide Temperature Range Sampling ADC

AD1385

FEATURES
16-Bit Resolution
500 kHz Sampling Rate
Differential Linearity Autocalibration
Specified over –55°C to +125°C Range
SNR 90 dB @ 100 kHz (min)
THD –88 dB @ 100 kHz (min)
0.0006% FSR DNL (typ)
0.0015% FSR INL (typ)
No Missing Codes
±5, ±10 V Bipolar Input Ranges
Zero Offset Autocalibration

APPLICATIONS
Medical Imaging
CAT
Magnetic Resonance
Radar
Vibration Analysis
Parametric Measurement Unit (ATE)
Digital Storage Oscilloscopes
Waveform Recorders
Analytical Instruments

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1385 is a complete 500 kHz, 16-bit, sampling analog-to-digital converter contained in a single package. Its differential linearity autocalibration feature allows this high resolution, high speed converter to offer outstanding noise and distortion performance, as well as excellent INL and DNL specifications, over the full military temperature range. Autocalibration effectively eliminates DNL drift over temperature.

The AD1385 architecture includes a low noise, low distortion track/hold, a three pass digitally corrected subranging ADC, and linearity calibration circuitry. A complete linearity calibration requires only 15 ms. Precision thin-film resistors and a proprietary DAC contribute to the part's outstanding dynamic and static performance.

The AD1385 uses four power supplies, ±5 V and ±15 V, and an external 10 MHz clock. Power dissipation is nominally 2.76 W. Two user selectable bipolar input ranges, ±5 V and ±10 V, are provided. Careful attention to grounding and a single package make it easy to design PCBs to achieve specified performance.

The AD1385's pinout is nearly identical to that of the AD1382, a factory calibrated 16-bit, 500 kHz SADC. Just two additional connections, to enable and monitor autocalibration, are required. This commonality provides an easy upgrade path to extend system performance and operating temperature range.

REV. 0

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AD1385—SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, V_{DD} = +5 V, V_{SS} = –5 V, 10 MHz External Clock, unless otherwise noted)

Parameter	AD1385KD Min	AD1385KD Typ	AD1385KD Max	AD1385TD Min	AD1385TD Typ	AD1385TD Max	Units
RESOLUTION	16			16			Bits
ANALOG INPUT							
Input Ranges		±5, ±10			±5, ±10		V
Input Impedance	2.45	2.5	2.55	2.45	2.5	2.55	kΩ
TRANSFER CHARACTERISTICS (Combined ADC/Track/Hold)							
Integral Nonlinearity[1, 2], T_{MIN} to T_{MAX}		±0.0015			±0.0015		% FSR[3]
Differential Nonlinearity[1]		±0.0006	±0.0015		±0.0006	±0.0015	% FSR
Drift, T_{MIN} to T_{MAX}		0.3			0.3		ppm/°C
Missing Codes, T_{MIN} to T_{MAX}			None			None	
Gain Error[4]		±0.05	±0.15		±0.05	±0.15	% FSR
Drift, T_{MIN} to T_{MAX}		8	15		8	15	ppm/°C
Bipolar Zero[4]		±0.05	±0.10		±0.05	±0.10	% FSR
Drift, T_{MIN} to T_{MAX}		5	15		5	15	ppm/°C
PSRR		±0.006	±0.10		±0.006	±0.10	% FSR/V
Noise		70			70		µV rms
DYNAMIC CHARACTERISTICS[2] ±5 V FSR, V_{IN} = –0.4 dB, T_{MIN} to T_{MAX}							
Sample Rate			500			500	kHz
Signal-to-Noise Ratio[5]							
f = 5 kHz	90	93		90	93		dB
f = 100 kHz	90	92		90	92		dB
f = 200 kHz	88	91		88	91		dB
Peak Distortion							
f = 5 kHz	–90	–107		–90	–107		dB
f = 100 kHz	–88	–95		–88	–95		dB
f = 200 kHz	–82	–88		–82	–88		dB
Total Harmonic Distortion[6]							
f = 5 kHz	–90	–105		–90	–105		dB
f = 100 kHz	–88	–95		–88	–95		dB
f = 200 kHz	–82	–88		–82	–88		dB
DYNAMIC CHARACTERISTICS[2] ±10 V FSR, V_{IN} = –0.4 dB, T_{MIN} to T_{MAX}							
Sample Rate			500			500	kHz
Signal-to-Noise Ratio[5]							
f = 5 kHz	90	95		90	95		dB
f = 100 kHz	90	94		90	94		dB
f = 200 kHz	88	93		88	93		dB
Peak Distortion							
f = 5 kHz	–90	–108		–90	–108		dB
f = 100 kHz	–80	–87		–80	–87		dB
f = 200 kHz	–74	–82		–74	–82		dB
Total Harmonic Distortion[6]							
f = 5 kHz	–90	–105		–90	–105		dB
f = 100 kHz	–80	–87		–80	–87		dB
f = 200 kHz	–74	–82		–74	–82		dB
DIGITAL INPUTS							
Input Voltage							
V_{IL}			0.8			0.8	V
V_{IH}	2.25			2.25			V
Input Current			±200			±200	µA
Input Capacitance		2			2		pF
Clock							
Frequency		2.5–10			2.5–10		MHz
Duty Cycle		40-60			40-60		%
Aperture Delay[7]		7			7		ns
DIGITAL OUTPUTS							
Output Voltage							
V_{OL} @ I_{OL} = 3.2 mA		0.2	0.4		0.2	0.4	V
V_{OH} @ I_{OH} = –3.2 mA	2.4	4.5		2.4	4.5		V
Output Capacitance		4			4		pF
Leakage, Outputs Disabled			±200			±200	µA

Parameter	AD1385KD Min	AD1385KD Typ	AD1385KD Max	AD1385TD Min	AD1385TD Typ	AD1385TD Max	Units
OUTPUT CODING	Complementary Offset Binary or Complementary Twos Complement						
INTERNAL REFERENCE							
Voltage	9.990		10.010	9.990		10.010	V
Current	2	5		2	5		mA
Drift		5	15		5	15	ppm/°C
TEMPERATURE RANGE, CASE							
Specified	0		+70	–55		+125	°C
Storage	–65		+150	–65		+150	°C
POWER REQUIREMENTS							
Specified Operating Range							
$\pm V_S$	14.25		15.75	14.25		15.75	V
$+V_{DD}$	4.75		5.25	4.75		5.25	V
$-V_{SS}$	–5.25		–4.75	–5.25		–4.75	V
Current Drains							
$+V_S$		52	80		52	80	mA
$-V_S$		48	75		48	75	mA
$+V_{DD}$		104	160		104	160	mA
$-V_{SS}$		148	200		148	200	mA
Power Dissipation		2.76	4.125		2.76	4.125	Watts

NOTES
[1]Integral linearity is inferred from FFTs. Differential linearity is derived from histograms.
[2]Performance over temperature is specified at the temperature at which the last calibration was performed.
[3]FSR = Full-Scale Range.
[4]Adjustable to zero.
[5]SNR excludes harmonics 2-9 of the fundamental.
[6]THD includes harmonics 2-9 of the fundamental.
[7]Aperture delay is the time from the rising edge on the Hold Command Input to the opening of the switch in the Track/Hold.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1, 2] (T_A = –55°C to +125°C, V_S = ±15 V, V_{DD} = +5 V, V_{SS} = –5 V)

Parameter	Design Minimum	Typ	Unit	Description
START COMMAND				
t_{SCS}	10		ns	Setup Time
t_{SCH}	10		ns	Hold Time
AUTOZERO				
t_{AZS}	10		ns	Setup Time
t_{AZH}	20		ns	Hold Time
DATA VALID				
t_{DVS}		1.5	CP[3]	Setup Time
t_{DVH}		0.5	CP[3]	Hold Time
HOLD COMMAND				
t_H		13	CP[3]	Hold Time
t_D		7	ns	Delay Time
DATA STROBE				
t_{DS}		2	CP[3]	Pulse Width
t_{DSD}		16.5	CP[3]	Delay
CALIBRATE PULSE WIDTH	20		ns	
CALIBRATION STATUS		15	ms	Duration

NOTES
[1]Refer to Figures 17, 18 and 24.
[2]Design minimums are derived from worst case design analysis and/or simulation results. Typical values are based on characterization data. These specifications are not guaranteed or tested.
[3]The time duration for this parameter varies in direct proportion to the width of the Clock Pulse (CP).

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to AGND . . . . . 18 V
$-V_S$ to AGND . . . . . –18 V
V_{DD} to PGND . . . . . 7 V
V_{SS} to PGND . . . . . –7 V
AGND to PGND . . . . . ±0.3 V
Analog Inputs . . . . . $\pm V_S$
Reference Input . . . . . 0 V to +11 V
Digital Inputs . . . . . –0.3 V to V_{DD} + 0.3 V
Output Short Circuit Duration
  Reference Output . . . . . Indefinite
  Track/Hold Output . . . . . 1 sec
  Digital Outputs . . . . . 1 sec for Any One Output
Case Temperature (Operating) . . . . . –55°C to +125°C
Storage Temperature . . . . . –65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range (Case)	Package Option*
AD1385KD	0°C to +70°C	DH-48A
AD1385TD	–55°C to +125°C	DH-48A
AD1385TD/883B	–55°C to +125°C	DH-48A

*DH-48A = Bottom Brazed Ceramic DIP.

AD1385 PIN CONNECTIONS

The AD1385 is housed in a 48-pin bottom-brazed ceramic bathtub package. The pinout is as follows:

Pin	Function	Pin	Function
1	CLOCK IN	48	V_{DD2} (+5 V POWER)
2	POWER GROUND	47	POWER GROUND
3	B1/B9 (MSB)	46	V_{SS2} (–5 V POWER)
4	B2/B10	45	AUTOZERO
5	B3/B11	44	B1 SELECT
6	B4/B12	43	POWER GROUND
7	B5/B13	42	POWER GROUND
8	B6/B14	41	$\overline{\text{CAL}}$
9	B7/B15	40	GAIN ADJUST
10	B8/B16 (LSB)	39	+10 V REFERENCE OUT
11	V_{DD1} (+5 V SIGNAL)	38	$-V_{S1}$ (–15 V)
12	POWER GROUND	37	SIGNAL GROUND
13	V_{SS1} (–5 V SIGNAL)	36	$+V_{S1}$ (+15 V)
14	SIGNAL GROUND	35	SIGNAL GROUND
15	DATA STROBE	34	DNC
16	HI/LO BYTE SELECT	33	DNC
17	$\overline{\text{OE}}$ DATA ENABLE	32	+10 V REFERENCE IN
18	START CONVERT	31	V_{IN} B
19	HOLD COMMAND OUT	30	V_{IN} A
20	SIGNAL GROUND	29	OFFSET ADJUST
21	$+V_{S2}$ (+15 V)	28	CAL STATUS
22	HOLD COMMAND IN	27	TRACK/HOLD OUTPUT
23	$-V_{S2}$ (–15 V)	26	SIGNAL GROUND
24	POWER GROUND	25	TRACK/HOLD INPUT

DNC = DO NOT CONNECT.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1385 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



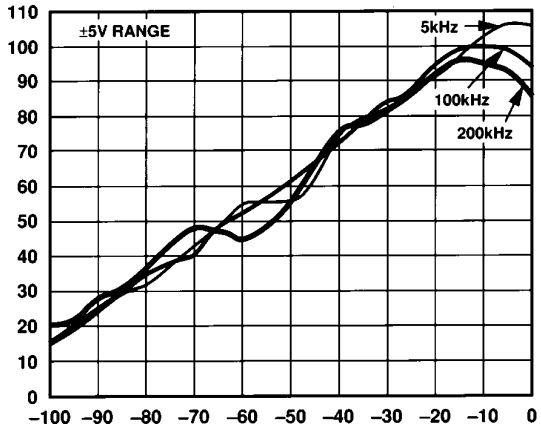


Figure 1. Spurious-Free Range vs. Input Amplitude, ±5 V Range, 2048-Point FFT, 500 kHz Sample Rate

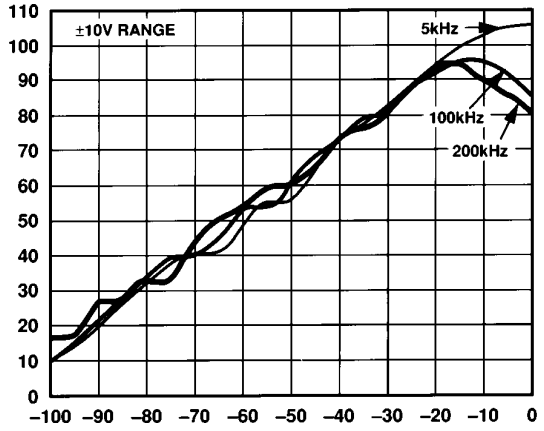


Figure 2. Spurious-Free Range vs. Input Amplitude, ±10 V Range, 2048-Point FFT, 500 kHz Sample Rate

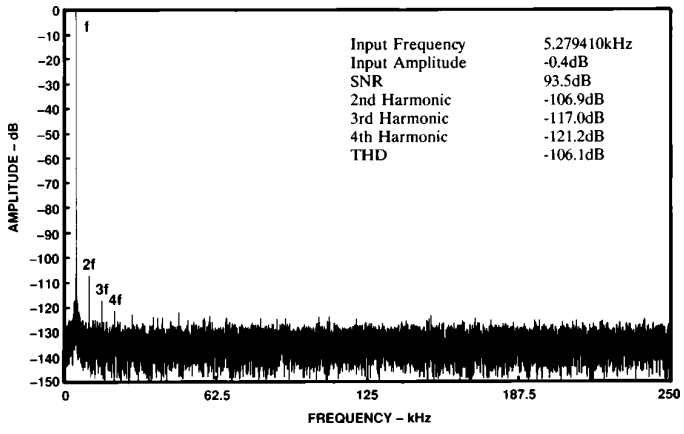


Figure 3. Full-Scale Sine Wave Power Spectral Density, ±5 V Range, 16384-Point FFT, 500 kHz Sample Rate

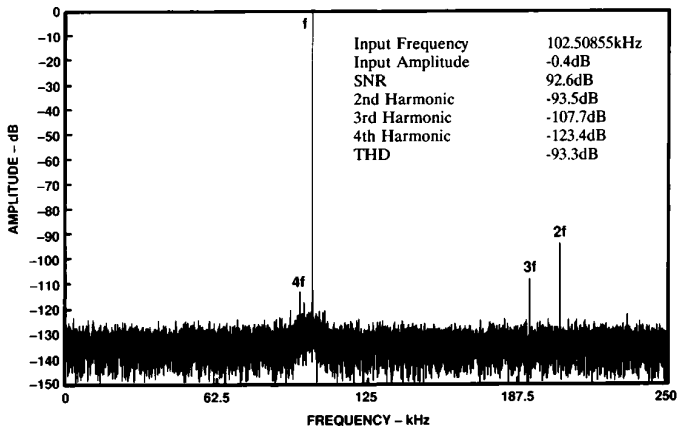


Figure 4. Full-Scale Sine Wave Power Spectral Density, ±5 V Range, 16384-Point FFT, 500 kHz Sample Rate

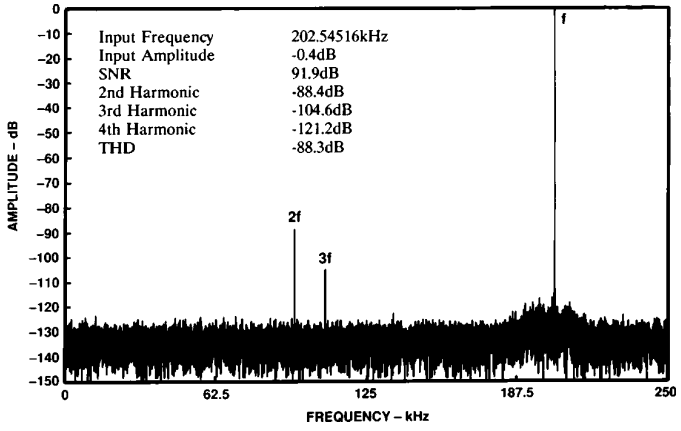


Figure 5. Full-Scale Sine Wave Power Spectral Density, ±5 V Range, 16384-Point FFT, 500 kHz Sample Rate

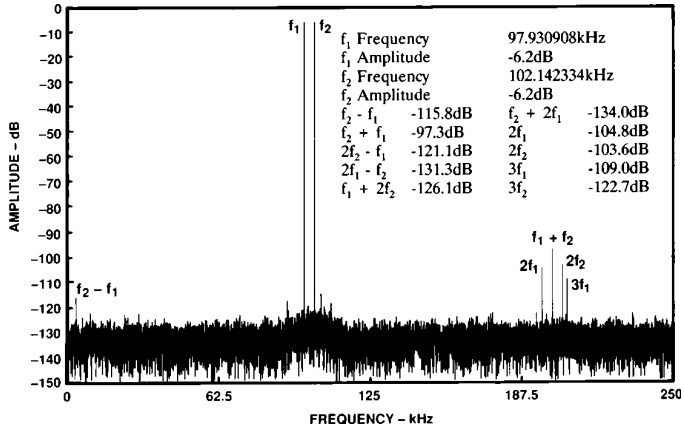


Figure 6. 100 kHz Intermodulation Performance, ±5 V Range, 16384-Point FFT, 500 kHz Sample Rate

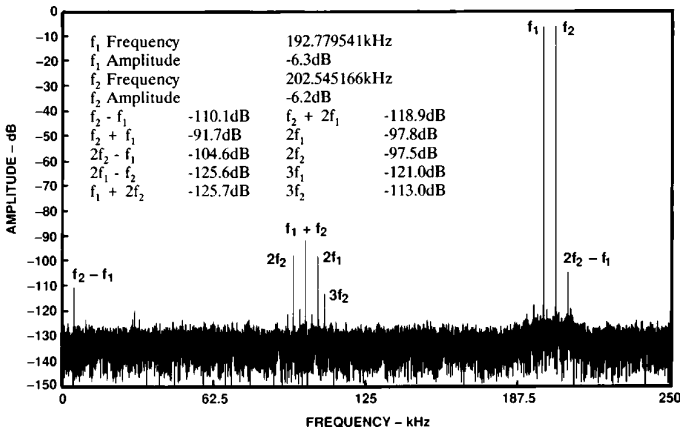


Figure 7. 200 kHz Intermodulation Performance, ±5 V Range, 16384-Point FFT, 500 kHz Sample Rate

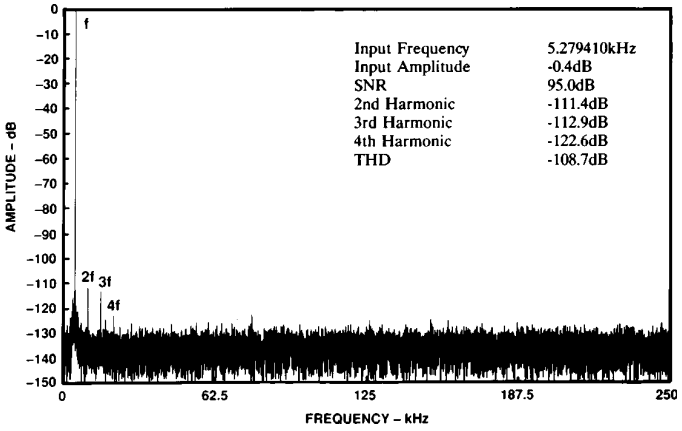


Figure 8. Full-Scale Sine Wave Power Spectral Density, ±10 V Range, 16384-Point FFT, 500 kHz Sample Rate

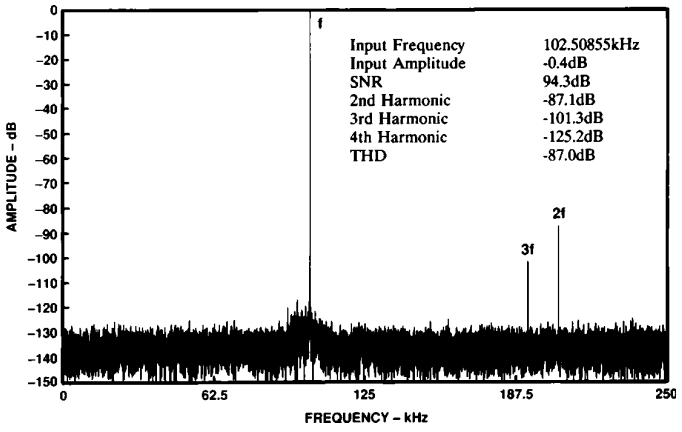


Figure 9. Full-Scale Sine Wave Power Spectral Density, ±10 V Range, 16384-Point FFT, 500 kHz Sample Rate

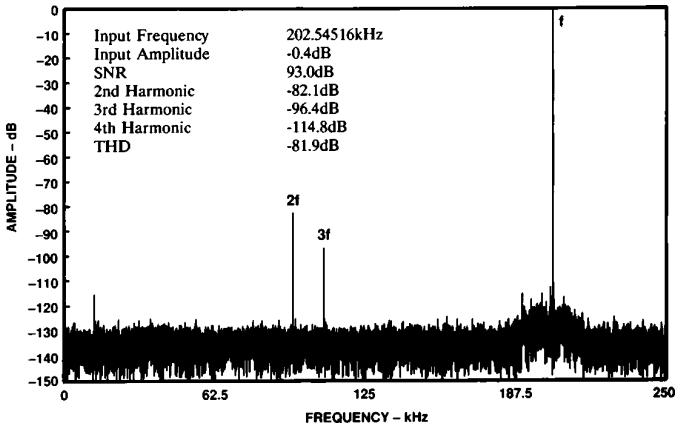


Figure 10. Full-Scale Sine Wave Power Spectral Density, ±10 V Range, 16384-Point FFT, 500 kHz Sample Rate

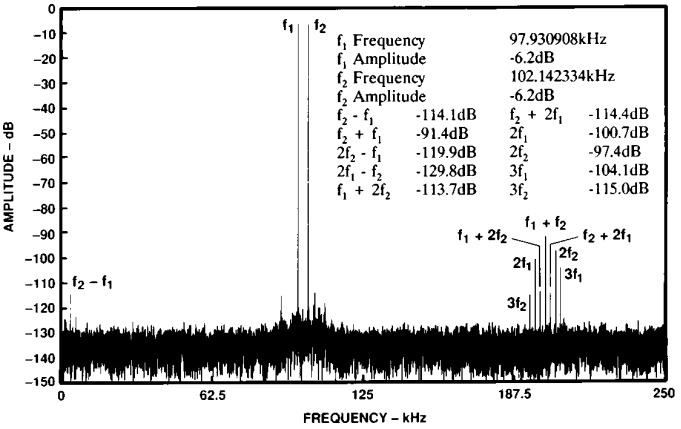


Figure 11. 100 kHz Intermodulation Performance, ±10 V Range, 16384-Point FFT, 500 kHz Sample Rate

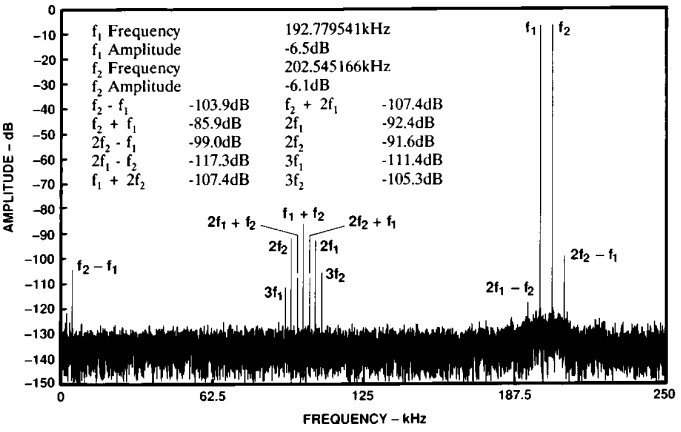


Figure 12. 200 kHz Intermodulation Performance, ±10 V Range, 16384-Point FFT, 500 kHz Sample Rate

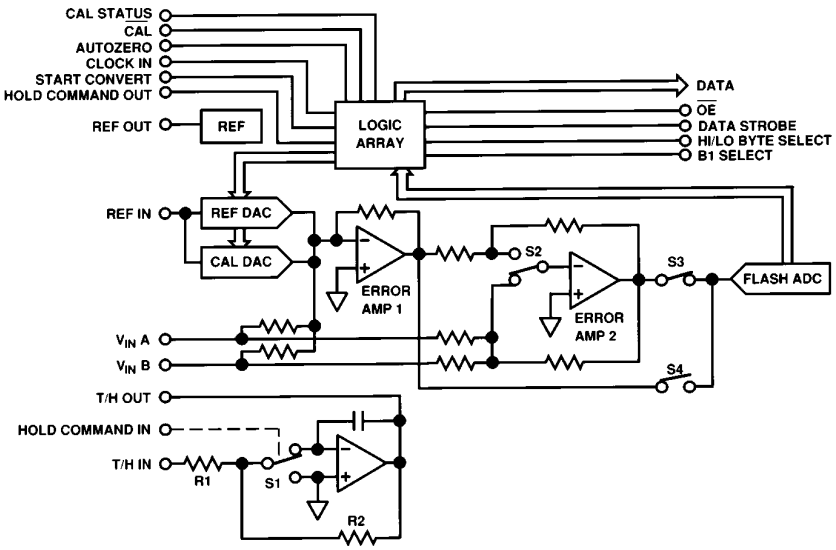


Figure 13. AD1385 Functional Block Diagram

THEORY OF OPERATION

The AD1385 performs conversions using a three-pass subranging technique. This proven circuit concept, implemented with state of the art components, allows the ADC, track-hold, and a low noise reference to fit into a single hermetic package, simplifying the task of board design. The T/H and ADC portions of the AD1385 are distinct circuits with inputs and outputs available on separate pins. This functional division allows greatest application flexibility. The AD1385's major functional blocks are shown in Figure 13.

The T/H uses a low noise high performance hybrid amplifier and high speed analog switches to achieve precision performance. It operates as an inverting amplifier during Track mode. Summing junction switch S1 disconnects the analog input to place the circuit into Hold mode; the amplifier's output stays constant because the dc path to its inverting input is broken. S1 also grounds the junction of R1 and R2 to minimize signal feedthrough. Pedestal is independent of the analog input level because all switching is done near ground. This ensures very low nonlinearity and distortion.

A precision Reference DAC and an 8-bit flash ADC form the heart of the AD1385's subranging design. High speed amplifiers combine the analog input and DAC output to produce the voltages encoded by the flash ADC during each pass. A logic array provides all necessary timing, control, and computation.

The first rising clock edge after Start Convert goes high begins the conversion (provided the previous conversion is complete). The Hold Command goes high and switches the T/H into hold. The held signal from the T/H goes through S2, S3, and Error Amp 2 to the flash ADC. During this pass Error Amp 2 actually attenuates the ADC input to keep the voltage within the flash ADC's input range. The flash ADC is strobed after a 100 ns settling period. The 8-bit result is saved in the logic array and is routed to the MSBs of the Reference DAC.

Error Amp 1 amplifies the difference between the Reference DAC output and the held input signal during the second pass. S4 routes this error signal to the flash ADC, which is strobed a second time after Error Amp 1 has settled. The new 8-bit result is used to correct the previous result, increasing the accuracy of this intermediate answer to 13-bit precision. Following this the Reference DAC is updated.

Both error amplifiers are active during the third pass. S2 is closed, allowing Error Amp 2 to amplify Error Amp 1's output. S3 now brings Error Amp 2's output to the flash ADC. The flash ADC is strobed a final time after the DAC and both error amplifiers have settled. The logic array combines the data from the third flash conversion with the earlier 13-bit word to produce the final 16-bit result. The T/H is returned to track mode, and Error Amp 2 is reconnected as an attenuator 50 ns after the completion of the third flash conversion to prepare for the next conversion.

The output data are placed on the data bus in two 8-bit bytes to be read by the host system. The Data Strobe output synchronizes the data transfer by providing a rising edge for the first byte and a falling edge for the second byte. The Hi/Lo Byte Select input allows the user to choose which data byte is presented first. B1 Select sets the polarity of the MSB to provide either complementary twos complement or complementary offset binary data.

The AD1385's internal linearity calibration capability may be used to compensate for shifts in Reference DAC linearity with time and temperature. The calibration sequence uses the AD1385's error amplifiers and flash converter to directly measure Reference DAC linearity errors. The routine calculates the Corrections required to each of the Reference DAC's 8 MSBs and stores these in an internal memory; the memory address is determined by the Reference DAC's codes. The RAM data control a Correction DAC whose output is summed with the Reference DAC's output. Together the two DACs provide the 18-bit linearity required for accurate A/D conversions. Calibration corrects only linearity errors, and has a negligible effect on gain and offset errors. A calibration cycle requires 15 ms and may be initiated at any time (see Autozero).

CONNECTION AND OPERATION OF THE AD1385

Analog Input

The analog input should be connected to the Track/Hold Input (Pin 25). Two pin programmable operating ranges are available: ±5 V and ±10 V. Connect the Track/Hold Output to V_{IN} A and/or V_{IN} B as follows:

Desired Scale	Connect V_{IN} A to	Connect V_{IN} B to
±5 V	Track/Hold Output	Track/Hold Output
±10 V	Track/Hold Output	Analog Signal GND

Harmonic distortion is lower when using the ±5 V range, while noise is lower when using the ±10 V range.

The AD1385's noise and distortion performance exceed the capability of most signal sources. Maintaining this performance at the system level requires attention to every detail of grounding, bypassing, and signal sources. A low impedance high bandwidth signal source is essential to achieve low distortion. Few monolithic amplifiers exist which can maintain signal fidelity at levels comparable with the AD1385's performance, even at low frequencies. High bandwidth means increased noise and decreased SNR. See *Testing the AD1385* for techniques of achieving the lowest possible noise and distortion.

Grounding

Proper treatment of the AD1385's power and ground connections is vital to achieve the best possible system performance. The ideal grounding arrangement is to have a single, solid, low impedance ground plane beneath the device to which all ground and supply bypassing connections are made. This results in the lowest possible ground noise and minimizes undesired interactions between the sensitive circuits inside the AD1385. Aperture uncertainty, for example, can be degraded by noise in Power Ground because the Hold Command signals are referenced to this ground. The digital interface between the AD1385 and the rest of the user's system is also critical. The following discussion will help in obtaining optimal performance. These guidelines are general and apply equally well to other high performance analog and digital circuits.

The AD1385 must connect to three other parts of the system: the input signal(s), the power supplies, and the digital interface. The system designer must determine the magnitude and type of ground currents and whether they are constant or dynamic. A system block diagram is a valuable aid to understanding how grounds should be connected for good performance. Figure 14 shows recommended ground connections for the AD1385 in a typical system.

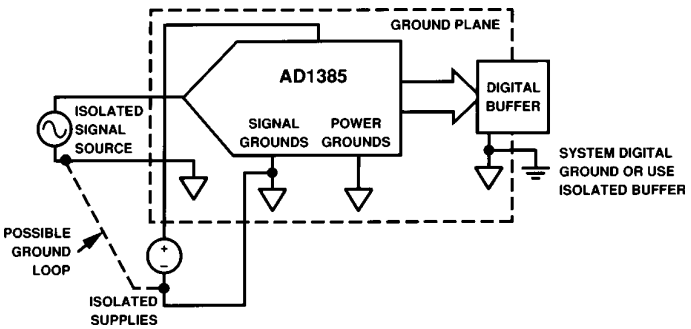


Figure 14. AD1385 Grounding

The AD1385 has a net ground current of about 40 mA. Most of this flows in the power grounds. There are also substantial dynamic currents in the power grounds. The signal grounds have primarily low level static (dc) currents. Signal and power grounds are separated inside the hybrid because the resistance and inductance inherent in thick-film construction would cause interactions between ground currents, leading to poor performance. (Remember that an LSB can be as small as 156 µV.)

Care must be taken to prevent the AD1385's ground currents from flowing in the signal ground between the signal source and the AD1385 if this ground has significant resistance. This is not usually a problem if the signal source is located on the same board as the AD1385 because the resistance can be made very low through the use of a ground plane.

The signal source's ground and supply currents must be considered when the source and ADC share common power supplies. A ground loop formed by the AD1385, the signal source, and the power supplies can cause significant errors.

The connection between the AD1385's ground plane and the system's digital ground is best made away from the AD1385. This will prevent noisy system ground currents from passing through critical parts of the ADC. In a very noisy environment it may be wise to isolate the entire analog circuit. Figure 14 shows the required isolation provided by a digital buffer. The buffer can then drive resistive and/or capacitive loads without compromising ground at the ADC. Using separate isolated supplies for the ADC and signal source will result in a single-point connection between system digital ground and the ADC's ground plane at the digital buffer.

Power Supplies and Bypassing

The AD1385 has four sets of power supply pins. These are:

±5 V Analog	(V_{DD1}/V_{SS1})
±15 V	($+V_{S1}$/$-V_{S1}$)
±15 V	($+V_{S2}$/$-V_{S2}$)
±5 V Power	(V_{DD2}/V_{SS2})

A single source may be used to supply like voltages (e.g., V_{DD1}, V_{DD2} from the same +5 V supply). Each of the four ±5 V supply pins should have a distinct low impedance connection to a well-bypassed central source node. This is required because each pin draws large transient currents. These dynamic currents, if passed through a common supply path, would introduce crosstalk and increase the AD1385's apparent noise. The two sets of ±15 V supplies need not be split in this fashion.

Every AD1385 supply pin should be bypassed to the ground plane with a high quality ceramic capacitor of 0.01 µF to 0.1 µF. This capacitor should be located as close as possible to the AD1385 to minimize lead lengths. Each V_{DD} and V_{SS} pin must also be bypassed to the ground plane with a 10 µF solid tantalum bypass capacitor located close to the AD1385. Ten microfarad bypass capacitors for $\pm V_{S2}$ (Pins 21 and 23) are also necessary. These power distribution concepts are shown in Figure 15.

All power supplies should be of the linear type. Switching power supplies are not recommended as they can introduce considerable high frequency noise into sensitive analog signal paths, degrading the AD1385's apparent performance.

Supply pins of equivalent voltage should not be allowed to differ by more than 0.3 V.

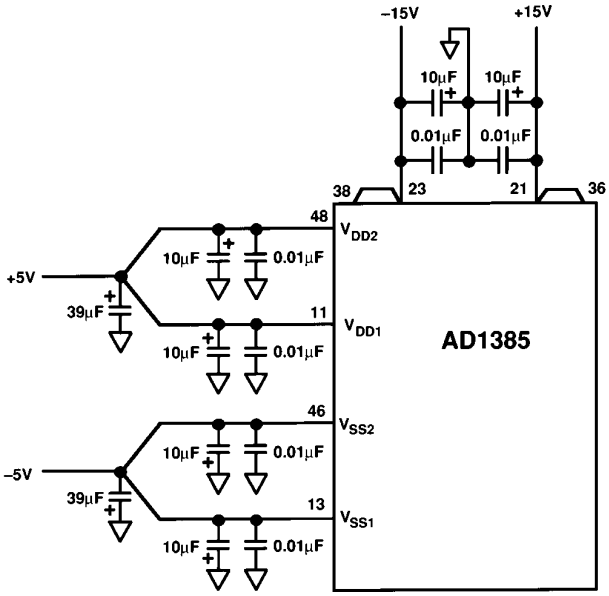


Figure 15. Recommended AD1385 Power Distribution. All 10 μF and 0.01 μF capacitors must have minimum lead length and be located as close as possible to the bypassed pins. Make all ground connections directly to the groundplane.

If separate ground planes are used for Signal and Power Ground, the supplies should be bypassed as follows:

Supply	Bypass to
±5 V Analog	Signal Ground
±15 V ($+V_{S1}/-V_{S1}$)	Signal Ground
±15 V ($+V_{S2}/-V_{S2}$)	Power Ground
±5 V Power	Power Ground

Care is also required when using a +5 V powered crystal oscillator to provide the AD1385's clock signal. These devices produce considerable supply noise and proper bypassing is essential. The oscillator should be bypassed with both ceramic and solid tantalum capacitors using minimum lead lengths. A 10 Ω resistor in series with the +5 V supply provides additional isolation and low pass filtering of transients produced by the oscillator.

Reference

The AD1385 has an excellent internal reference with a typical temperature coefficient of 5 ppm/°C. The Reference Out (Pin 39) is normally connected to Reference In (Pin 32). An external reference may be connected to the reference input if desired. The reference input pin requires negligible current. The reference input voltage should not exceed +11 V and must remain more positive than 0 V. The reference output requires no bypassing and should not be capacitively loaded. If an external reference is used, it must have low noise to avoid degrading the signal to noise ratio of the AD1385.

The reference output can source up to 2 mA of static (dc) current without affecting the performance of the AD1385. By using the AD1385's internal reference as the system reference, gain error over temperature can be minimized.

DIGITAL INTERFACES

10 MHz Clock

The AD1385 requires a stable external clock. A 10 MHz clock provides a sample rate of 500 kilosamples per second. Since the ADC operates synchronously with this clock, clock phase noise will appear as jitter in the aperture time. Lower clock frequencies may be used, and the sample rate will be reduced proportionately.

Standard TTL and CMOS crystal oscillator modules may be used successfully to generate the required 10 MHz clock signal. These oscillators often create considerable power supply transient noise. The oscillator should be bypassed with both ceramic and solid tantalum capacitors using minimum lead lengths. A 10 Ω resistor in series with the +5 V supply provides additional isolation and low-pass filtering of transients produced by the oscillator. See Figure 16.

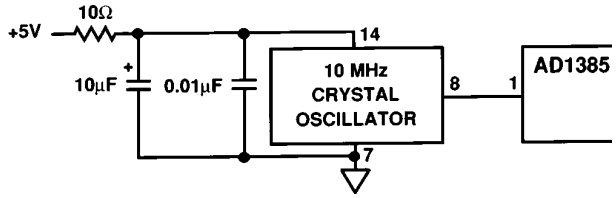


Figure 16. Isolating Clock Noise. Bypass Capacitors Should Be Located Close to the Oscillator

Transmission line effects cannot be ignored when supplying the AD1385's 10 MHz clock. The large impedance mismatch between typical PCB traces and the AD1385's CMOS clock input can give rise to reflections and high frequency transients when the 10 MHz clock source is located more than a few inches from the AD1385. This noise can corrupt local ground and cause degradation in the AD1385's apparent SNR performance. A series termination resistor of 50 Ω to 100 Ω, located at the clock source, will usually eliminate this problem.

START CONVERT (PIN 18)

Synchronous Operation

The Start Convert signal acts like the data input of a flip-flop. A conversion begins on the first rising clock edge after Start Convert goes high (provided setup time requirements are met). This edge drives Hold Command Out high, switching the T/H into Hold mode. Hold Command Out (Pin 19) should be connected to Hold Command In (Pin 22) for synchronous operation. Continuous conversions at a 500 kHz rate may be obtained by holding Start Convert high. The 10 MHz clock may be divided down and used to drive the Start Convert input when a lower conversion rate is desired. This will provide clock-synchronized conversions at the lower rate. Synchronous conversion timing is shown in Figures 17 and 18.

Start Convert may also be used as a gate to capture data in a time window. The rising and falling edges of Start Convert define the beginning and end of the window during which conversions are desired.

Some restrictions apply when using a pulse to drive the Start Convert input. Start Convert is ignored during a conversion for seven clock periods after Hold Command Out goes low to signal the end of a conversion. The state of Start Convert is sampled on each rising clock edge, beginning with the seventh edge after Hold Command Out goes low, until a logical high is detected.

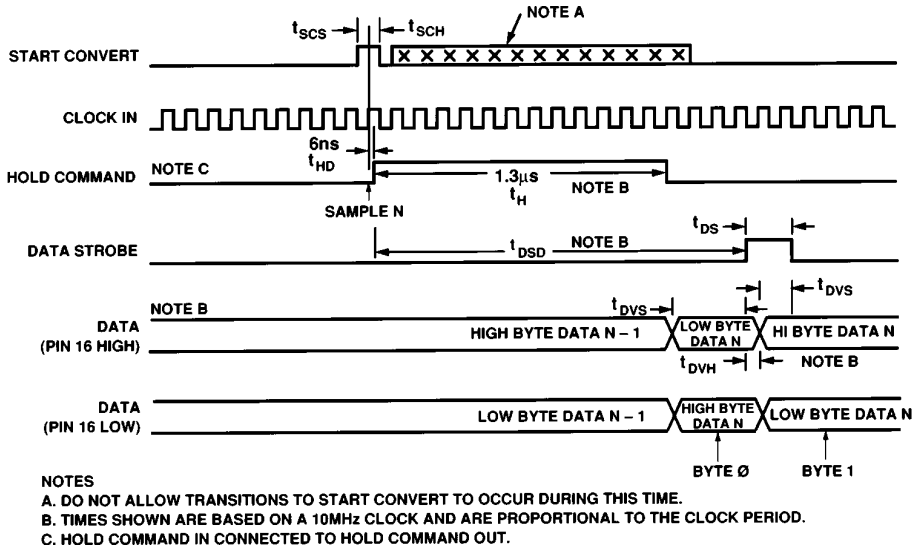


Figure 17. Start-Convert Controlled Conversion Timing

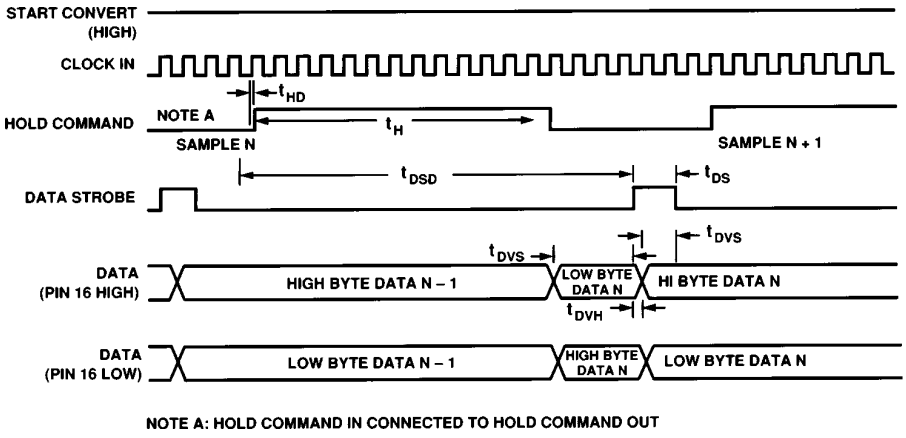


Figure 18. Free Running Conversion Timing

At this point a new conversion will be initiated. The minimum setup and hold times for Start Convert relative to the rising clock edge are 10 ns. Start Convert transitions should not be placed in the window which begins 100 ns (one clock period) after the rising edge of Hold Command Out and which ends 1300 ns (thirteen clock periods) after this rising edge (see Figure 17). This minimizes internal coupling between Start Convert and sensitive internal circuit nodes.

Transmission line effects at the Start Convert input should be considered when designing circuit boards for the AD1385. A series termination resistor of 50 Ω to 100 Ω is recommended when the source of Start Convert is more than a few inches away from the AD1385. This will control reflections and transients which could otherwise degrade the part's performance.

Asynchronous Operation

In synchronous operation the T/H is placed into Hold mode by the first rising clock edge after Start Convert goes high. This mode of operation provides maximum rejection of system clock noise. Some applications may require the AD1385 to operate asynchronously, that is, with the Start Convert input directly controlling the track-to-hold transition. This may be achieved using a 2-input OR gate connected as shown in Figure 19. The rising edge of Start Convert places the T/H into Hold mode; the A/D conversion cycle begins with the first rising clock edge after the Start Convert transition, and Start Convert must remain high during at least one rising clock edge in order to begin the conversion. The width of Start Convert should be either less than 150 ns or greater than 1400 ns to minimize coupling between the falling edge of Start Convert and sensitive internal nodes. In asynchronous operation the T/H will remain in Hold

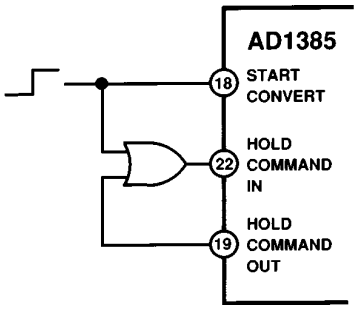


Figure 19. Connecting the AD1385 to Sample the Input Signal Asynchronously from the Clock

mode as long either Hold Command Out or Start Convert is high. Care is needed in defining system timing to ensure that the T/H has a minimum of 700 ns for signal acquisition before another conversion begins. The minimum width of Start Convert is 20 ns, the sum of t_{SCS} and t_{SCH}, the minimum setup and hold times.

Transmission line effects at the Start Convert and Hold Command In inputs should be considered when designing circuit boards for the AD1385. A series termination resistor of 50 Ω to 100 Ω is recommended when the source of either of these signals is more than a few inches away from the AD1385. This will control reflections and transients which could otherwise degrade the part's performance.

Output Data

The output data are multiplexed in two bytes onto an 8-bit data bus. Data are guaranteed to be stable at the time of the edges of Data Strobe (Pin 15). Hi/Lo Byte Select (Pin 16) controls which byte is presented first. If Hi/Lo Byte Select is high, then BYTE0 is B9–B16 and BYTE1 is B1–B8. The order of the data bytes is interchanged when Hi/Lo Byte Select is low. BYTE 0 and BYTE 1 are defined in the timing diagram Figure 17. B1 is the most significant bit of the reconstructed 16-bit data.

B1 SELECT (Pin 44) determines whether data is presented in complementary twos complement or complementary offset binary form. Complementary twos complement data is provided when B1 Select is LOW. $\overline{OE}$ may be used to place the data bus into a high impedance state.

The arithmetic unit in the AD1385 saturates at all 0s or all 1s if the input range is exceeded.

Table I.

B1 Select	**0**	**1**
Data Format	Complementary Twos Complement	Complementary Offset Binary
–Full-Scale Data	7FFFH	FFFFH
0 V Data	FFFFH	8000H
+Full-Scale Data	8000H	0000H

CALIBRATION (Pins 28 and 41)

Calibration corrects for linearity errors in the Reference DAC arising from internal component mismatches or temperature changes. It has a negligible effect on gain and offset errors, and these should be corrected by other means. The AD1385 must be calibrated after power-up, and recalibration is recommended whenever the part's temperature has changed by more than 15°C. Performance degrades gracefully with temperature changes, resulting in small but gradual decreases in SNR and increases in distortion which may be eliminated by recalibration. Calibration codes are stored in internal RAM and are lost when power is removed. Figures 20–22 show the effects of uncalibrated versus calibrated operation.

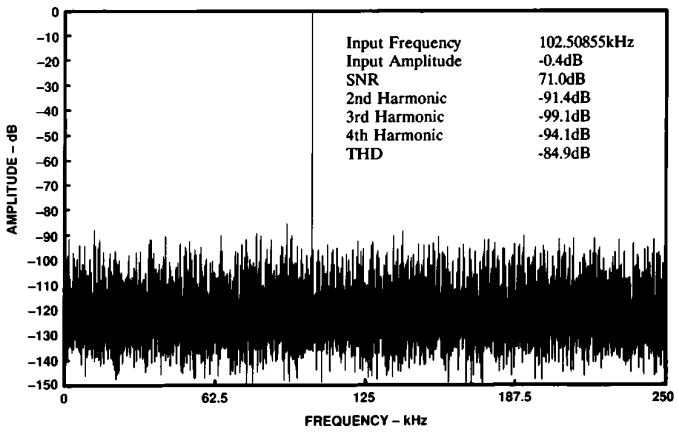


Figure 20. Full-Scale Power Spectral Density after Power-up at T_{CASE} = +25°C Without Calibration, ±5 V Range, 16384-Point FFT, 500 kHz Sample Rate. Compare with Figure 4.

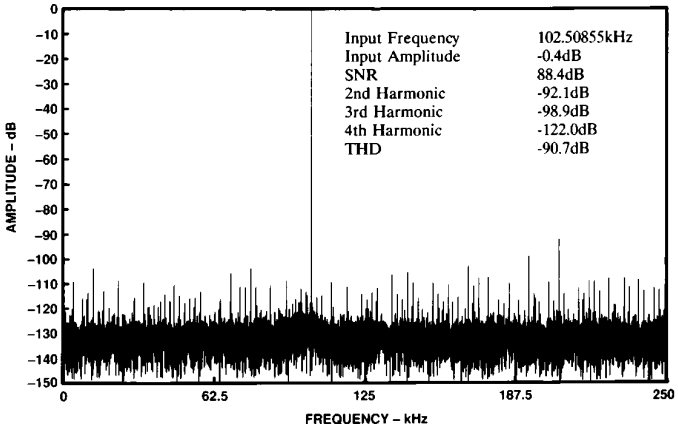


Figure 21. Full-Scale Power Spectral Density at T_{CASE} = +125°C, Calibration Performed at T_{CASE} = +25°C, ±5 V Range, 16384-Point FFT, 500 kHz Sample Rate

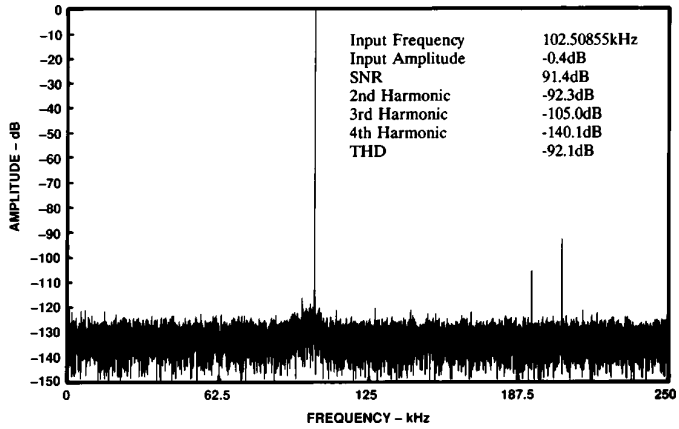


Figure 22. Same as Figure 21 Following Recalibration at T_{CASE} = +125°C

No external switches or relays are required for calibration and all connections to the AD1385 may remain in place. The Track/Hold is internally isolated from the analog input by analog switches and used as a buffer during the calibration process. Its signal output (Pin 27) *must* remain connected to the A/D input(s) (Pin 30 and/or Pin 31, as appropriate) for successful calibration. Hold Command Out (Pin 19) must also remain connected to Hold Command In (Pin 22), either via direct connection (synchronous sampling) or with an external OR-gate (asynchronous sampling, Figure 19).

A calibration sequence may be initiated at any time by bringing the $\overline{\text{CAL}}$ input (Pin 41) low. The calibration request remains pending if a conversion is in process, and calibration begins on the first rising clock edge after the end of that conversion. Calibration begins on the first rising clock edge after $\overline{\text{CAL}}$ is asserted if the AD1385 is idle when calibration is requested. The minimum pulse width for the CAL input is 20 ns. The $\overline{\text{CAL}}$ input has priority over the Start Convert signal in all cases.

The CAL Status output (Pin 28) goes high as soon as calibration begins and remains high until the calibration cycle is completed. Pulsing $\overline{\text{CAL}}$ low while CAL Status is high has no effect. A full calibration requires about 15 ms with a 10 MHz clock and proportionately longer with slower clocks.

Calibration has no effect on the contents of the Autozero register. The apparent zero point may shift a few LSBs as a result of the calibration. Autozero after recalibration will provide the greatest possible accuracy (see *Autozero)*.

The AD1385 controller allocates 17 clock periods after the conclusion of a calibration cycle for Track/Hold recovery and signal acquisition. Activity at the Start Convert input during this interval is ignored. Figure 23 shows the timing associated with the resumption of synchronous conversions following a calibration cycle.

Start-Convert should remain low during the calibration period when using asynchronous sampling (Figure 19).

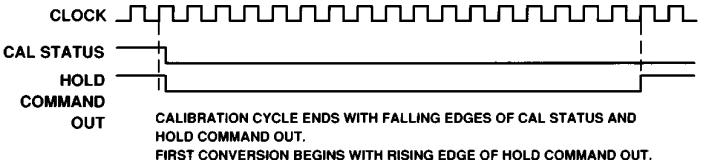


Figure 23. Resumption of Synchronous Conversions Following Completion of Calibration

The $\overline{\text{CAL}}$ input may be held low indefinitely, causing repeated calibration cycles. The AD1385 will complete the calibration in progress when $\overline{\text{CAL}}$ goes high and will then begin normal conversions after the 17-clock-period delay. This simplifies the system-level implementation of the power-up reset function.

The AD1385 requires a 5 minute warmup to reach thermal equilibrium after power is applied, and calibration may drift slightly during this time. Occasional recalibration will provide a slight improvement in distortion and noise performance during warmup.

AUTOZERO (Pin 45)

The Autozero function may be used to digitally correct internal offsets in the Track/Hold and ADC as well as external offsets. To use Autozero the Track/Hold input must be connected to a zero reference prior to the zeroing conversion. This connection is external to the AD1385 and must be provided by the user; the resistance of this connection is not critical but should be less than 1000 Ω. An Autozero cycle forces the AD1385's digital output to indicate exactly zero when its input is at the zero point, nominally 0 V. (This assumes that the complementary twos complement data format is used. Autozero forces the digital output to midscale when the selected data format is complementary offset binary.) Autozero operates by storing the digital result of a zeroing conversion and subtracting it from all subsequent conversion results. This reduces the maximum nonsaturating input of the AD1385 a small amount at one end of its range depending on the magnitude and polarity of the offset.

The Autozero feature is enabled by driving the Autozero input (Pin 45) low before a falling edge at the Data Strobe output. Offset data will be stored on the first rising edge of Data Strobe after Autozero is brought high; the offset data are also available on the AD1385's data bus during this Data Strobe pulse. Autozero operation is illustrated in Figure 24. All subsequent A/D conversions will be digitally corrected by the offset term as long as Autozero remains high. The offset register is cleared when Autozero goes low and the contents of the data output registers will revert to their uncorrected value. Figure 24 shows Autozero timing requirements. Autozero cannot be activated until the first conversion after power-up has been completed.

The Autozero feature may be disabled by keeping Autozero low.

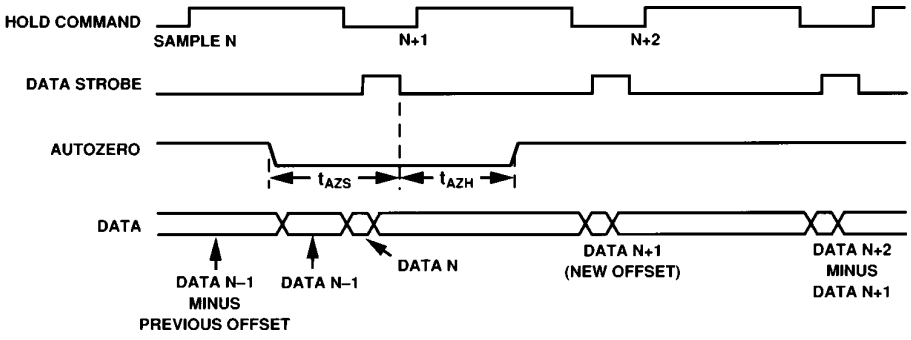


Figure 24. Autozero Cycle Operation

GAIN ADJUST (Pin 40)

The internal reference of the AD1385 may be adjusted by varying the voltage applied to the Gain Adjust pin. The input impedance of this pin is nominally 20 kΩ, with a tolerance of ±20%. A change of 1 V on Pin 40 will change the reference voltage by about 10 mV. The reference may be adjusted by ±150 mV without degrading the AD1385's performance. The simplest method of implementing the gain adjust is to connect a potentiometer between the ±15 V supplies, with the wiper connected to the Gain Adjust pin. Care should be taken to ensure that noise does not enter the ADC through the Gain Adjust pin.

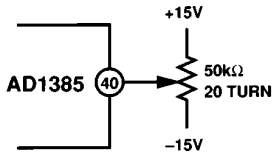


Figure 25a. AD1385 Gain Adjust Circuit

OFFSET ADJUST (Pin 29)

The ADC's offset voltage may be adjusted by means of a voltage applied to the Offset Adjust pin. The nominal adjustment sensitivity is 0.005% FSR/V. The input impedance is 20 kΩ with a ±20% tolerance. The simplest way to implement the offset adjust is to connect a potentiometer between the ±15 V supplies, with the wiper connected to the Offset Adjust pin. Care should be taken to ensure that noise does not enter the ADC through the Offset Adjust pin.

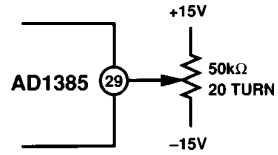


Figure 25b. AD1385 Offset Adjust Circuit

APPLICATIONS

Mounting and Thermal Considerations

The AD1385's operation is specified over a case temperature range of –55°C to +125°C. Case temperature in still air is normally about 20°C above ambient, and a heat sink and/or air flow is required to guarantee specified performance when high ambient temperatures are expected. A thin heat transfer plate, mounted beneath the package to conduct heat into the ground plane, may be sufficient. This plate may be made of metal provided care is taken to prevent shorting the package pins. An excellent alternative is to use an elastomeric heat conducting material. These materials will conform to the board and to the AD1385 package to improve heat transfer while reducing mechanical stress. Elastomeric materials normally will not require thermally conductive grease.

Testing the AD1385

It is difficult to test the AD1385 with ordinary test methods because of the part's very low distortion and noise. The number of output codes and the nature of the analog to digital conversion make static tests of performance especially cumbersome. Subranging converters with error correction circuitry can have flaws at any place in their transfer function and all codes must be exercised for a complete test.

Histograms provide a convenient way to measure all codes in a modest amount of time. Even histograms can be slow, when 20 million conversions (40 seconds) may be required to achieve statistically valid results.

Dynamic tests based on FFTs are the most powerful. They quantify noise and distortion as a function of input frequency. From them one can infer qualitative integral and differential nonlinearity performance while determining the ADC's specific dynamic performance. FFTs are especially useful for systems which require excellent dynamic response, such as magnetic resonance imaging. They also uncover performance problems that don't show up in static tests of linearity.

The difficulty in doing FFT tests stems from the requirement for ultra pure sine wave inputs at various frequencies over the operating bandwidth of the ADC. Even the best available generators are not capable of supplying signals with sufficiently low noise and low distortion for testing the AD1385. Few generators permit phase-locking to the ADC clock. (Phase-locking makes it possible to obtain an integral number of cycles of the input sine wave within the FFT data window, which in turn eliminates the need for windowing functions and the spectral spreading they cause.)

The best generator currently available for this purpose is the Brüel and Kjaer Model 1051 (or 1049). This generator provides a programmable output frequency up to 250 kHz with better than 0.001 Hz resolution. The generator's distortion performance at frequencies below 20 kHz is better than the AD1385 but degrades at 100 kHz and higher. Noise is a problem at all frequencies, being about –85 dB over the AD1385's bandwidth. Both noise and distortion can be reduced to acceptable levels with filters. Passive narrow bandwidth filters will reduce harmonic distortion to less than –100 dB. Inductors wound on large pot cores with air gaps can be made quite linear, and with careful winding will provide low loss and low capacitance. Such filters will reduce noise to negligible levels outside their pass band to provide a much better view of actual ADC performance. The effect of aperture jitter, for example, cannot be observed without a filter.

The FFTs shown in Figures 3-12 were produced using these methods. These tests are done as a normal part of production testing to guarantee the dynamic performance of the AD1385.

Multiplexing and High Impedance Inputs

Multiplexing the AD1385's input presents several challenges in component selection. The ON-resistance of most available multiplexers and switches is a function of the applied voltage. This, coupled with the AD1385's 2.5 kΩ input resistance, can introduce significant harmonic distortion unless the multiplexer output is buffered. All monolithic switches and multiplexers exhibit this behavior to some extent, with CMOS-based designs generally worse than those using JFET technology.

An acceptable alternative is the DG180 family produced by Siliconix. These hybrid switches use discrete JFET pass devices to provide an extremely low ON-resistance virtually independent of signal level. Care should be taken to match the switch's common-mode signal capability with operating range desired for the AD1385. The finite on-resistance of any unbuffered switch driving the AD1385 will introduce a gain error, and that error may change appreciably over temperature.

Buffering the multiplexer's output will eliminate the problems caused by its ON-resistance. The choice of buffer depends on the nature of the system's input signals. There are two cases to consider: static inputs and dynamic inputs.

"Static" Applications

Amplifier noise, CMRR linearity, and settling time are of primary importance when the inputs are low frequency or DC. This is the case in a CAT-scan imager, for example, when signals are produced by integrating photocurrents. Noise limits ultimate system resolution. The AD1385 has a typical input-referred noise of 70 μV rms. Buffer noise must be added to this in a root-sum-squares fashion to determine total system noise. A buffer amplifier which adds noise of 18 μV rms, for example, will result in a system noise level of $(18^2 + 70^2)^{1/2}$ = 72 μV rms, a negligible increase. Detailed system noise calculations require knowledge of the buffer's noise spectral density and equivalent noise bandwidth. The AD1385's equivalent noise bandwidth is 2.2 MHz. *Low Noise Electronic Design* (C.D. Motchenbacher and F.C. Fitchen, John Wiley and Sons, New York, 1973) provides excellent discussions of noise analysis and calculations.

Buffer amplifier CMRR produces only gain error as long as the value of CMRR is independent of signal level. The size of this "gain error" is directly related to the actual value of CMRR; an amplifier with 60 dB CMRR will create an apparent gain error of 0.1%. The precise value of CMRR is not critical as long as it remains independent of signal level. Any variation in CMRR with input level will introduce nonlinearity. The smaller the value of CMRR (in dB), the more critical variations in this value become. An amplifier with CMRR ranging from 100 dB to 110 dB over the range of –10 V to +10 V will produce negligible nonlinearity, while an amplifier whose CMRR varies from 60 dB to 70 dB over the same range would be completely unacceptable.

Buffer settling time will affect the system's throughput. The system sample rate can be maintained at 500 kHz provided the buffer's settling time is less than about 1.7 microseconds. The input channel should be switched just after the AD1385's SHA enters Hold mode as indicated by a rising edge at Hold Command In (Pin 22).

"Dynamic" Applications

Dynamic applications complicate the choice of buffer amplifier. The amplifier's harmonic distortion performance now becomes as important as its noise, CMRR linearity, and settling behavior. Few manufacturers specify amplifier THD in the noninverting configuration. These specifications, when available, seldom address signals greater than 10 V p-p or frequencies above 1 kHz. It may be necessary to characterize candidate amplifiers from several vendors to find the best fit to the amplitude and frequency requirements of a particular application. Such evaluations are easily performed using a spectrum analyzer. A notch filter tuned to the fundamental frequency greatly improves measurement resolution. It is also possible to use the AD1385 as the measuring device by performing FFTs on the output data. Refer to the discussion of signal sources in *Testing the AD1385*.

Unipolar Operation

The AD1385 does not provide a direct unipolar input capability. Unipolar inputs can be achieved using the circuits of Figures 26 and 27. The circuit in Figure 26 is suitable when a low input impedance is acceptable. The AD845 is an excellent amplifier choice for this application. Multiplexed applications should use the circuit of Figure 27. The discussions under High Impedance Inputs also apply to amplifier selection for high impedance unipolar operation.

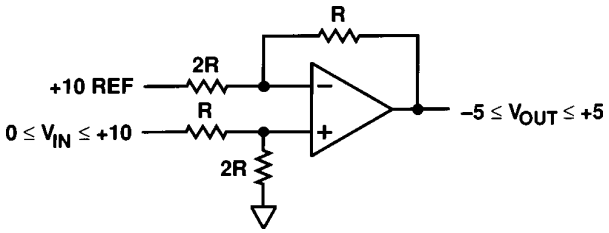


Figure 26. Unipolar-to-Bipolar Conversion (Low Input Impedance)

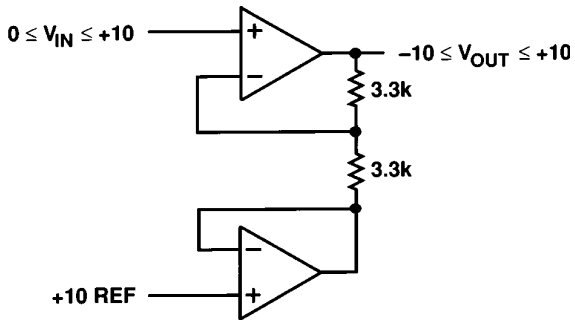


Figure 27. High Input Impedance Unipolar-to-Bipolar Conversion Circuit

Data Bus Interface

The AD1385's data outputs are 4 mA CMOS drivers and are not intended to be connected directly to a system data bus. Charging and discharging a capacitive data bus creates large supply transients and ground spikes which can interfere with the AD1385's operation and result in erroneous data. Registers and/or buffers should be used to isolate the AD1385 from the bus. Buffering devices should be located close to the AD1385 to minimize the capacitive load presented to the converter's data outputs. Control will be simplified by permanently grounding the AD1385's $\overline{OE}$ input when using buffers. A schematic of a typical 16-bit bus interface is shown in Figure 28.

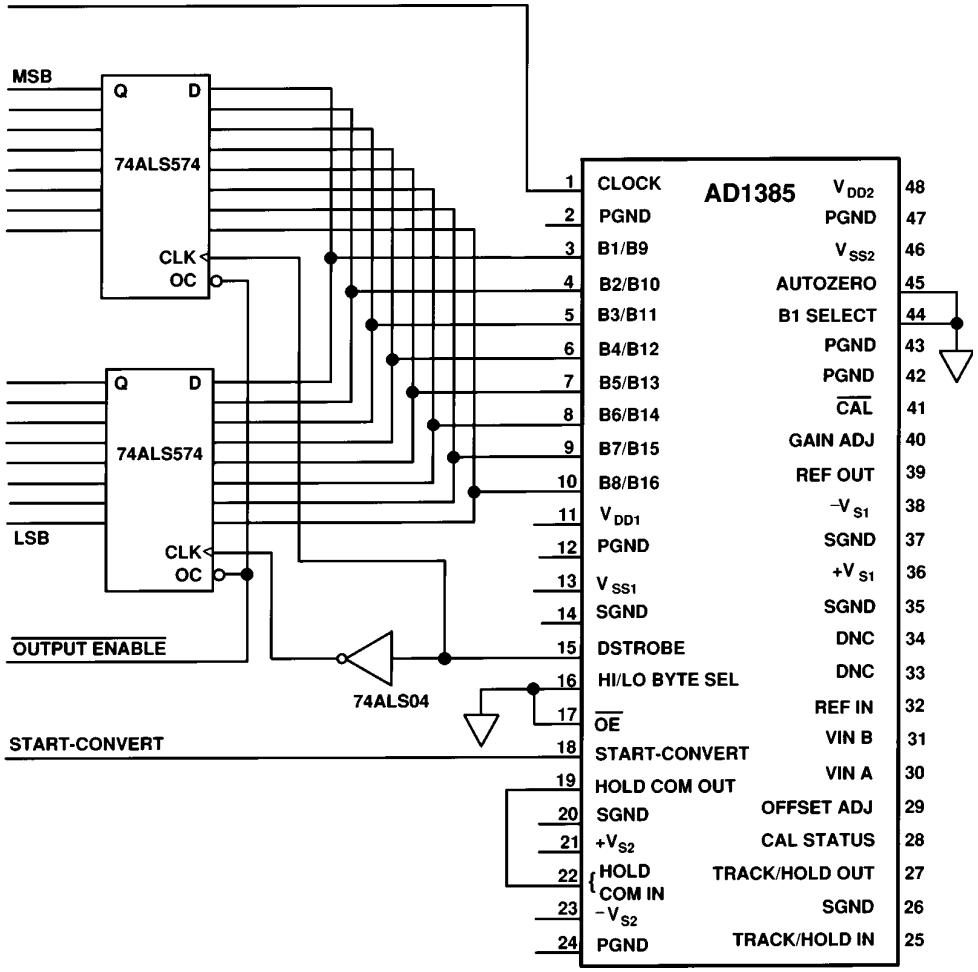


Figure 28. Basic AD1385 Digital Interface (16-Bit Complementary 2s Complement Data, Autozero Not Used, Other Digital and Analog Inputs Not Shown)

Sample Board Layout

Figures 29-34 show the layout of an evaluation board for the AD1385. This layout incorporates the grounding, power distribution, and interface concepts described in previous sections. This 4-layer layout makes extensive use of ground and power planes and provides optimal AD1385 performance.

The layout accommodates buffer amplifiers with standard op amp pinouts in both 14- and 8-pin DIP packages. The pin numbers shown for U12 in Figure 29 refer to the 14-pin format. An 8-pin op amp such as the AD845 should be positioned with package Pin 4 inserted in layout Pin 6. The AD845 provides slightly better distortion performance than the AD842, an amplifier in a 14-pin package, with no significant increase in noise.

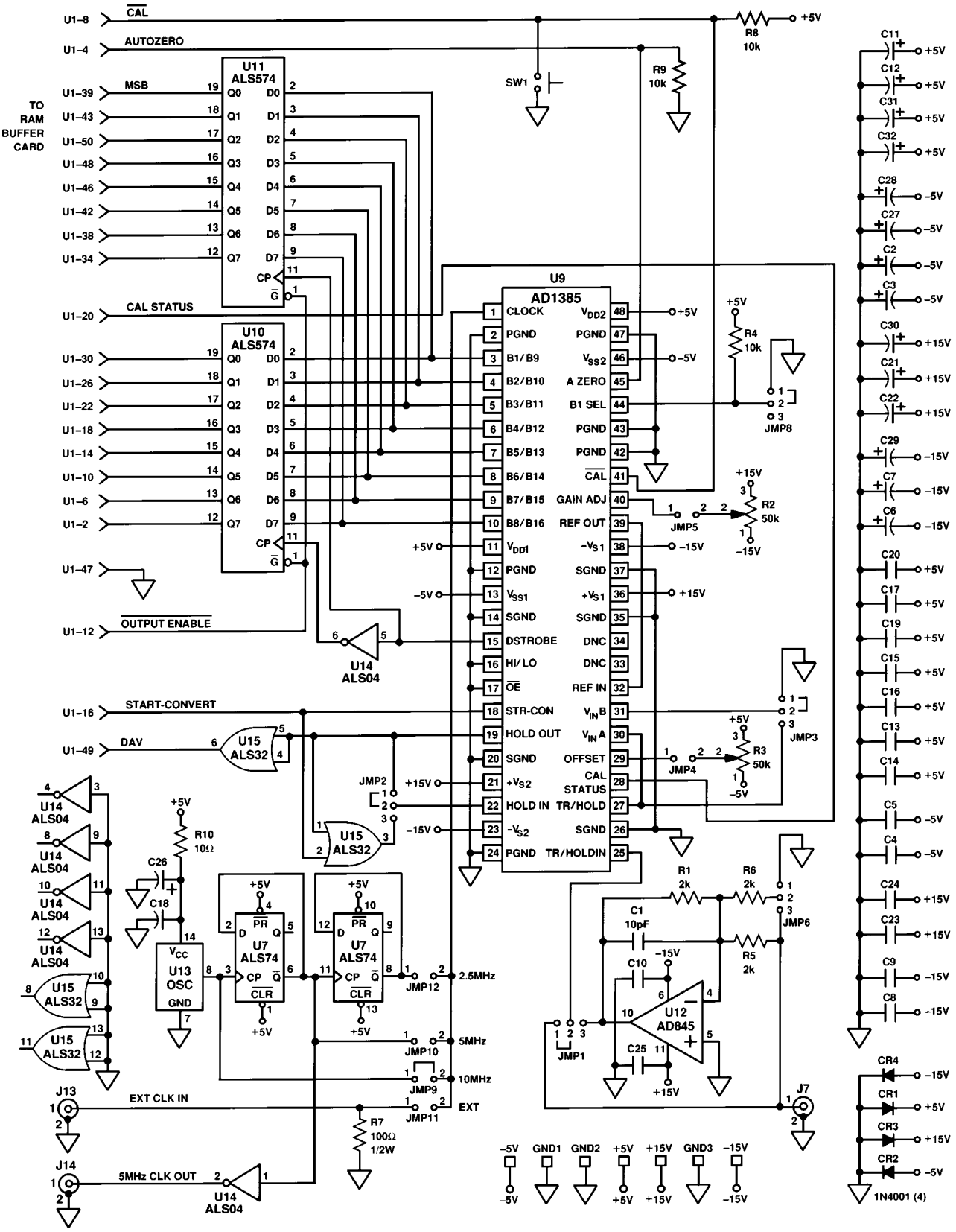


Figure 29. AD1385 Evaluation Board Schematic

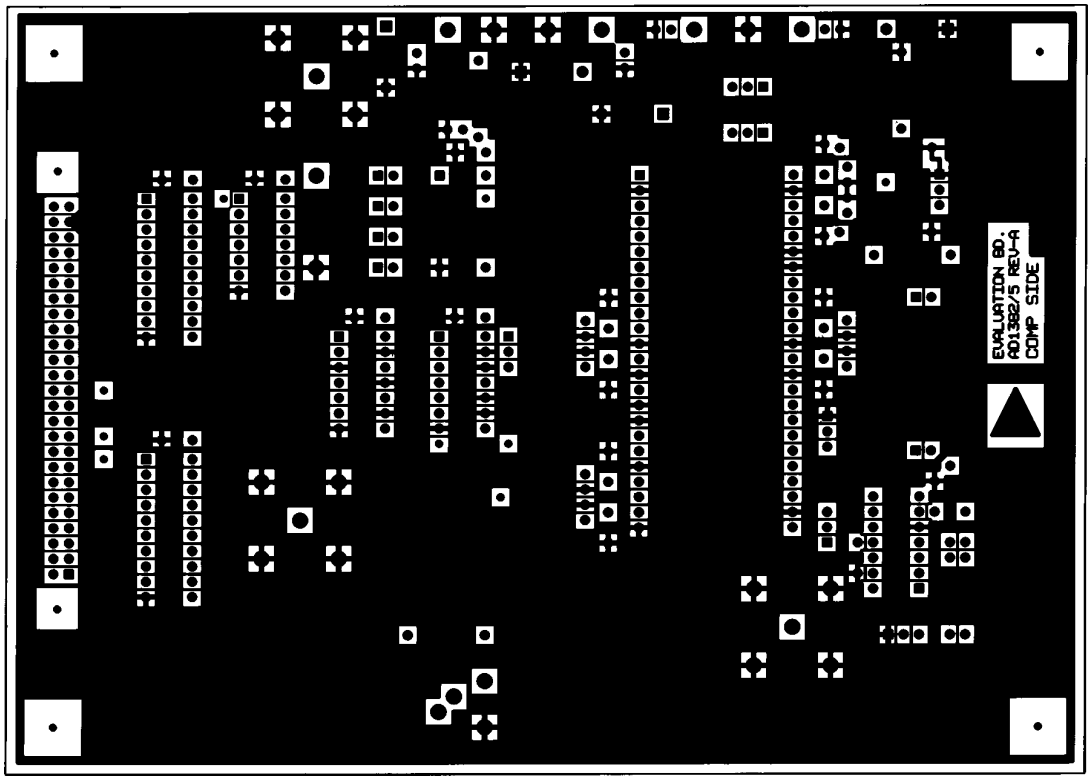


Figure 30. AD1385 Evaluation Board Layout, Layer 1 (Component Side)

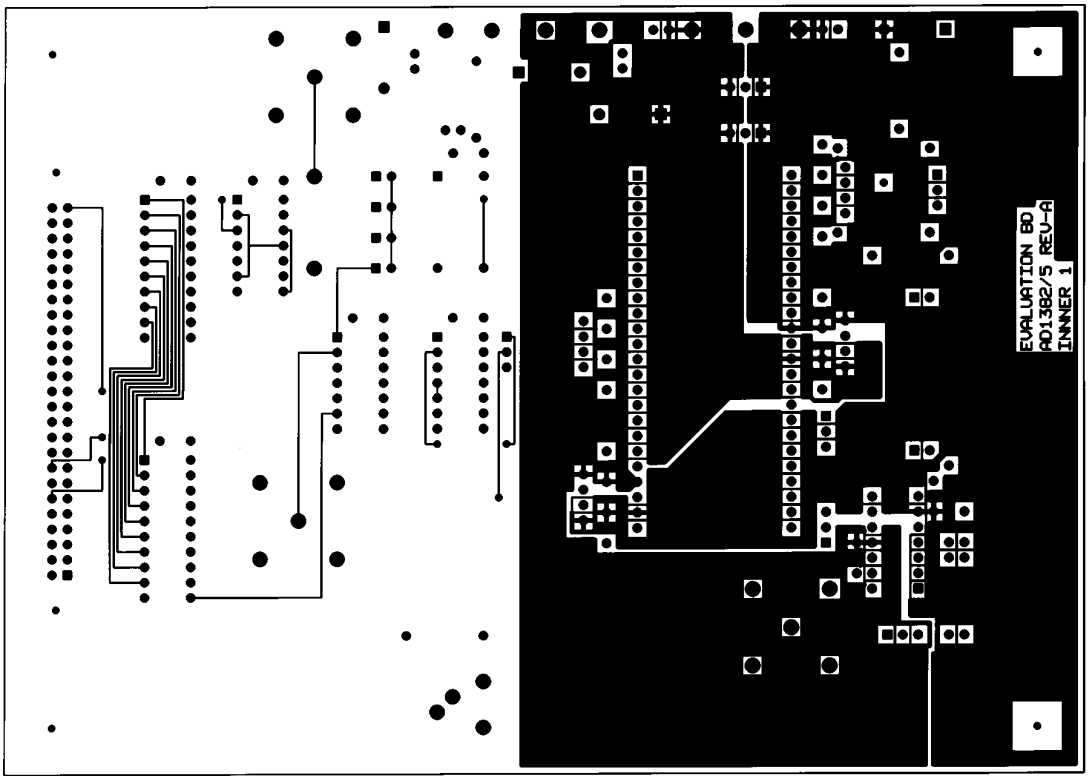


Figure 31. AD1385 Evaluation Board Layout, Layer 2 (±15 V Planes)

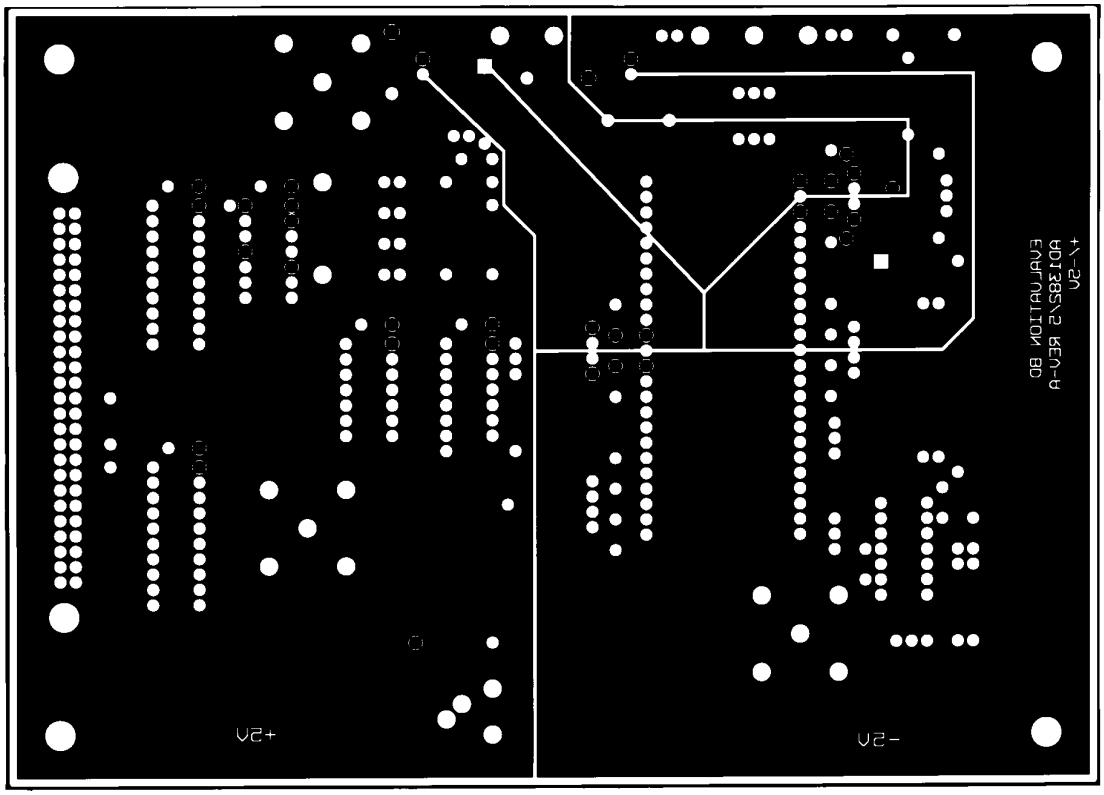


Figure 32. AD1385 Evaluation Board Layout, Layer 3 (±5 V Planes)

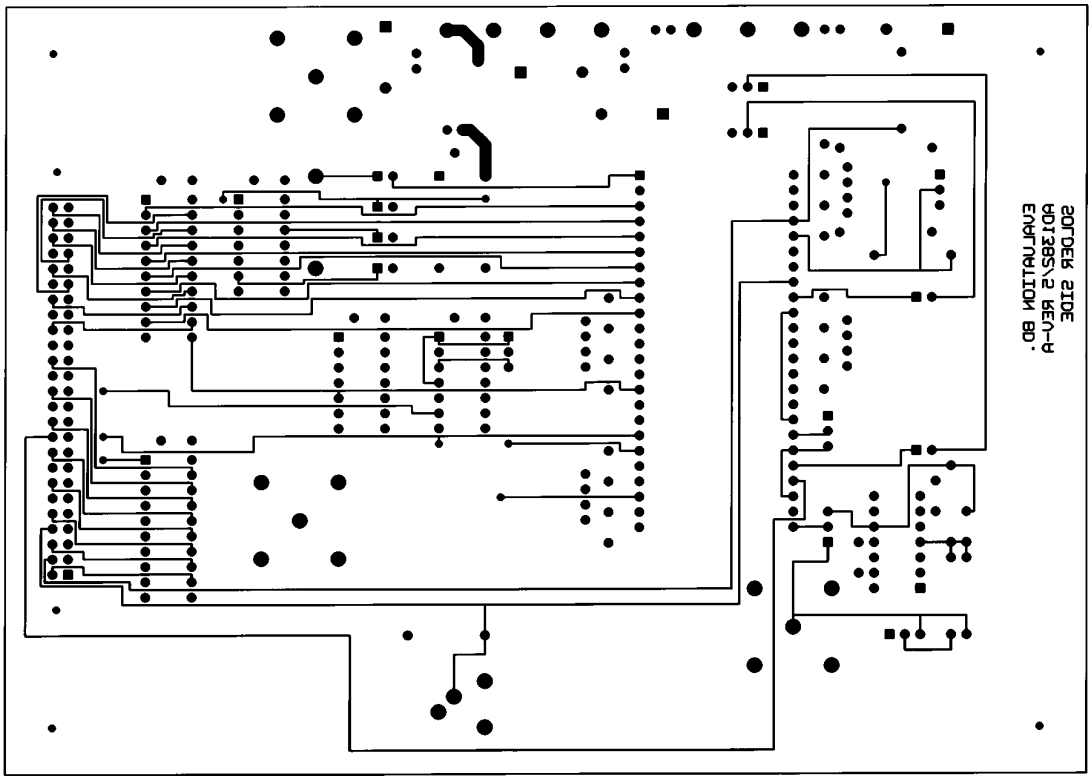


Figure 33. AD1385 Evaluation Board Layout, Layer 4 (Solder Side)

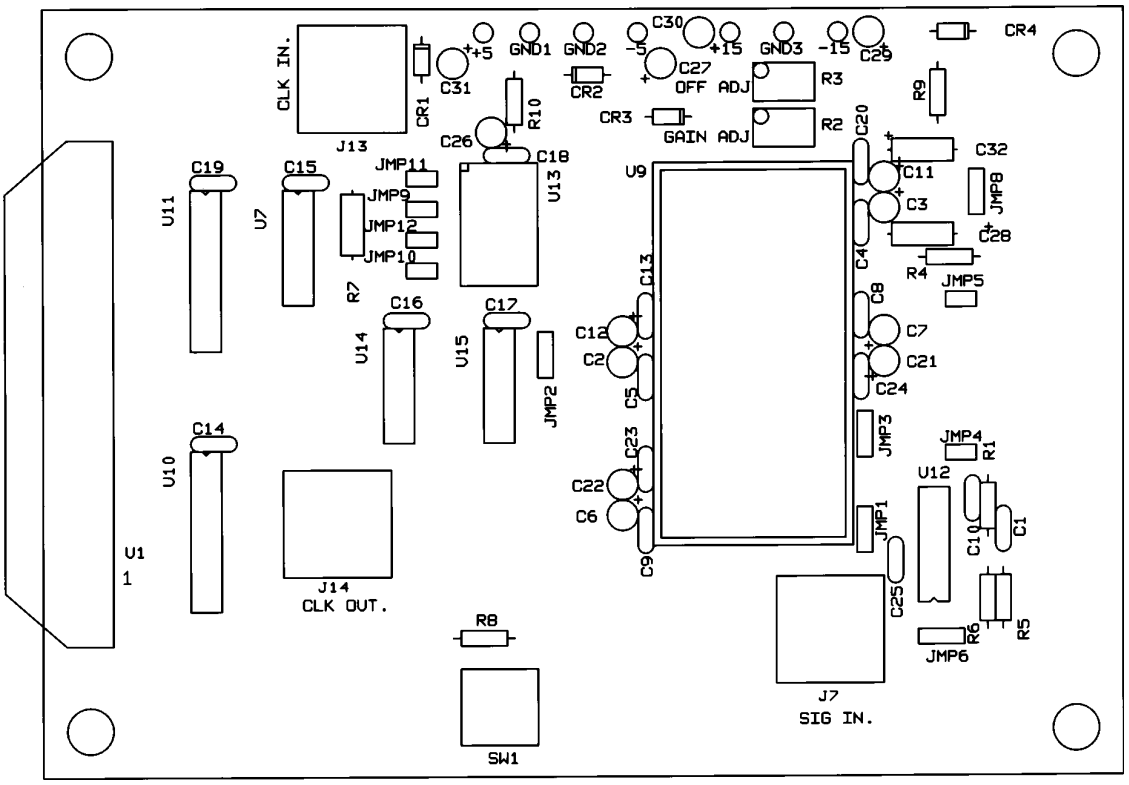


Figure 34. AD1385 Evaluation Board Silkscreen

AD1385 EVALUATION BOARD PARTS LIST

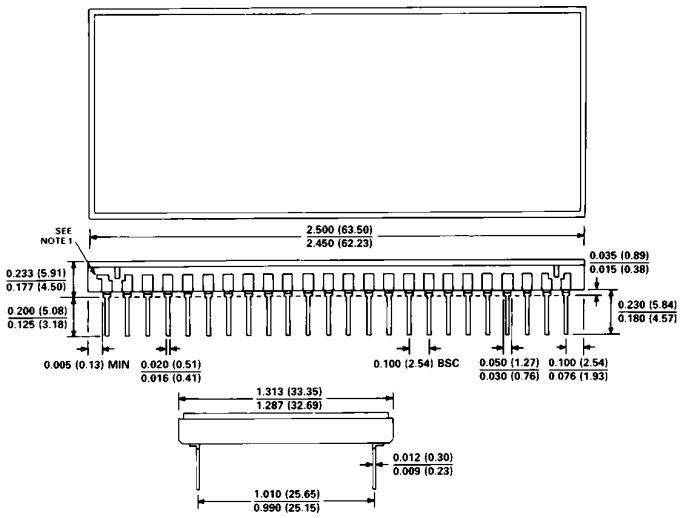
Qty.	Ref. Des.	Description (Manufacturer/PN)
1	C1	Ceramic Capacitor, 10 pF, 50 V (Mallory CEC100J)
13	C2, C3, C6, C7, C11, C12, C21, C22, C26, C27, C29–C31	Tantalum Capacitor, 10 µF, 35 V (Mallory TDL106K035S1D)
16	C4, C5, C8–C10, C13–C20, C23–C25	Ceramic Cap, 0.1 µF, 100 V(Murata Erie RPE122Z5U104M100V)
2	C28, C32	Tantalum Capacitor, 39 µF, 10 V (Kemet T110B396K010AS)
4	CR1–CR4	1N4001 Diode
3	J7, J13, J14	BNC Female, PC Mount (Pomona 4578)
8	JMP2–JMP6, JMP8, JMP9, JMP13	Jumper, 2 Position (3M 929950-00)
3	R1, R5, R6	RN55C Resistor, 2.00k
2	R2, R3	50k 20-Turn Trimpot* (Bourns 3299W-1-503)
2	R4, R8, R9	RN55C Resistor, 10.0k
1	R7	Carbon Composition Resistor, 100 Ω, 1/2 W
1	R10	RN55C Resistor, 10 Ω
1	SW1	Momentary SPST, C & K KS l l-R2-C-Q
1	U7	74ALS74
1	U9	AD1385KD (Analog Devices)
2	U10, U11	74ALS574
1	U 12	AD845KN (Analog Devices)
1	U13	10 MHz DIP Crystal Oscillator
1	U14	74ALS04
1	U15	74ALS32
2	—	Socket Strip (SPC MPS1P-32-GG)
1	—	Pin Strip (3M 929647-01-36)
1	—	Socket, 14-Pin Oscillator (Augat 504-AG10D)
4	—	Socket, 14-Pin (Augat 514-AG11D)
2	—	Socket, 20-Pin (Augat 520-AG11D)
2	—	Ejector Latch (3M 3505-3)
1	—	50-Pin Connector (3M 3433-5002)
2	—	Screw, 2-56 × 1/2
2	—	Hex Nut, 2-56

*Trimpot is a trademark of Bourns.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Pin Bottom Brazed Ceramic DIP (DH-48A)



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