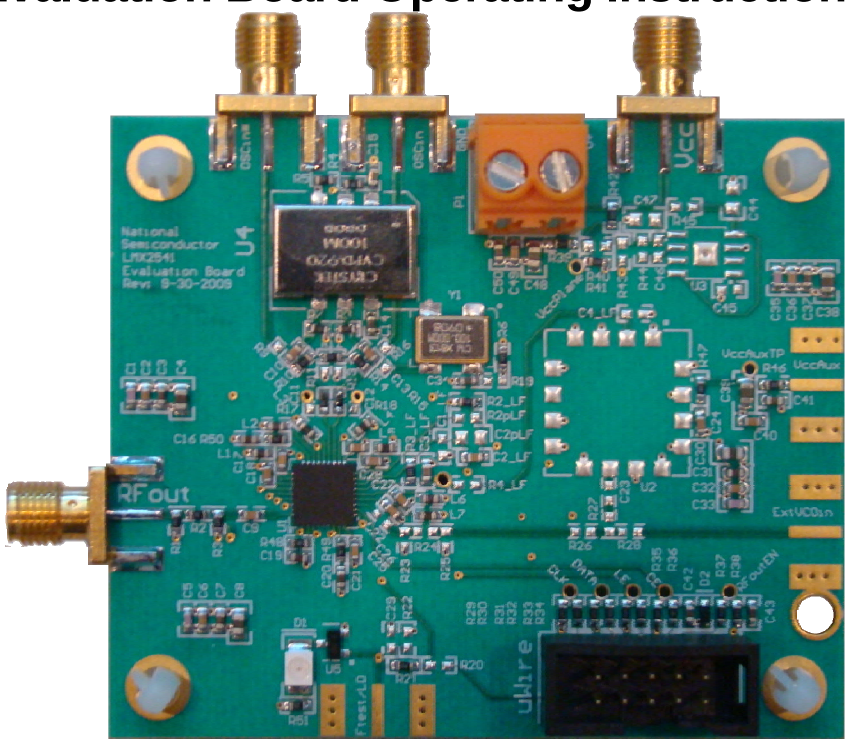
LMX2541 Family

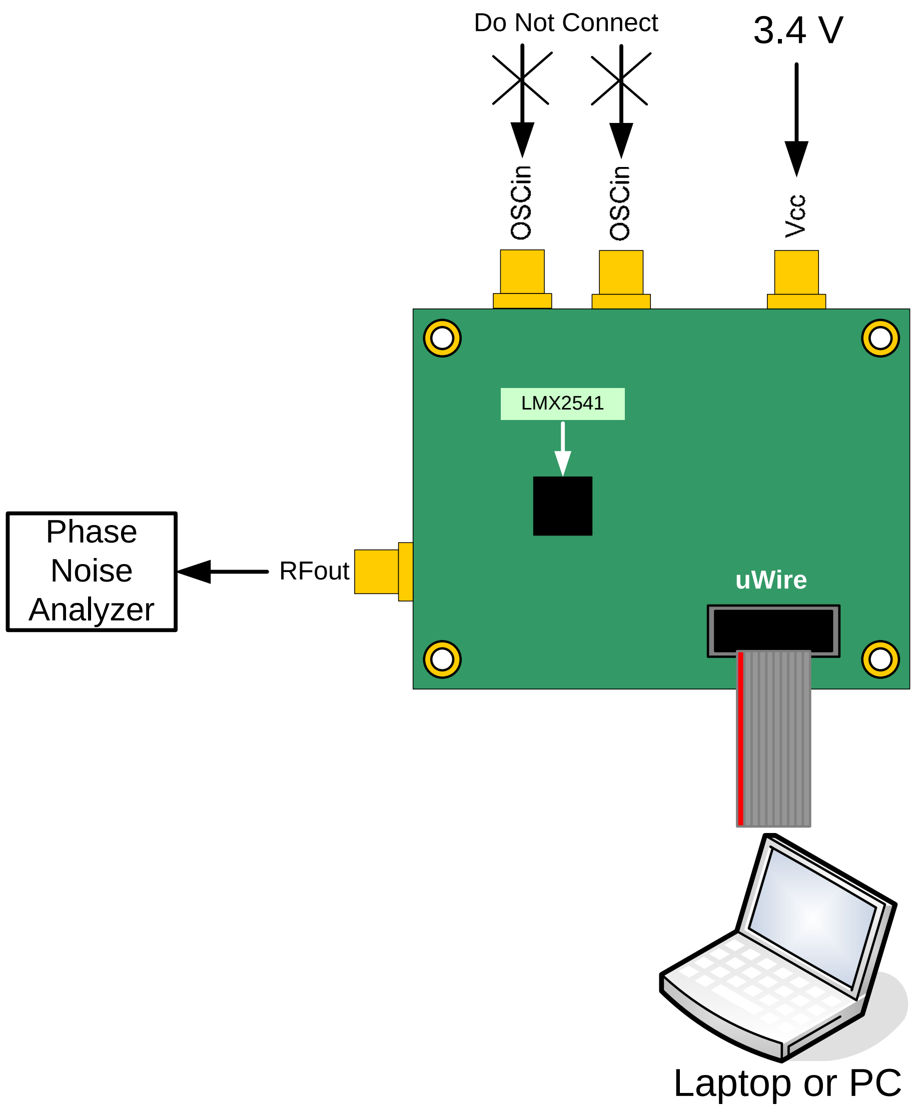
Ultra Low Noise Frequency Synthesizer with Integrated VCO
Evaluation Board Operating Instructions



National Semiconductor Corporation
High Speed Signal Path Division
Precision Timing Devices
12-4-2009

TABLE OF CONTENTS

QUICK SETUP



RFout
Connect to a spectrum analyzer or phase noise analyzer. The Agilent E5052A was used for these instructions.

Vcc
Connect to a 3.4 volt low noise power supply

uWire
Connect to a computer with CodeLoader software

ExtVCOin

This is not used in the default setup, but is included to support the use of an external VCO. In Full Chip Mode, this device has an on-chip VCO.

Ftest/LD

The LED is to ensure that the part is locked. This output can be very useful for diagnostic purposes

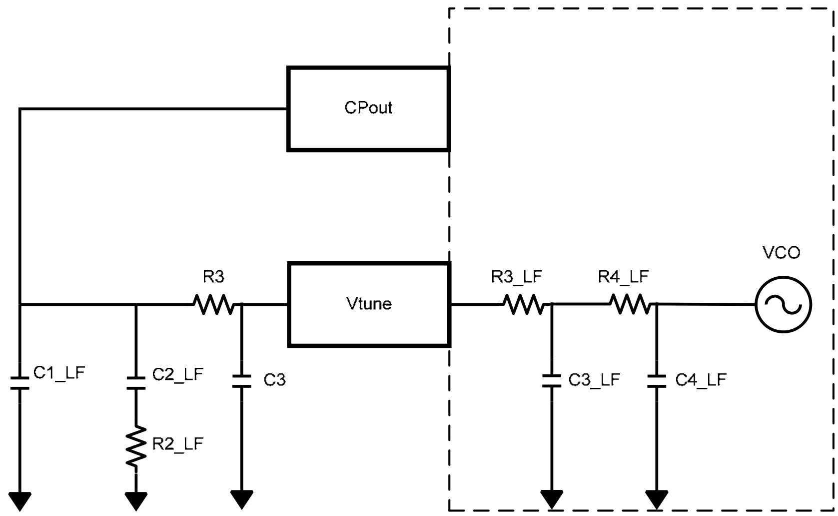
OSCin/OSCin*

This is not used in the default setup, but is included to support the use of an external OSCin signal. The board includes a 100 MHz TCXO, which has two varieties. The OSCin signal is absolutely critical for the phase noise and spur performance of the LMX2541.

Manufacturer	Model	Frequency	Comments
Connor Winfield	CWX-813	100 MHz	• Good phase noise • Low Cost • Drifts a lot.
Crystek	CVPD920	100 MHz	• Good Phase Noise • Drifts much less • High Cost
National Semiconductor	LMK01000 LMK02000 LMK03000 LMK04000	Any	• Eliminate drift issues • Potentially the best phase noise • Best for fractional spurs

Be very aware of the TCXO drift and the contribution that it can have to phase noise. Termination of the TCXO has a large impact on fractional spurs as well. The best results can be achieved by driving this board with an LMK01000 LVPECL output. Doing so results in about a 4 dB spur improvement.

Loop Filter Values

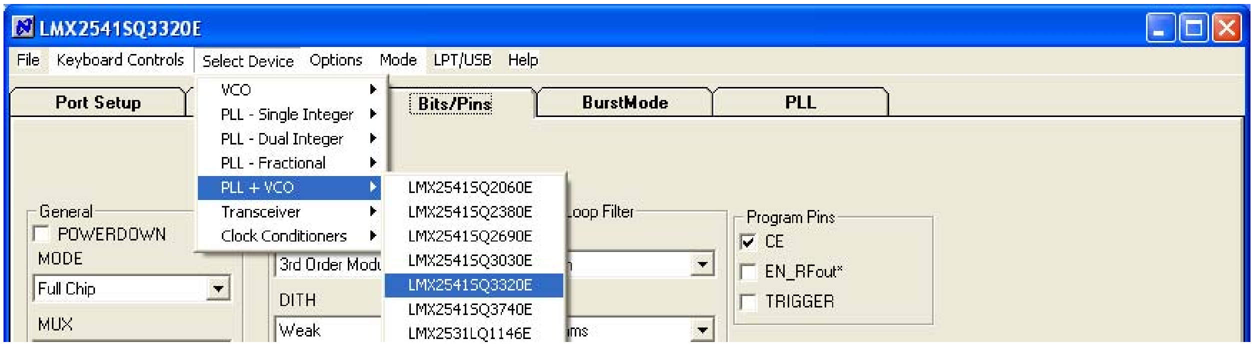


Parameter	LMX2541 SQ2060E	LMX2541 SQ2380E	LMX2541 SQ2690E	LMX2541 SQ3030E	LMX2541 SQ3320E	LMX2541 SQ3470E
VCO Frequency (MHz)	1990 – 2240	2200 - 2530	2490 – 2865	2810 - 3230	3130 - 3600	3480 - 4000
VCO Gain (MHz/V)	13-23	16-30	17-32	20-37	21-37	27 - 42
Charge Pump Gain (mA)	3.2	3.2	3.2	3.2	3.2	3.2
Phase Detector Frequency (MHz)	25	25	25	25	25	25
OSCin Frequency (MHz)	100	100	100	100	100	100
Loop Bandwidth (kHz)	37.3 – 54.6	40.8 – 61.7	38.7 – 58.6	40.0 – 59.9	38.1 – 54.7	43.1 – 55.7
Phase Margin (deg)	52.7 – 52.8	53.1-52	52.9 – 52.4	53.0 – 52.2	52.8 – 52.8	53.2 – 52.7
C1_LF (nF)	2.2	2.2	2.2	2.2	2.2	2.2
C2_LF (nF)	22	22	22	22	22	22
R2_LF (Kohm)	0.47	0.47	0.47	0.47	0.47	0.47
C3_LF (Internal) (nF)	0.02	0.02	0.02	0.02	0.02	0.02
C4_LF (Internal) (nF)	0.1	0.1	0.1	0.1	0.1	0.1
R3_LF (Internal) (Kohm)	1	1	1	1	1	1
R4_LF (Internal) (Kohm)	0.2	0.2	0.2	0.2	0.2	0.2

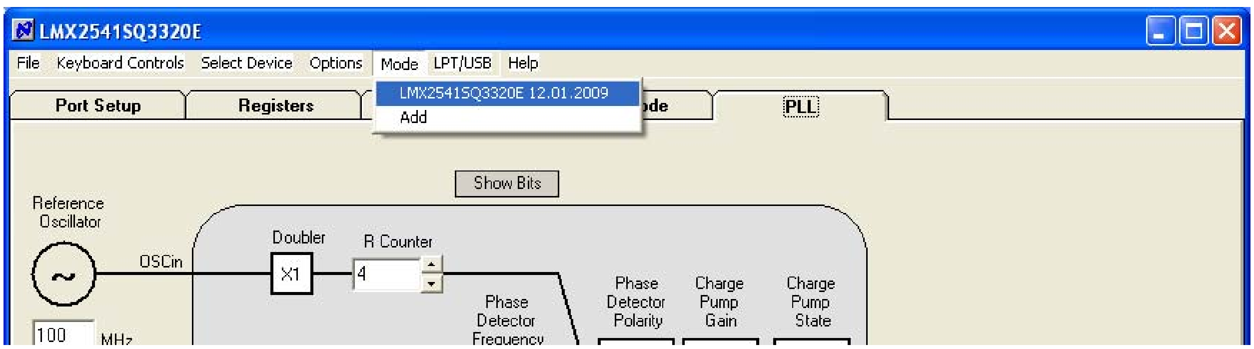
* Note that the VCO gain does change a fair amount. Although not demonstrated in these instructions, the charge pump gain could be adjusted to account for this variation.

CodeLoader Setup

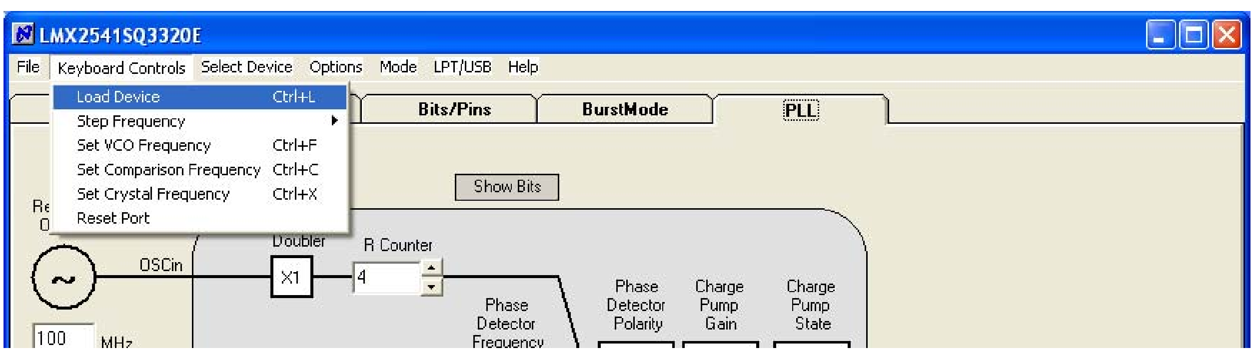
Select the part. In this case, it is the LMX2541SQ3320E.



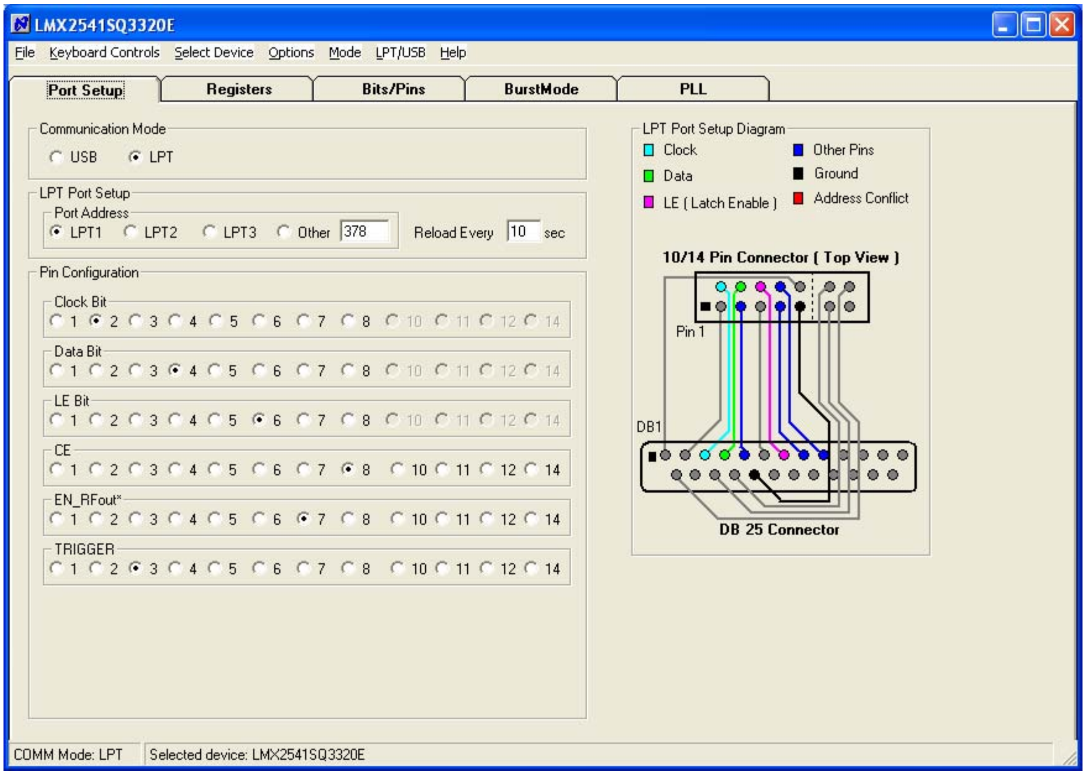
Choose the correct startup mode. This is determined by the part option.



Load the part. You can load it from the menu or also press Cntrl + L.



On the Port Setup tab, the user may select the type of communication port (USB or Parallel) that will be used to program the device on the evaluation board. If parallel port is selected, the user should ensure that the correct port address is entered.

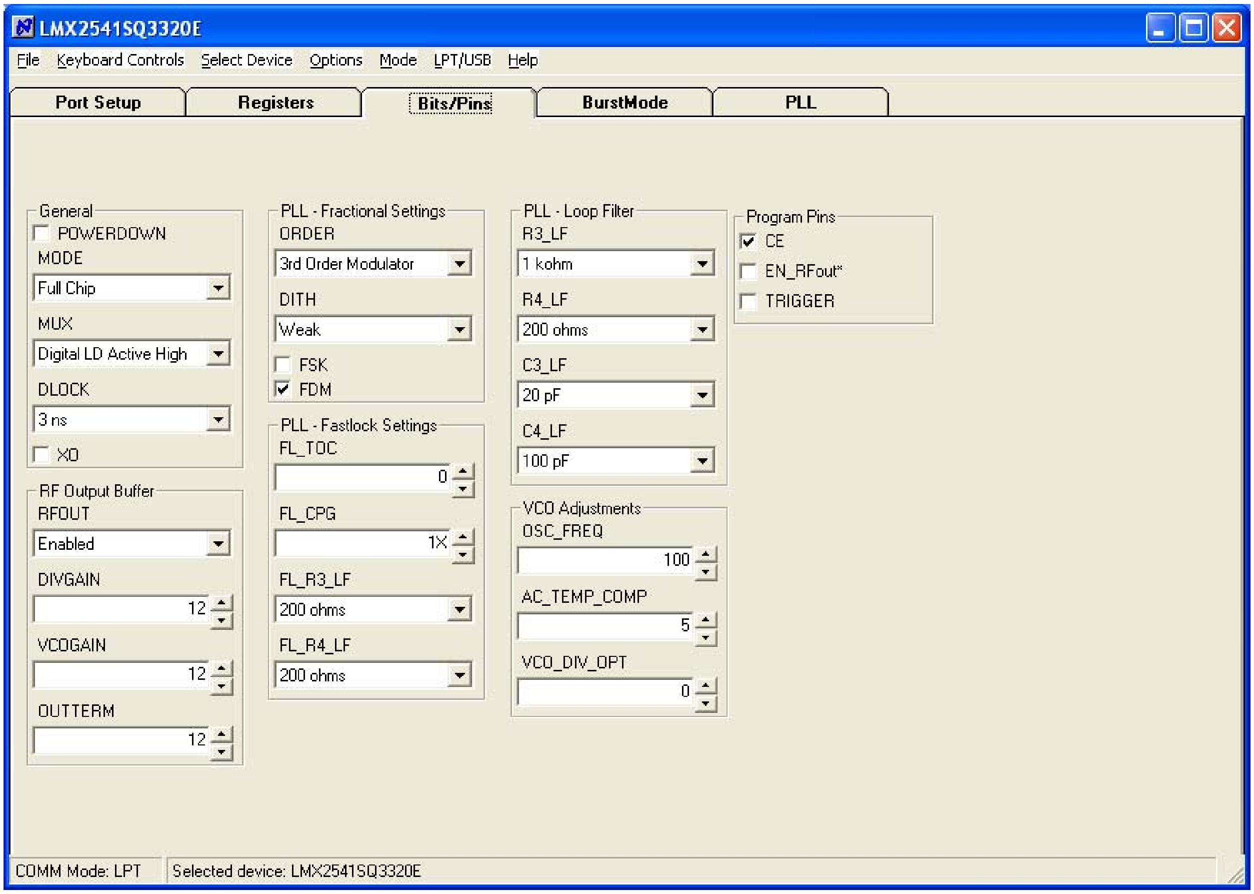


The Pin Configuration field is hardware dependent and normally <u>SHOULD NOT</u> be changed by the user.

The evaluation board is typically shipped with a parallel port cable that is used to interconnect the board to a PC LPT port, enabling the board to be programmed.

Separately available is a USB2UWIRE-IFACE board which simplifies evaluation by enabling the user to establish a USB connection from the Codeloader 4 software to the evaluation board.
http://www.national.com/store/view_item/index.html?nsid=USB2UWIRE-IFACE

To view the function of any bit on the CodeLoader configuration tabs, place the cursor over the desired bit register label and click the right mouse button on it for a description. This Bits/Pins configuration is common to all options of the LMX2541 evaluation board.

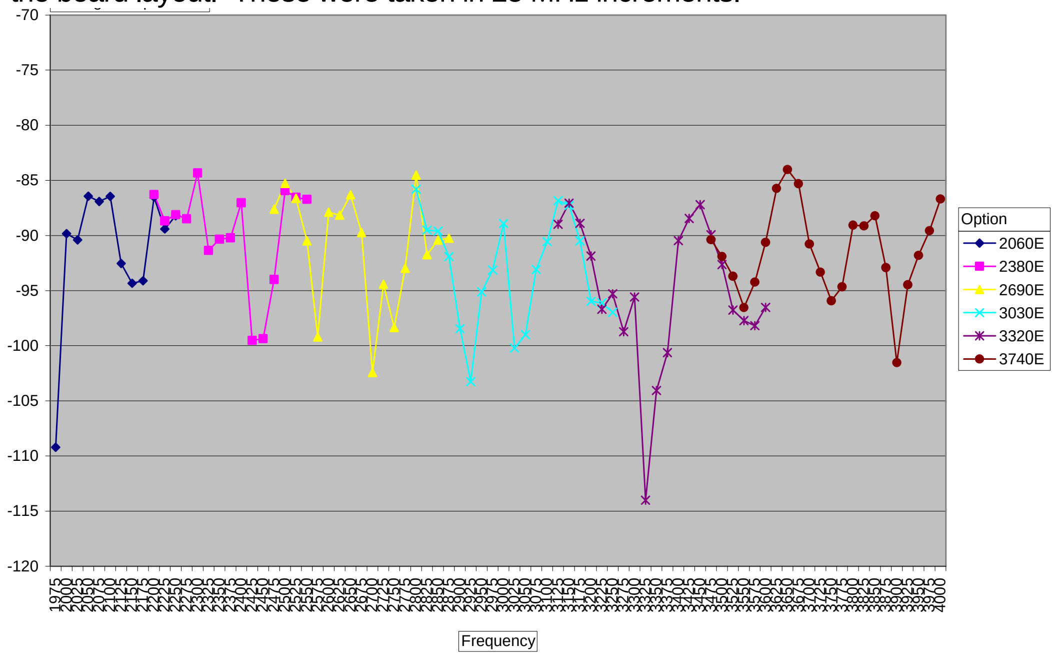


LMX2541SQ3320E
File Keyboard Controls Select Device Options Mode LPT/USB Help
Port Setup
Registers
Bits/Pins
BurstMode
PLL
General
POWERDOWN
MODE
Full Chip
MUX
Digital LD Active High
DLOCK
3 ns
XO
RF Output Buffer
RFOUT
Enabled
DIVGAIN
12
VCOGAIN
12
OUTTERM
12
PLL - Fractional Settings
ORDER
3rd Order Modulator
DITH
Weak
FSK
FDM
PLL - Fastlock Settings
FL_TOC
0
FL_CPG
1X
FL_R3_LF
200 ohms
FL_R4_LF
200 ohms
PLL - Loop Filter
R3_LF
1 kohm
R4_LF
200 ohms
C3_LF
20 pF
C4_LF
100 pF
VCO Adjustments
OSC_FREQ
100
AC_TEMP_COMP
5
VCO_DIV_OPT
0
Program Pins
CE
EN_RFout*
TRIGGER
COMM Mode: LPT
Selected device: LMX2541SQ3320E

Spurs

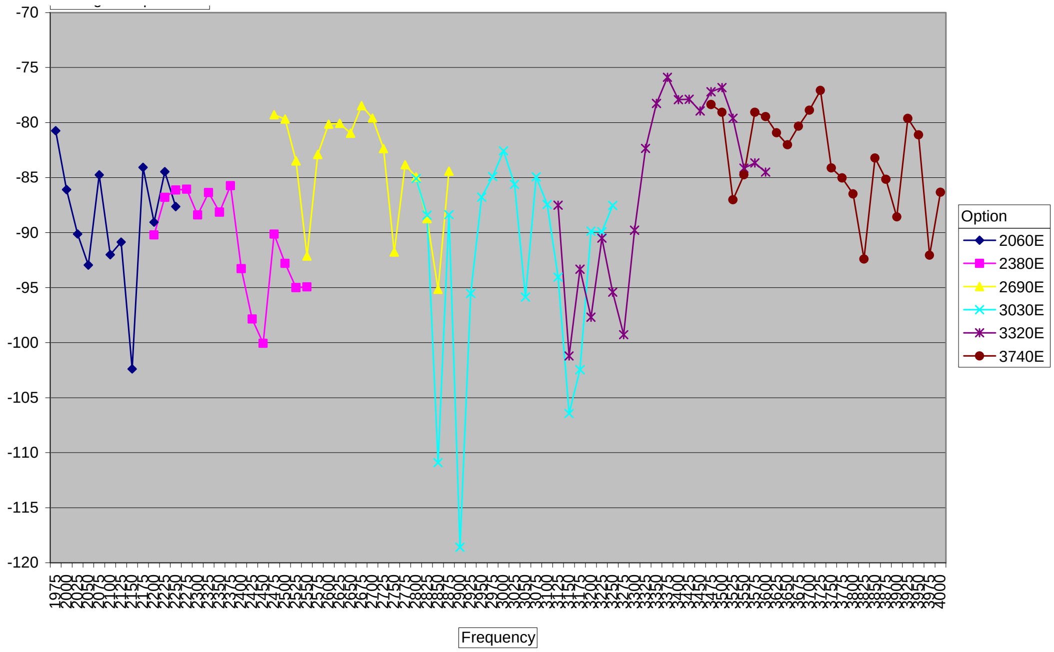
Oscillator Spurs

Oscillator spurs occur at the oscillator frequency (100 MHz) offset from the carrier. They can be largely impacted by the board layout. These were taken in 25 MHz increments.



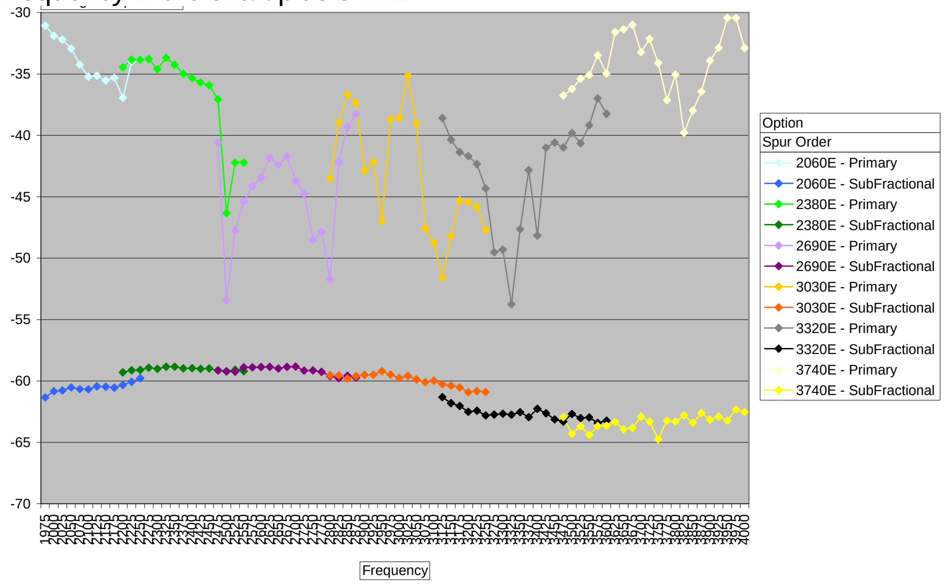
Reference (Phase Detector) Spurs

Reference spurs occur at a multiple of the phase detector frequency (25 MHz) from the carrier

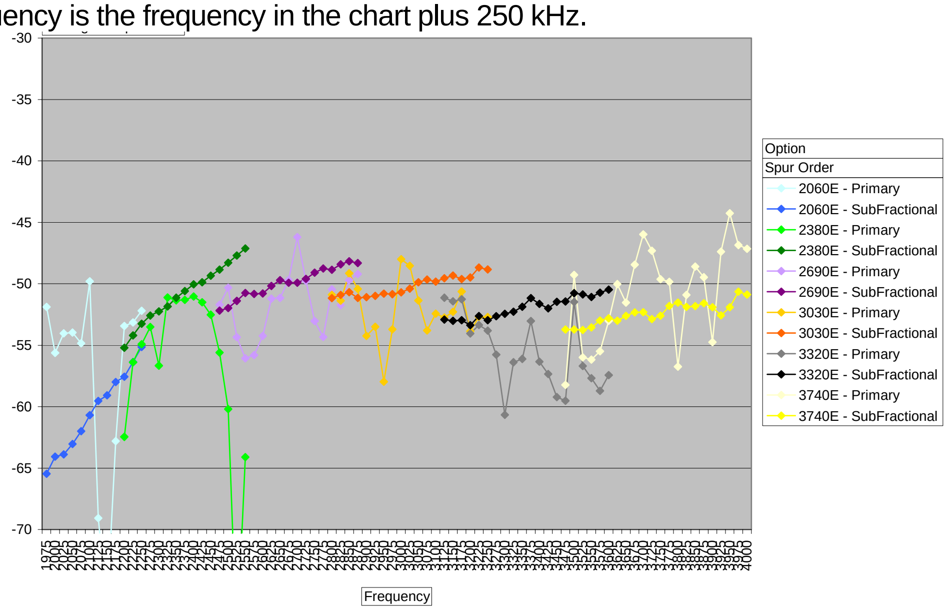


Fractional Spurs

In-band spurs occur inside the loop bandwidth. These spurs were measured with a WORST CASE fraction of 1/5000. The primary fractional spurs are at 5 kHz and the sub-fractional spurs are at 2.5 kHz. The actual frequency is the frequency in the chart plus 5 kHz.



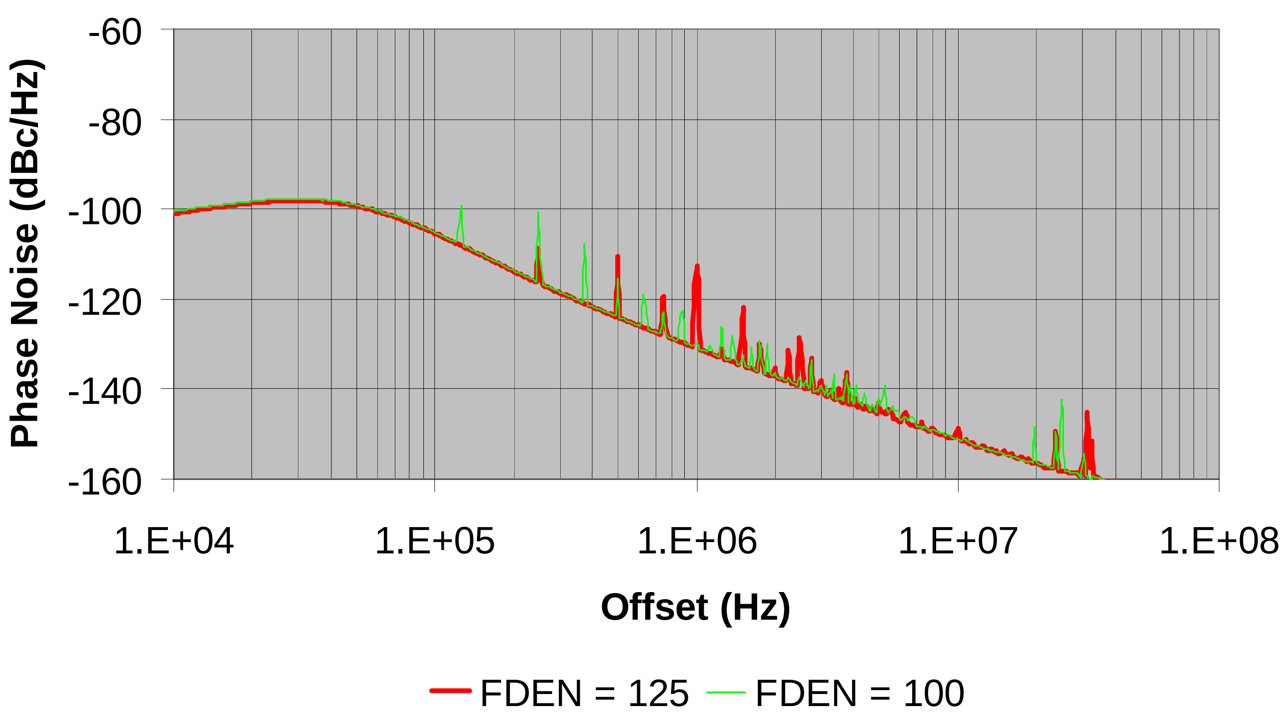
Out-band spurs occur inside the loop bandwidth. These spurs were measured with a WORST CASE fraction of 1/100. The primary fractional spurs are at 250 kHz and the sub-fractional spurs are at 125 kHz. The actual frequency is the frequency in the chart plus 250 kHz.



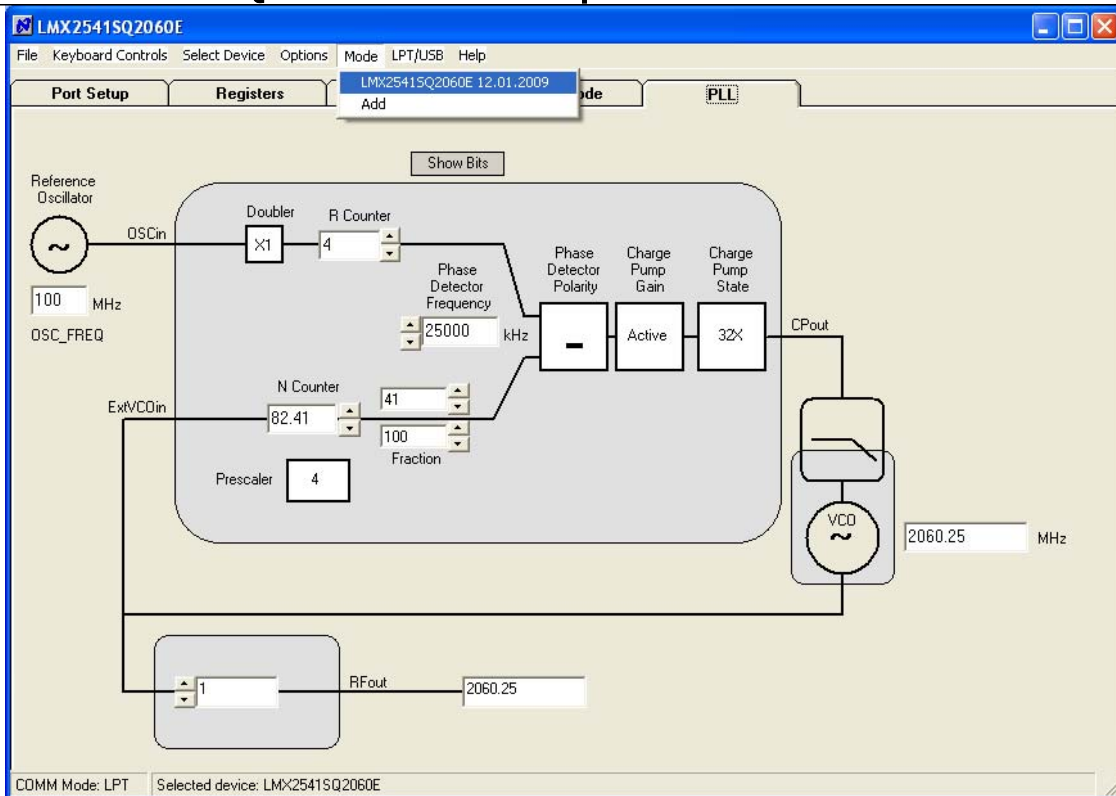
Minimizing Fractional Spurs

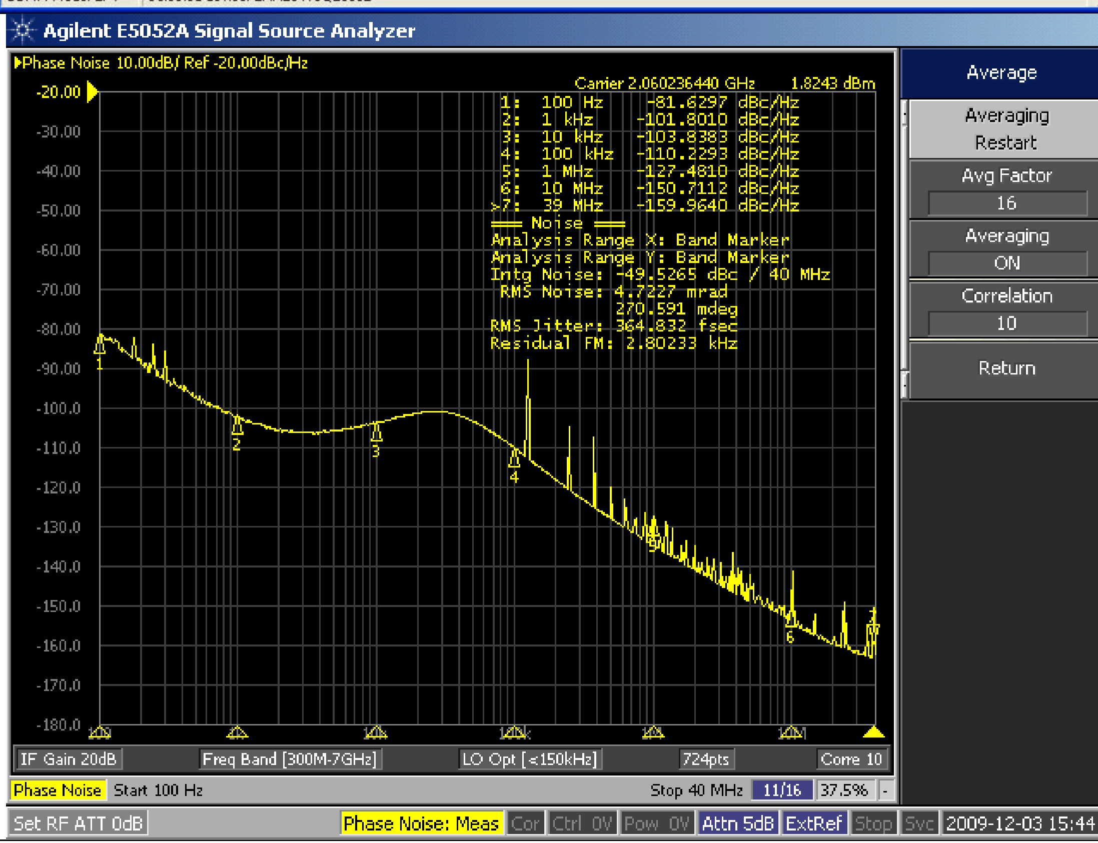
- Both fractional and sub-fractional spurs are highly sensitive to the OSCin signal. Higher slew rates are desired. Also, the termination makes a big difference. For this evaluation board, a series 120 ohm resistor had a large impact.
- The best results have been achieved when driving the part differentially with an LVPECL output of the LMK01000/2000/3000/400 series of clock conditioner devices from National Semiconductor.
- The spurs on this evaluation board are relatively high because the loop bandwidth is very wide. This wide loop bandwidth takes advantage of the close-in phase noise, but it does expose the fractional spurs more. The fractional spurs can be reduced by orders of magnitude by reducing the loop bandwidth. This requires a re-design of the loop filter.
- To eliminate the SubFractional spurs entirely, choose a fractional denominator with no factors of 2 or 3. For this 100 MHz TCXO and 250 kHz channel spacing, a phase detector frequency of 6.25 MHz and a fractional denominator of 25 would work. However, the higher N value does degrade the phase noise. An ideal scenario would be to use a TCXO frequency of something like 125 MHz. Then the sub-fractional spurs are eliminated if the phase detector is chosen to be 30.25 MHz and the fractional denominator is chosen to be 125.

  In the plot below, one was taken with the default 100 MHz TCXO and another was taken with a 125 MHz signal. The phase detector frequency was changed to 31.25 MHz, but the charge pump gain was reduced to 26X to compensate for this. This is the same part, board, and frequency (3030.25 MHz). Although the fraction is different, notice that the fractional denominator of 125 has no sub fractional spurs at 125 kHz, 375 kHz, and so on. An LMK01000 evaluation board driven by a 1250 MHz signal was used to produce this 125 MHz signal.

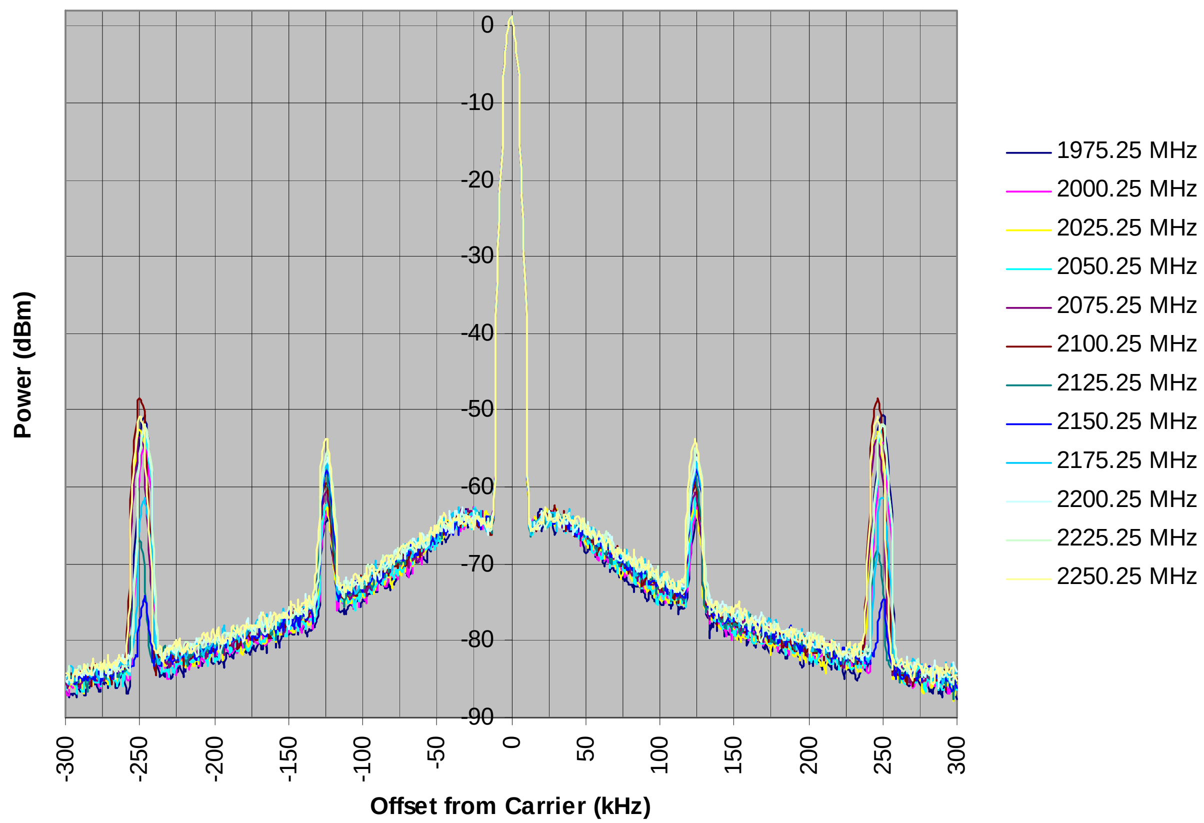


LMX2541SQ2060E Default Setup and Measured Performance



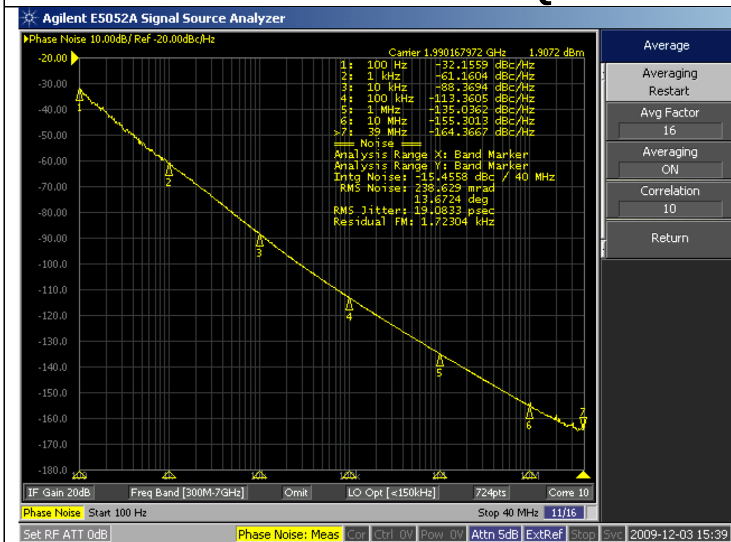


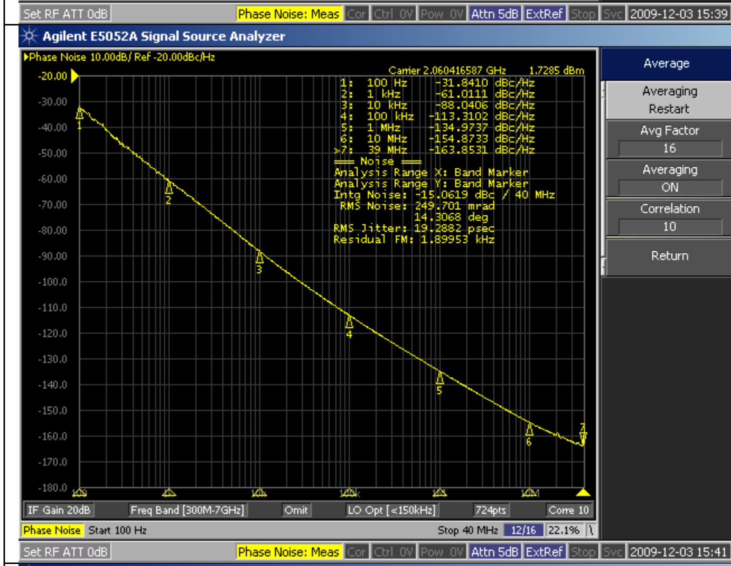
LMX2541SQ2060E Spurs for WORST CASE Channels (Fraction = 1/100)

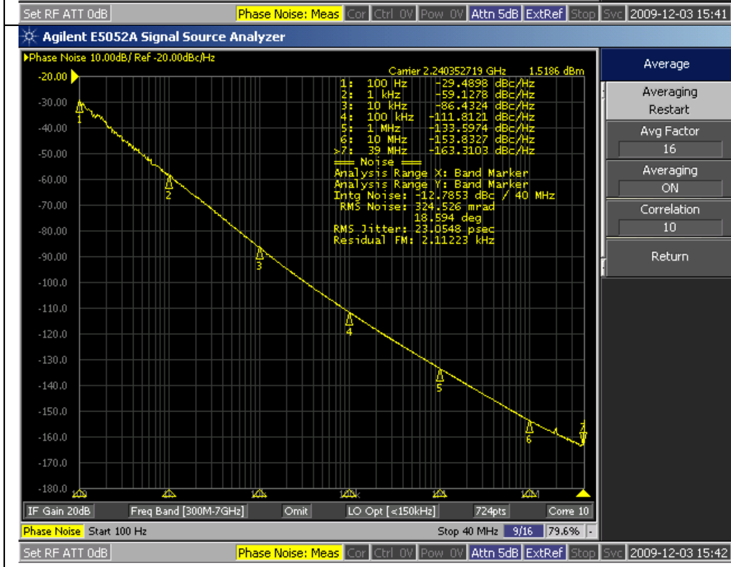


This graph has been normalized to the average carrier power.

LMX2541SQ2060E VCO Phase Noise



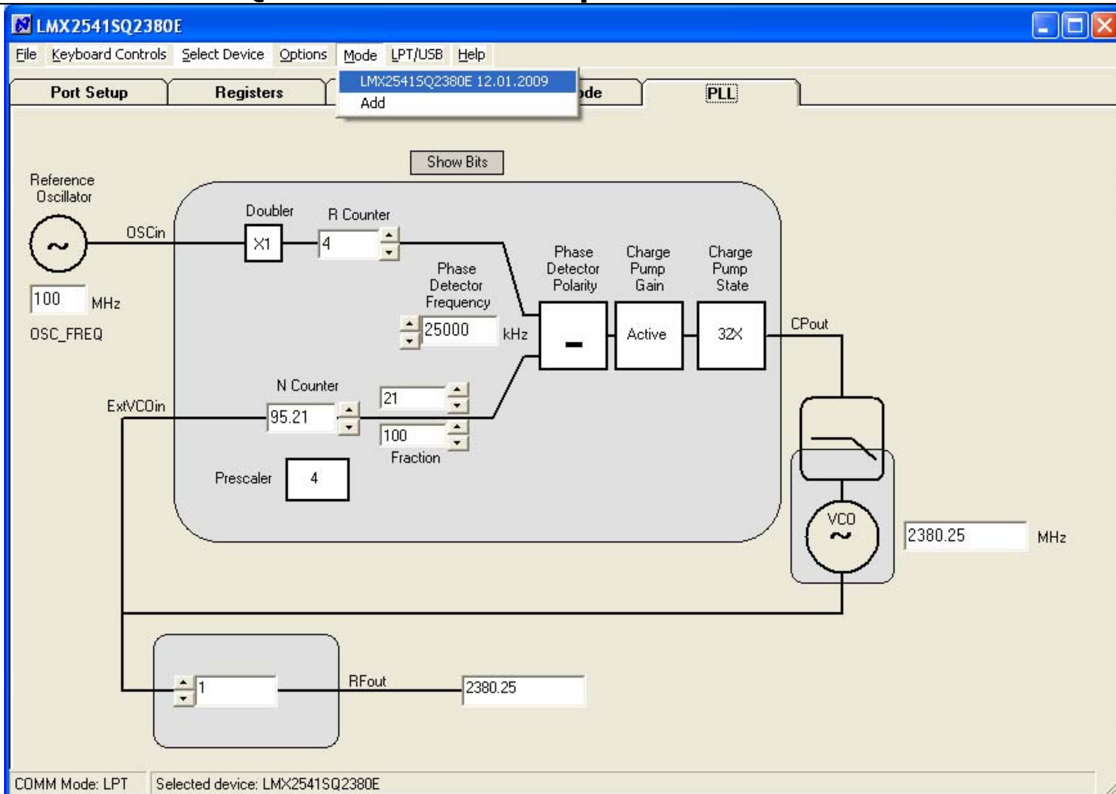


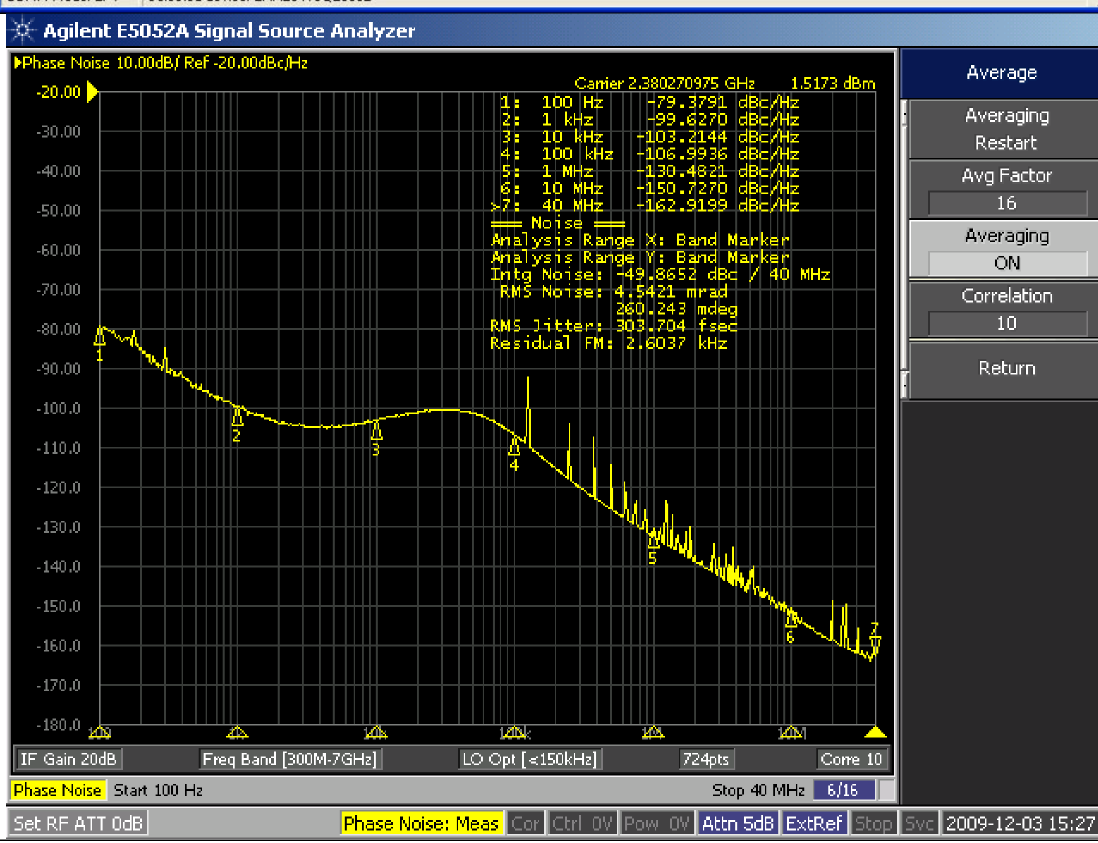


The plots show the VCO phase noise at low, middle, and high frequency.

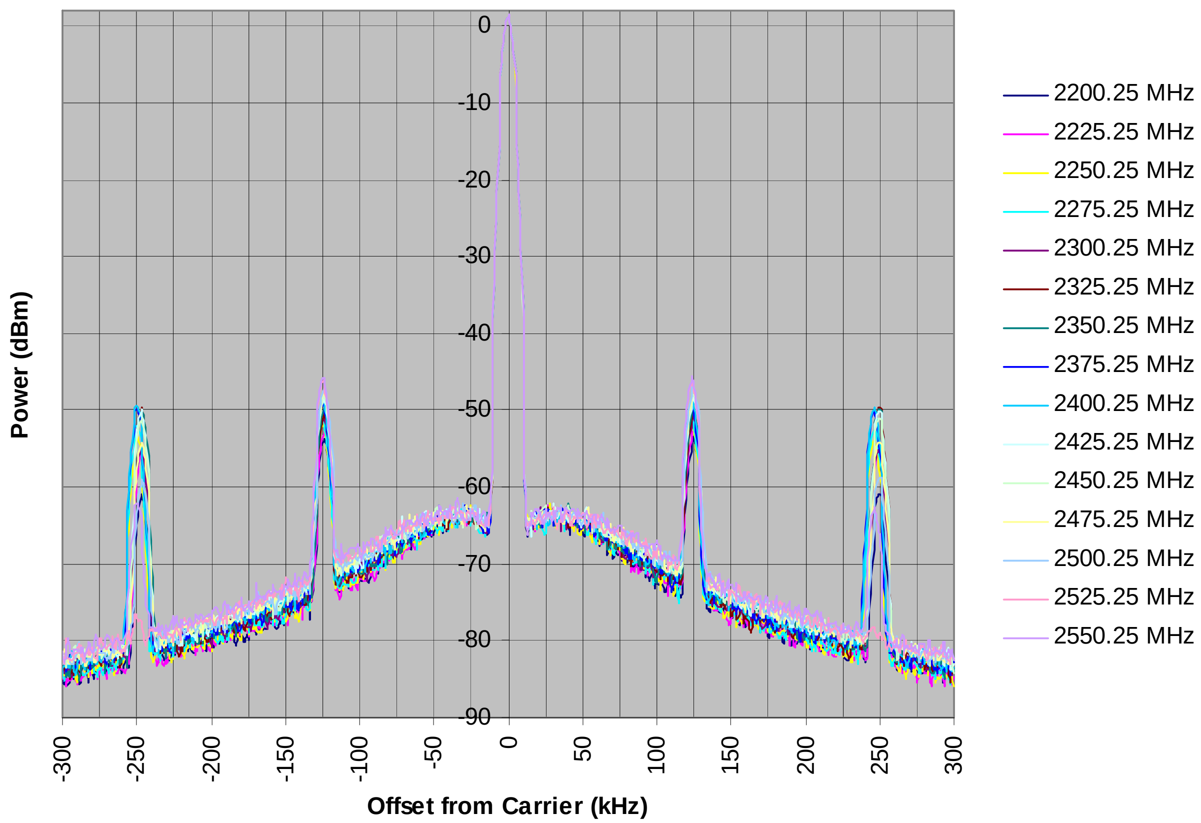
To measure the VCO phase noise, a simple technique is to lock the PLL to the desired frequency and set the charge pump state to "Tri-State", by clicking this on the PLL tab on Codeloader. If the phase noise analyzer can track the signal, a reasonable measurement can be made. To ensure that this measurement is of the VCO noise, omit the the spurs and disconnect the microwire programming cable.

LMX2541SQ2380E Default Setup and Measured Performance



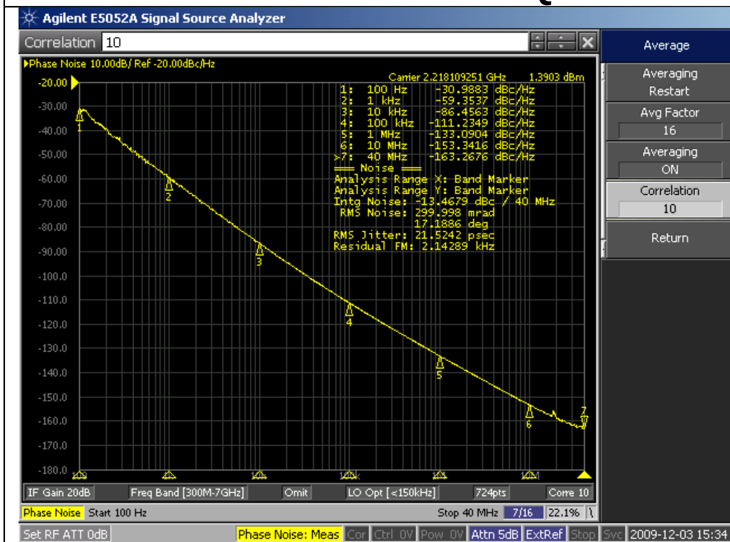


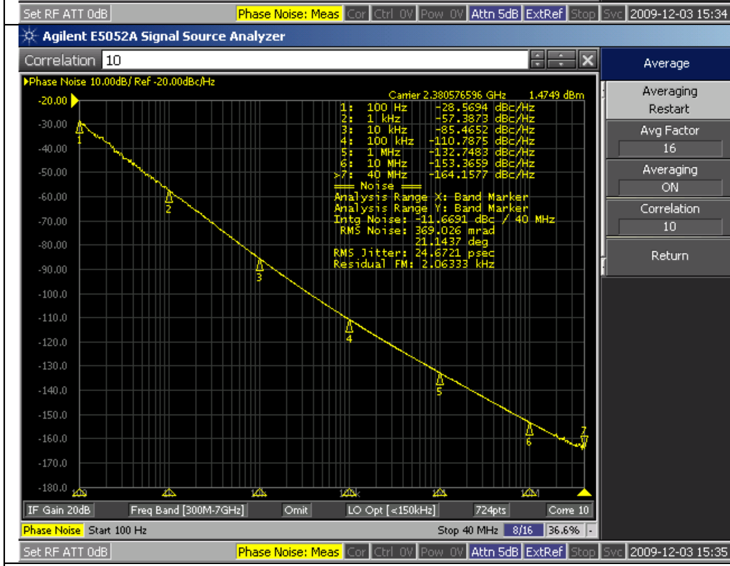
LMX2541SQ2380E Spurs for WORST CASE Channels
(Fraction = 1/100)

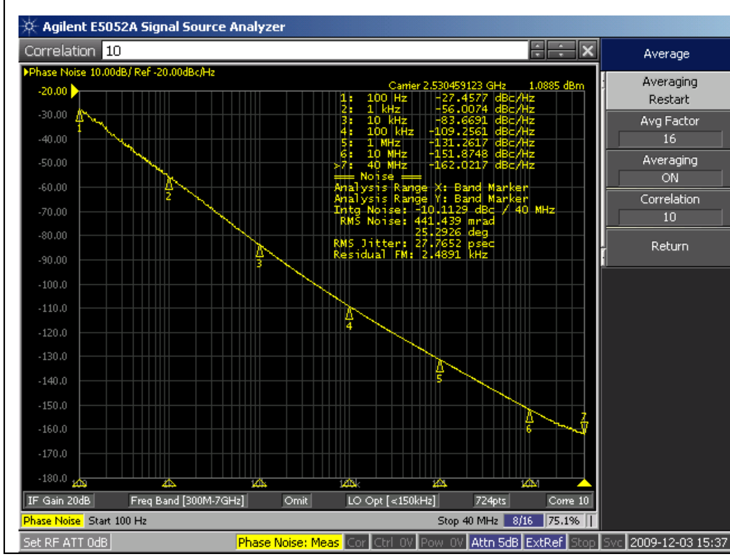


This graph has been normalized to the average carrier power.

LMX2541SQ2380E VCO Phase Noise



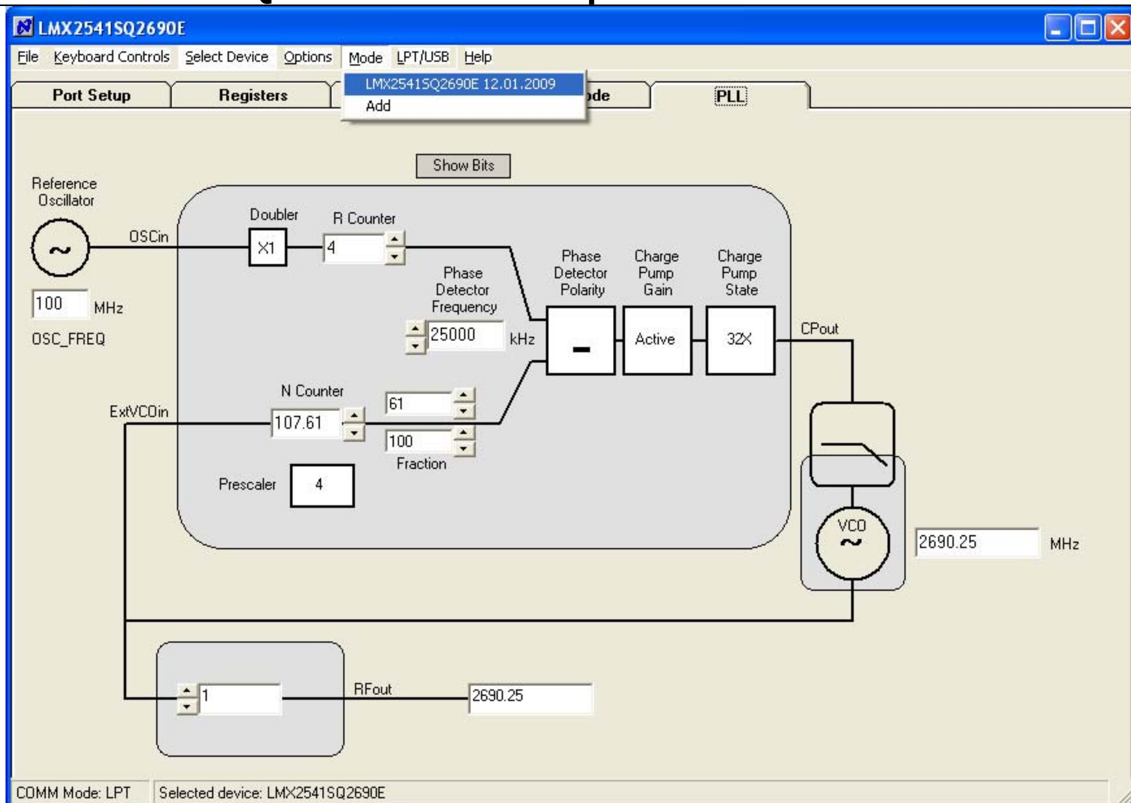


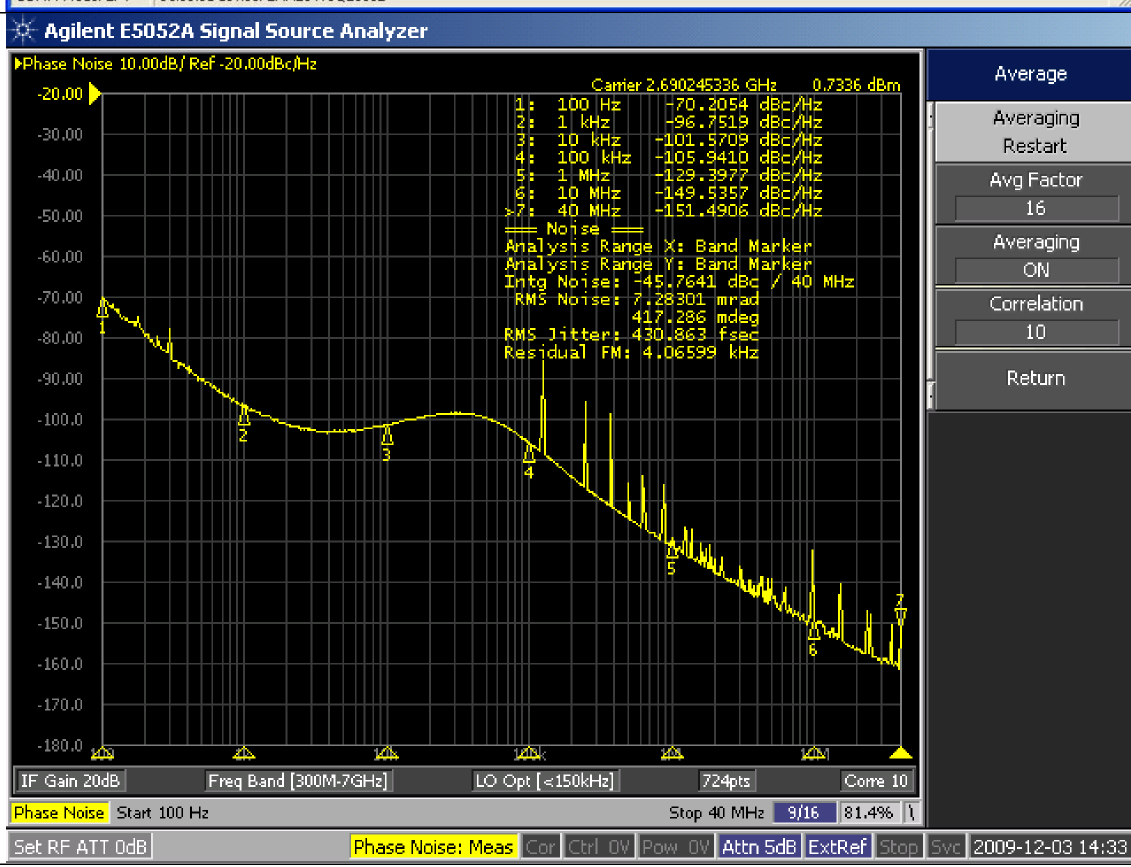


The plots show the VCO phase noise at low, middle, and high frequency.

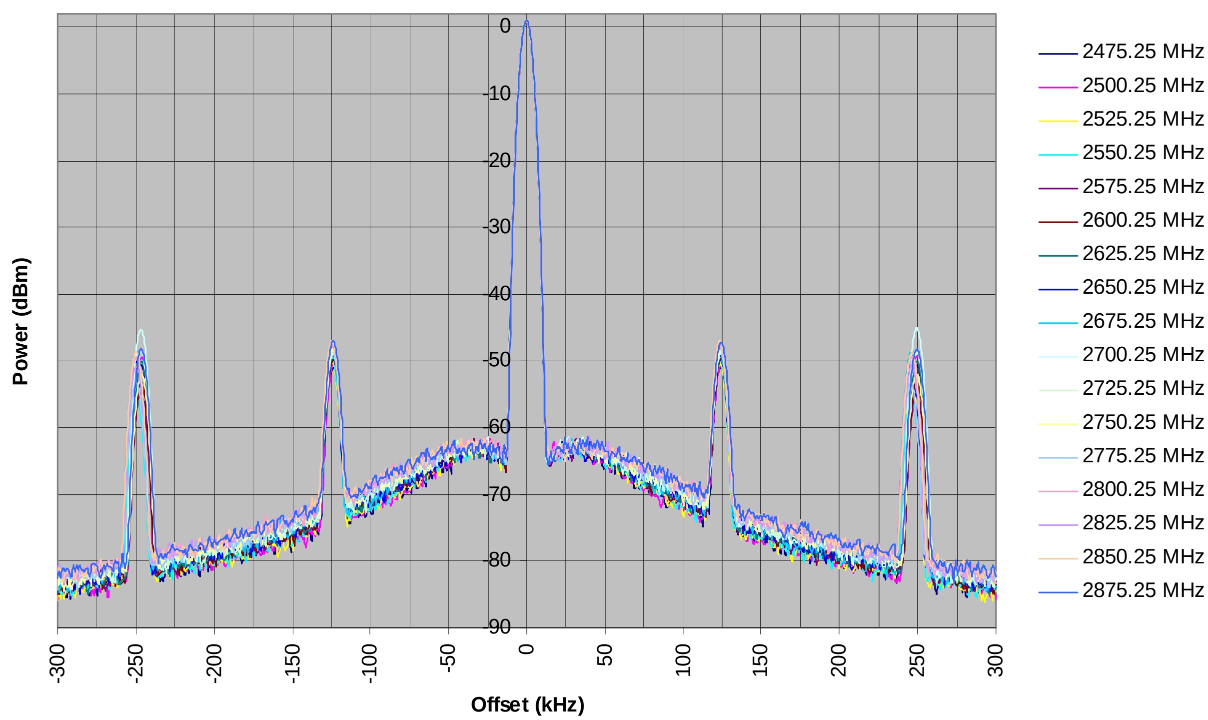
To measure the VCO phase noise, a simple technique is to lock the PLL to the desired frequency and set the charge pump state to “Tri-State”, by clicking this on the PLL tab on Codeloader. If the phase noise analyzer can track the signal, a reasonable measurement can be made. To ensure that this measurement is of the VCO noise, omit the the spurs and disconnect the microwire programming cable.

LMX2541SQ2690E Default Setup and Measured Performance



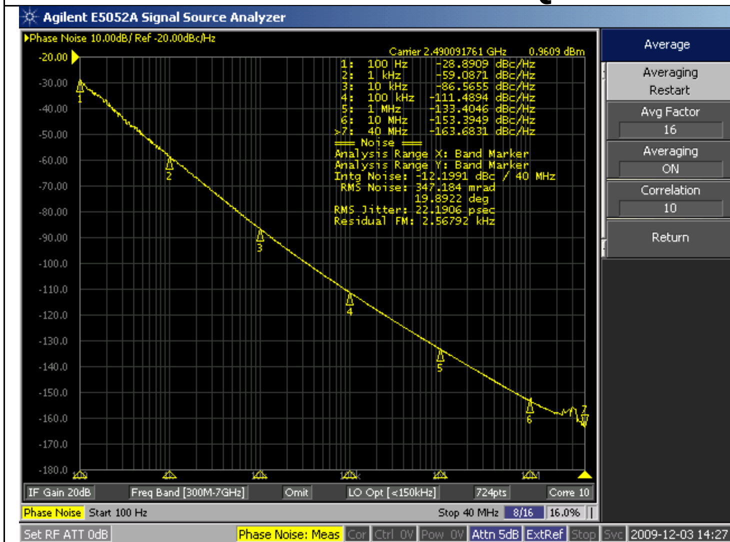


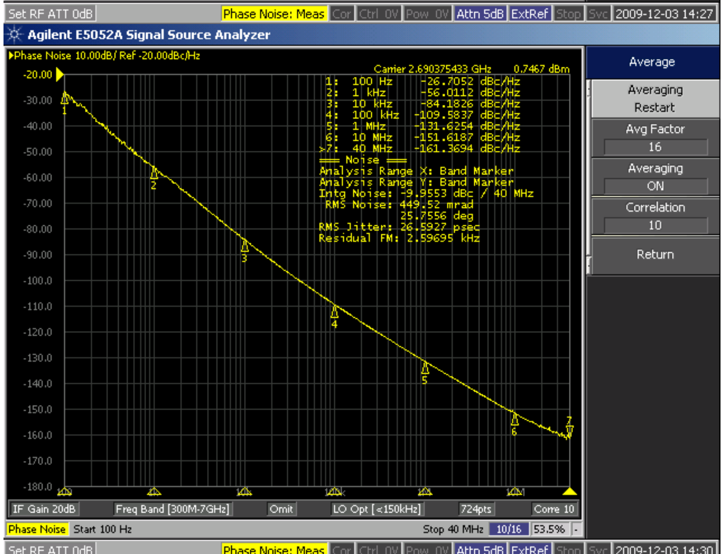
LMX2541SQ2690E Spurs for WORST CASE Channels
(Fraction = 1/100)

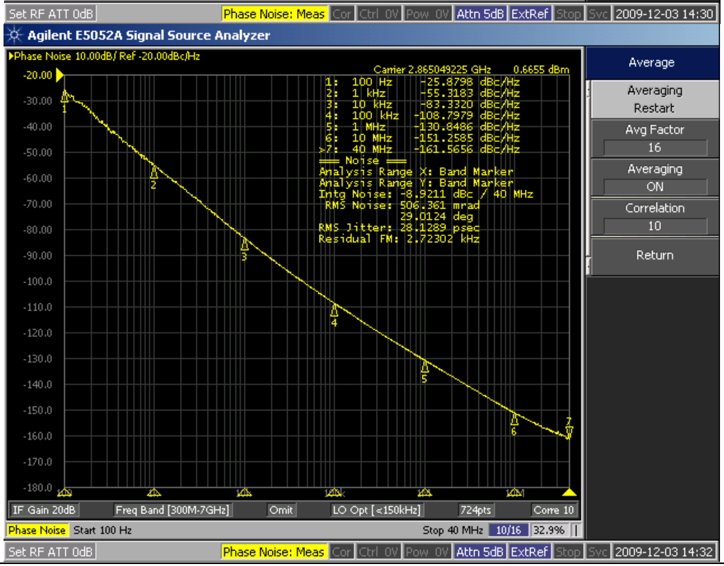


This graph has been normalized to the average carrier power.

LMX2541SQ2690E VCO Phase Noise



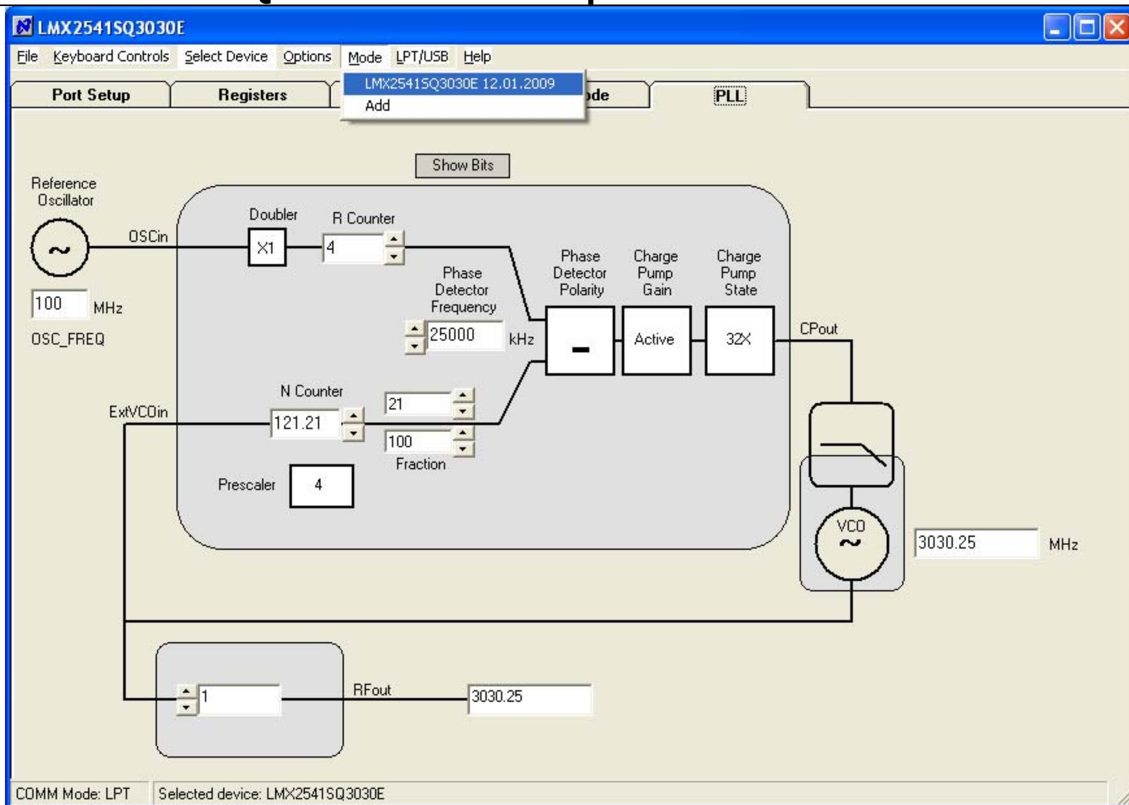


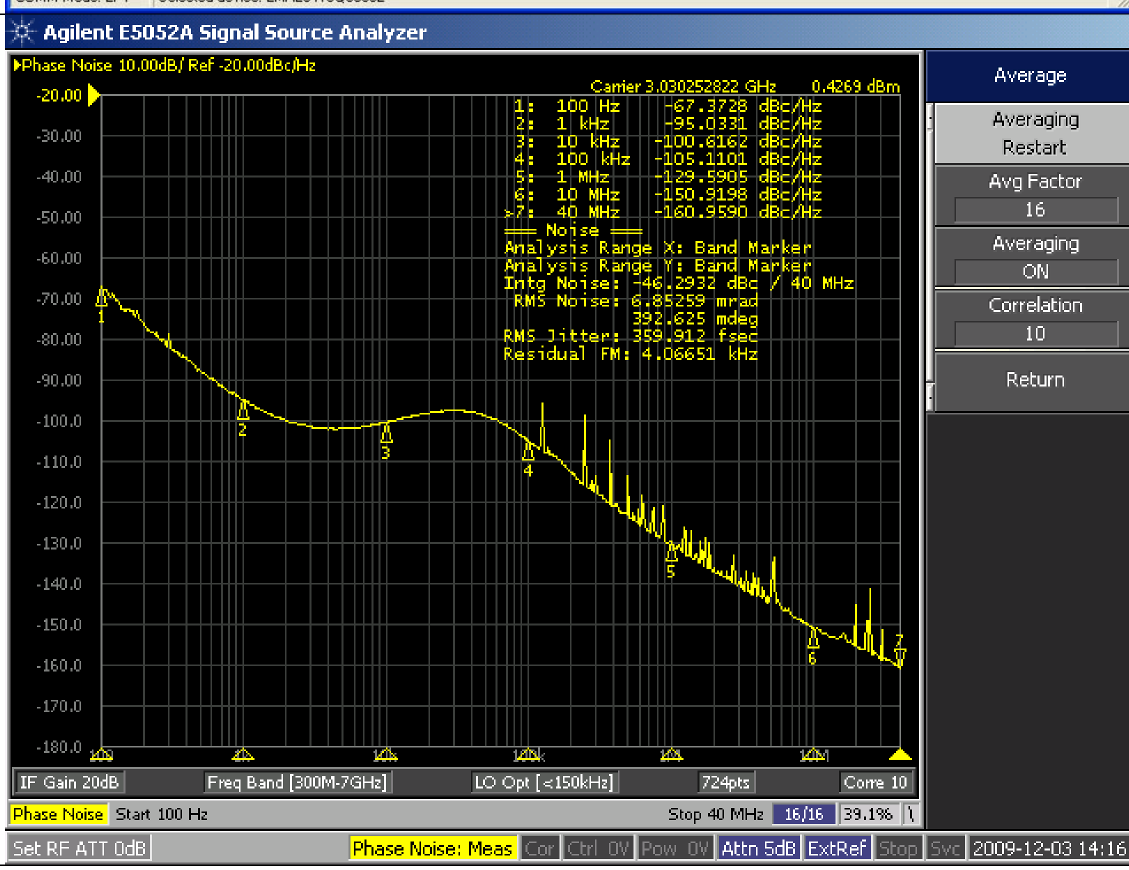


The plots show the VCO phase noise at low, middle, and high frequency.

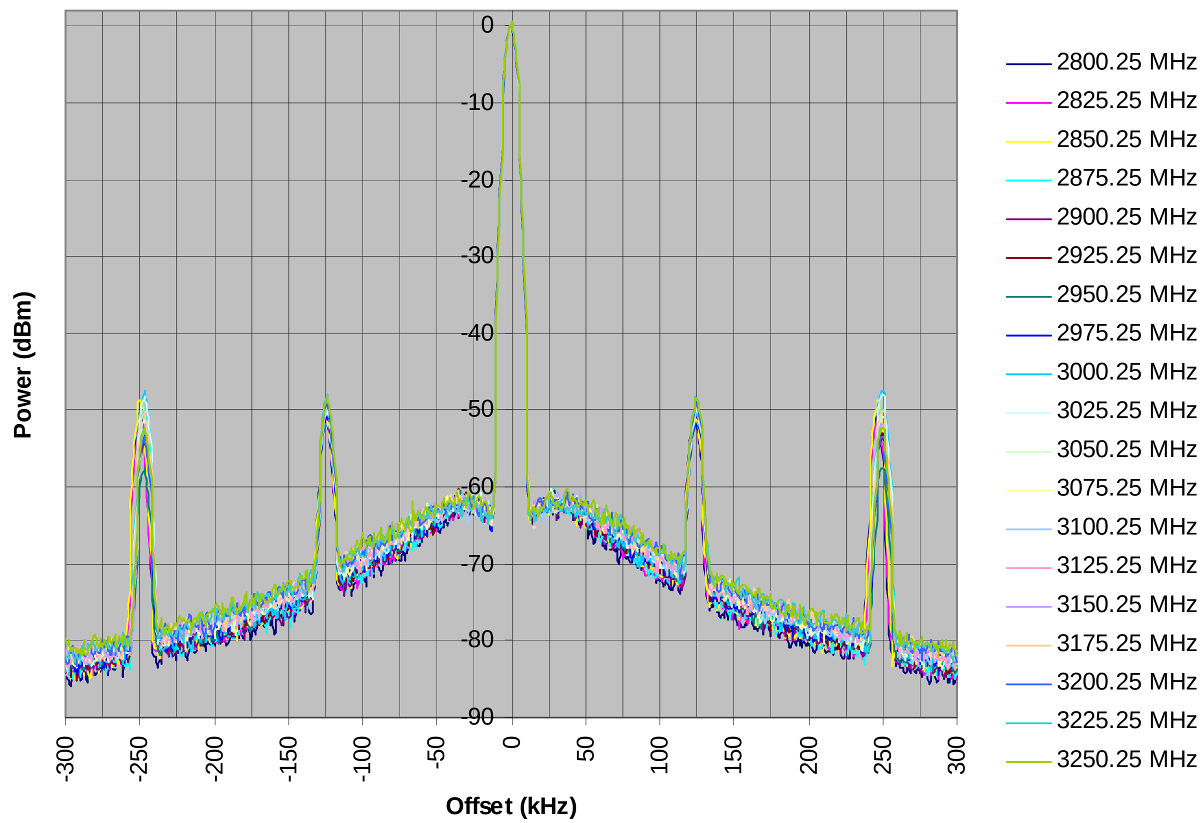
To measure the VCO phase noise, a simple technique is to lock the PLL to the desired frequency and set the charge pump state to “Tri-State”, by clicking this on the PLL tab on Codeloader. If the phase noise analyzer can track the signal, a reasonable measurement can be made. To ensure that this measurement is of the VCO noise, omit the the spurs and disconnect the microwire programming cable.

LMX2541SQ3030E Default Setup and Measured Performance



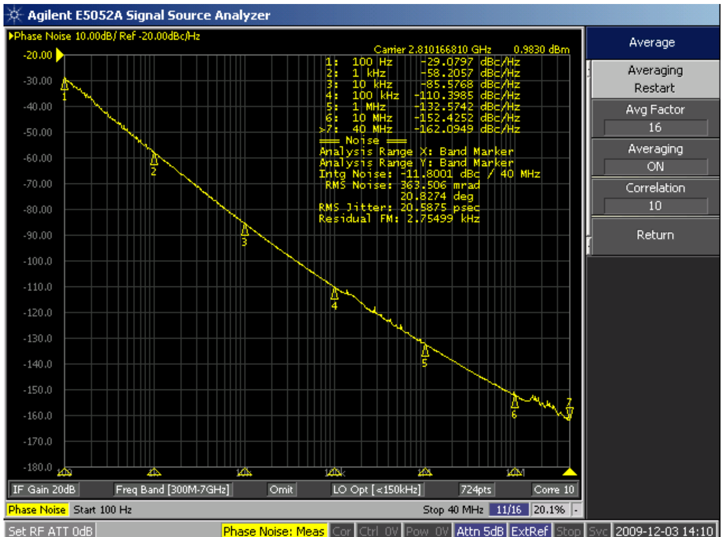


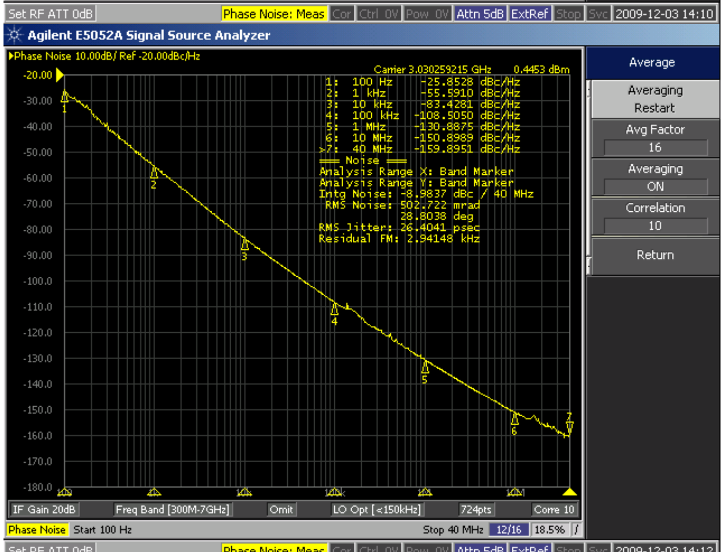
LMX2541S3030E Spurs for WORST CASE Channels (Fraction = 1/100)

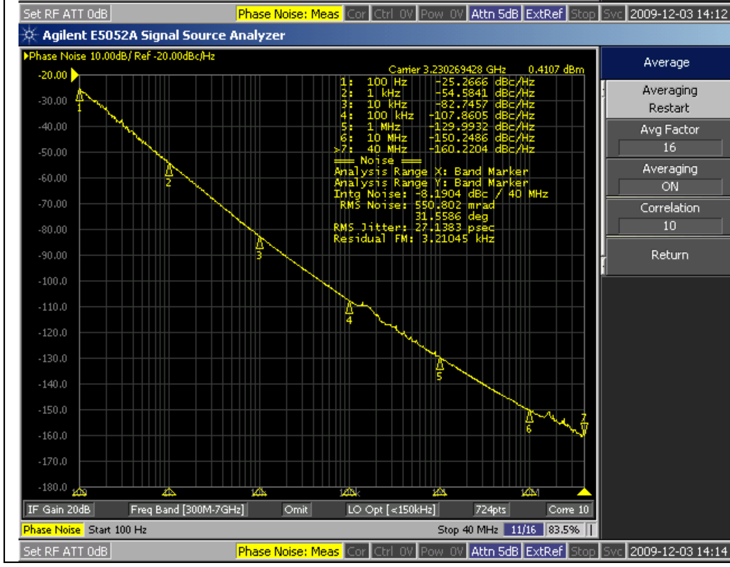


This graph has been normalized the average carrier power.

LMX2541SQ3030E VCO Phase Noise



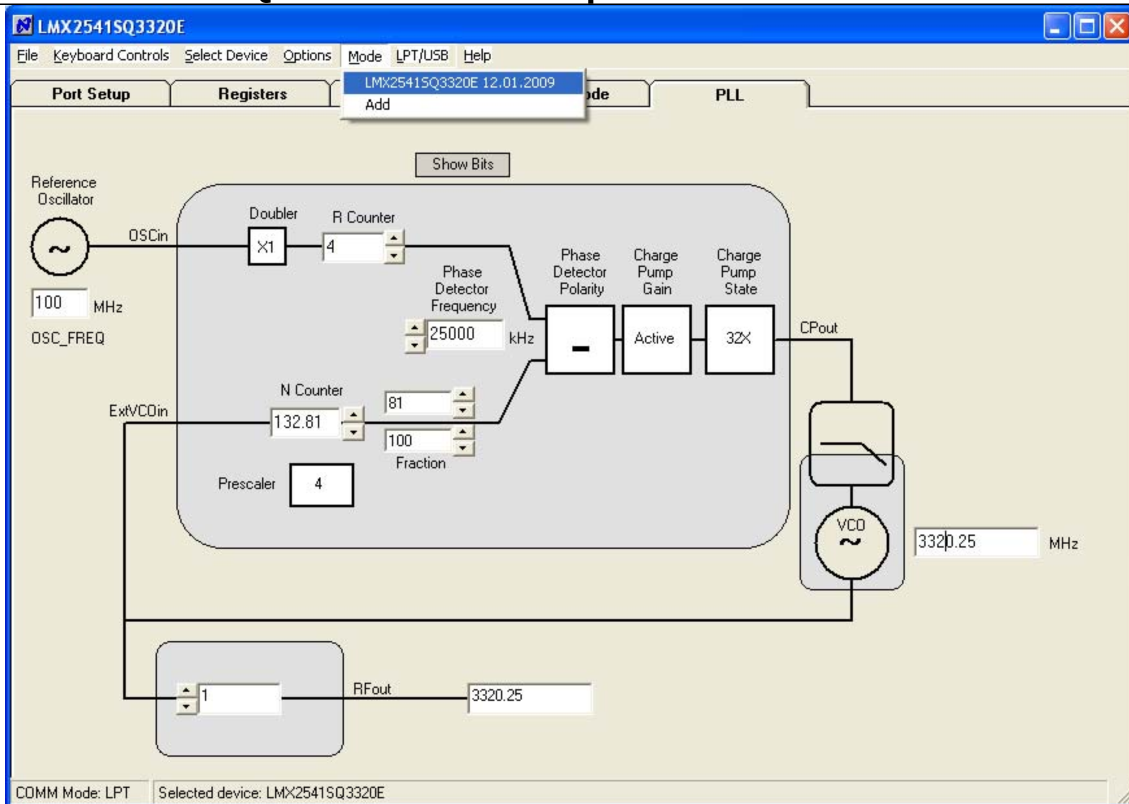


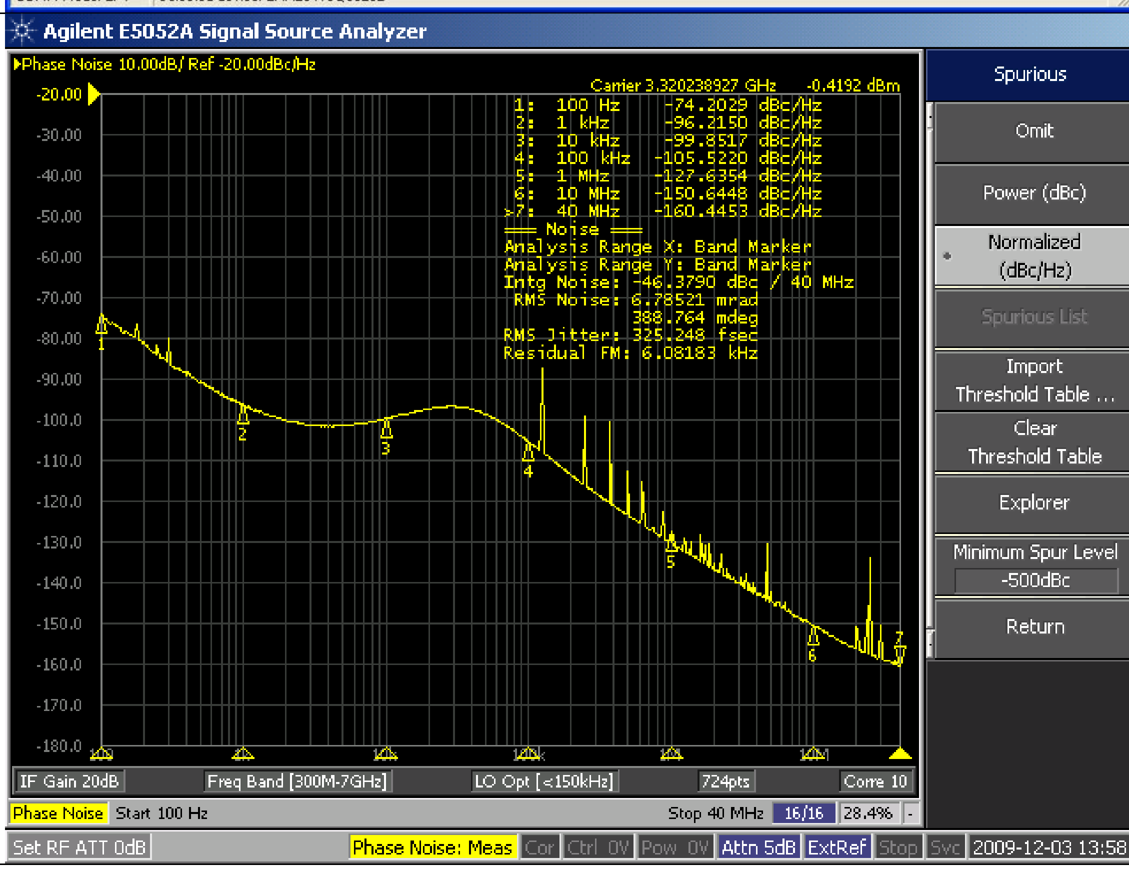


The plots show the VCO phase noise at low, middle, and high frequency.

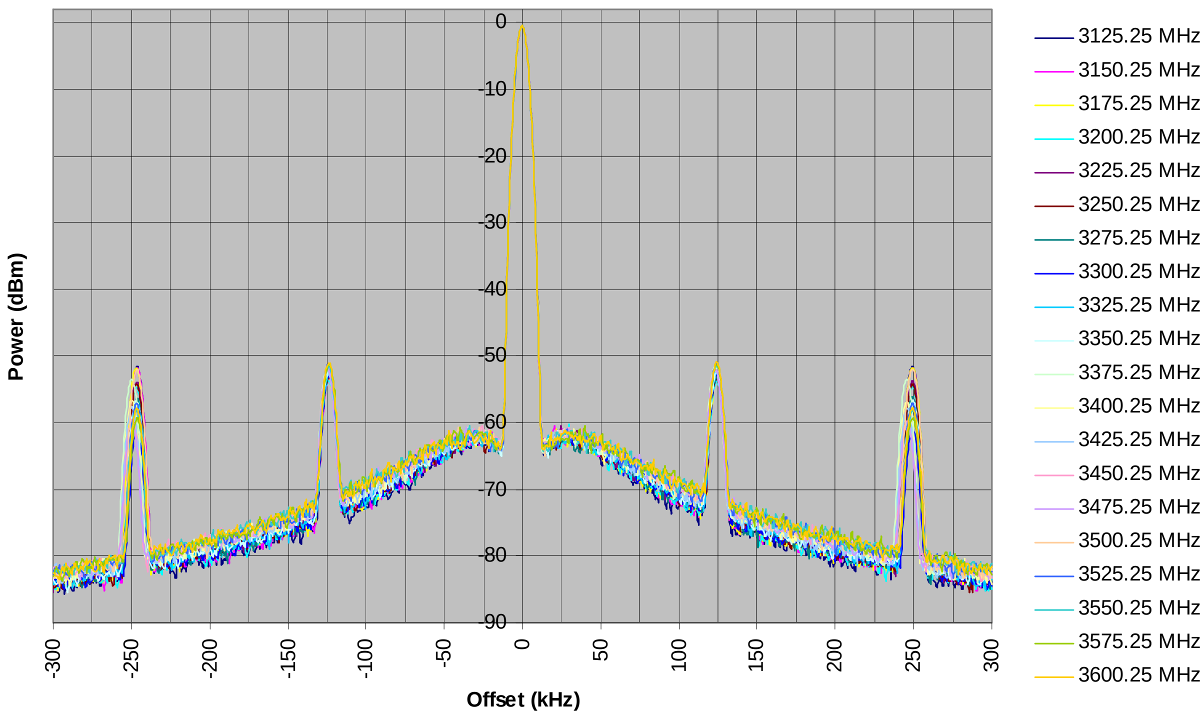
To measure the VCO phase noise, a simple technique is to lock the PLL to the desired frequency and set the charge pump state to “Tri-State”, by clicking this on the PLL tab on Codeloader. If the phase noise analyzer can track the signal, a reasonable measurement can be made. To ensure that this measurement is of the VCO noise, omit the the spurs and disconnect the microwire programming cable.

LMX2541SQ3320E Default Setup and Measured Performance



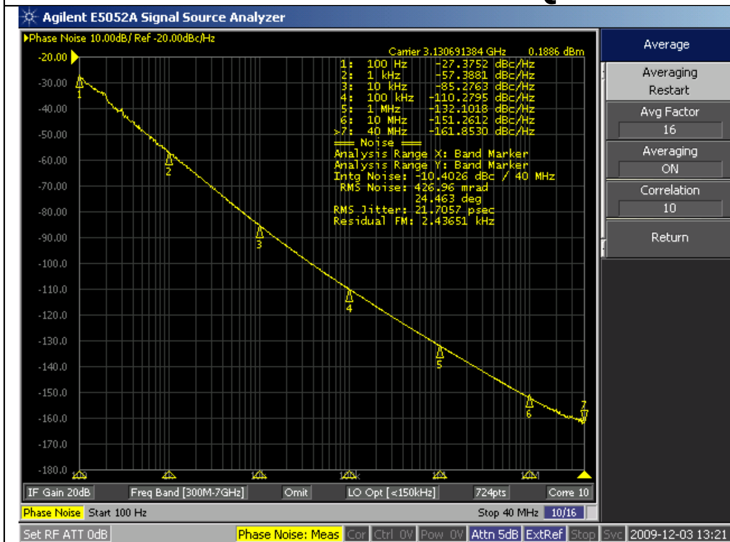


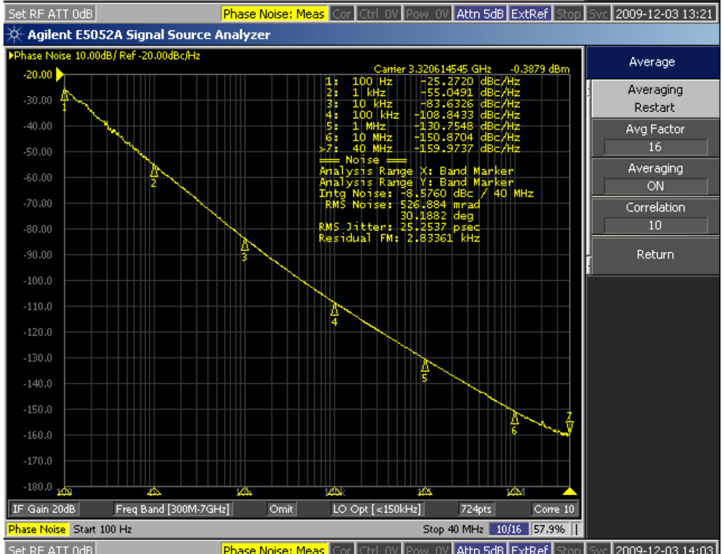
LMX2541S3320E Spurs for WORST CASE Channels (Fraction = 1/100)

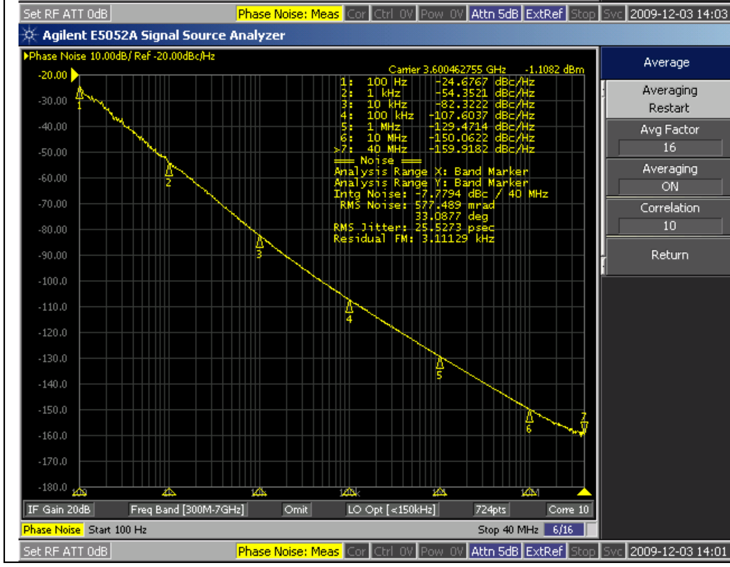


Note that the graphs have all been normalized the average carrier power.

LMX2541SQ3320E VCO Phase Noise



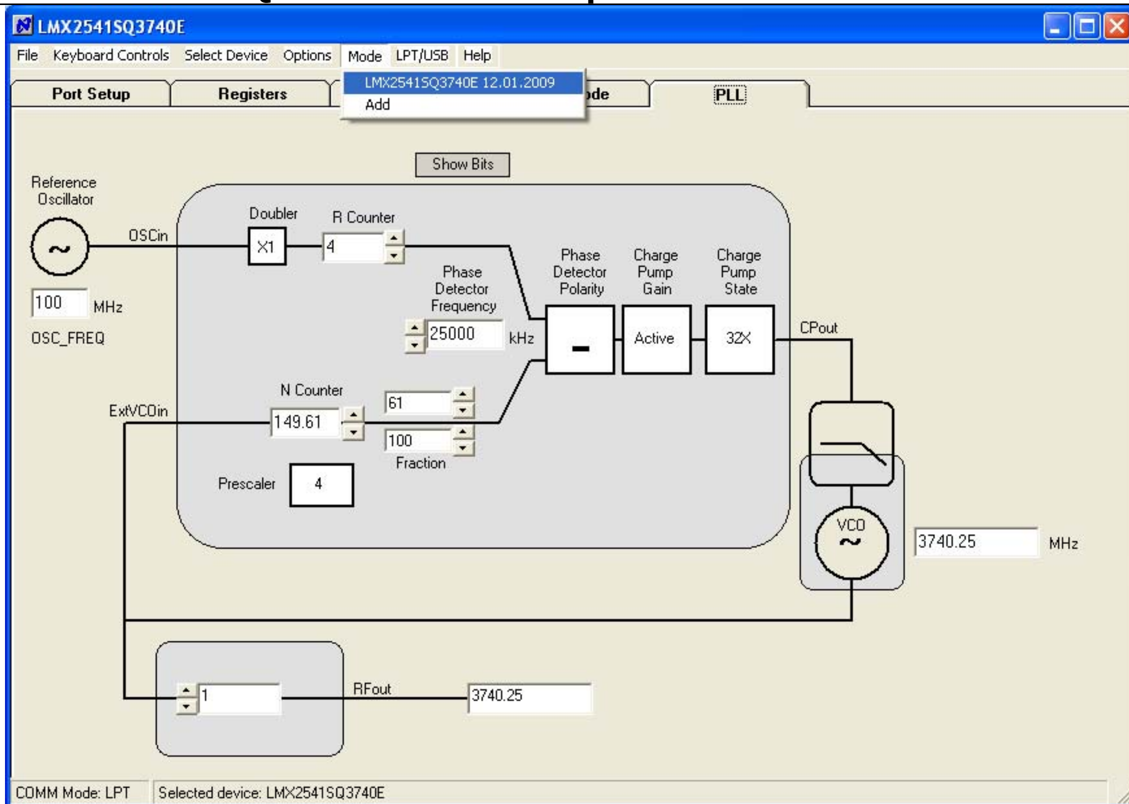


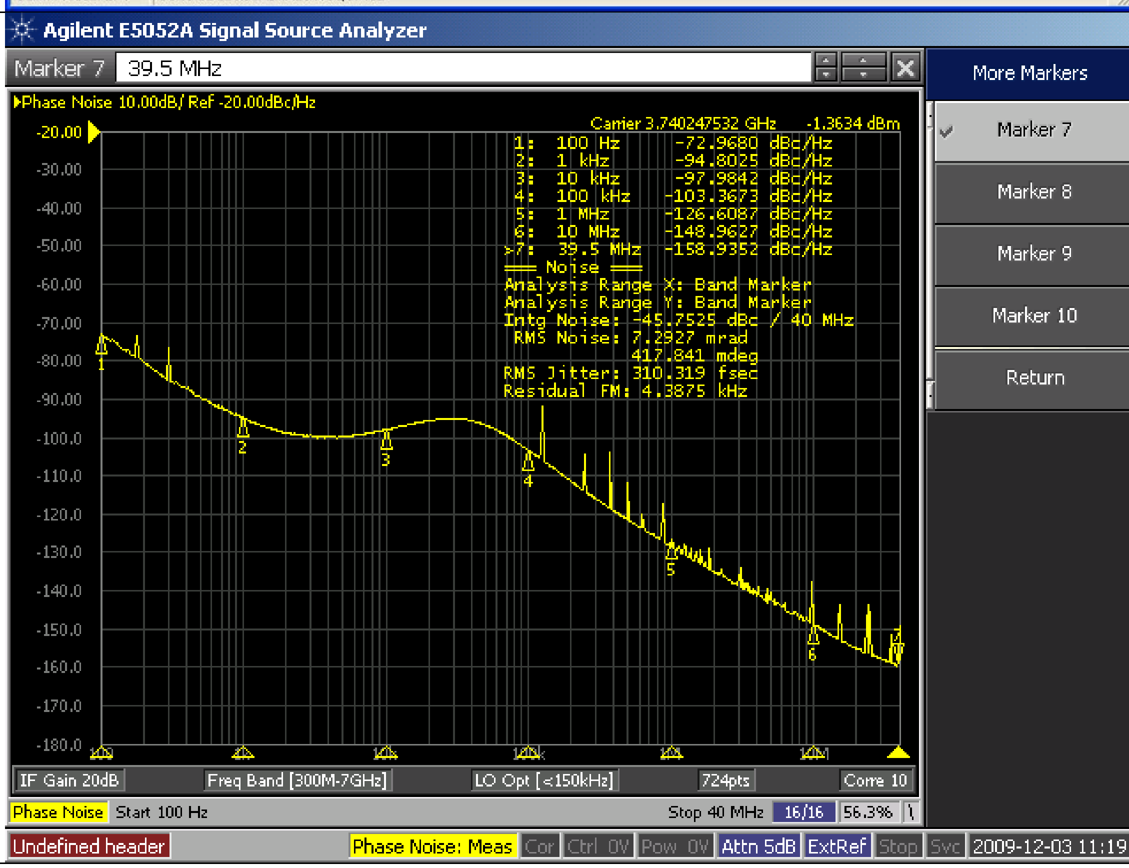


The plots show the VCO phase noise at low, middle, and high frequency.

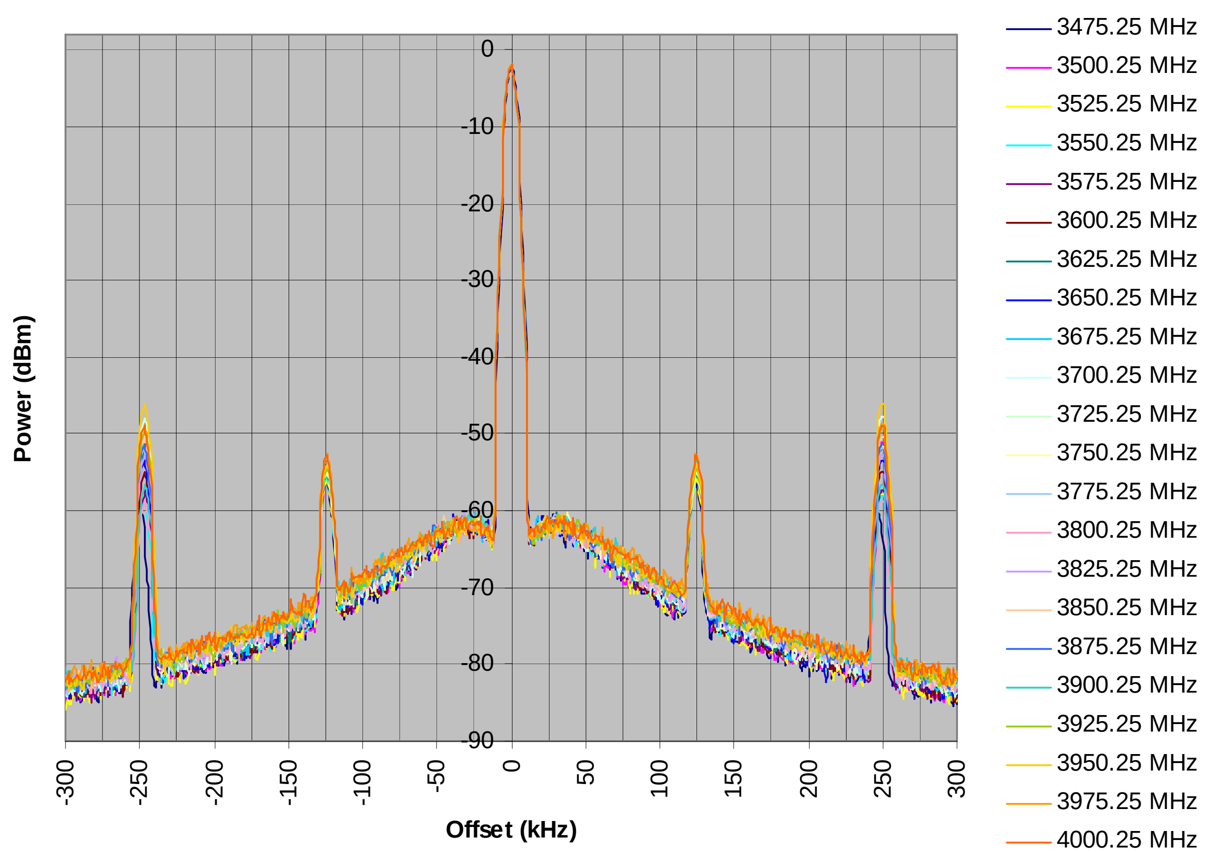
To measure the VCO phase noise, a simple technique is to lock the PLL to the desired frequency and set the charge pump state to "Tri-State", by clicking this on the PLL tab on Codeloader. If the phase noise analyzer can track the signal, a reasonable measurement can be made. To ensure that this measurement is of the VCO noise, omit the the spurs and disconnect the microwire programming cable.

LMX2541SQ3740E Default Setup and Measured Performance



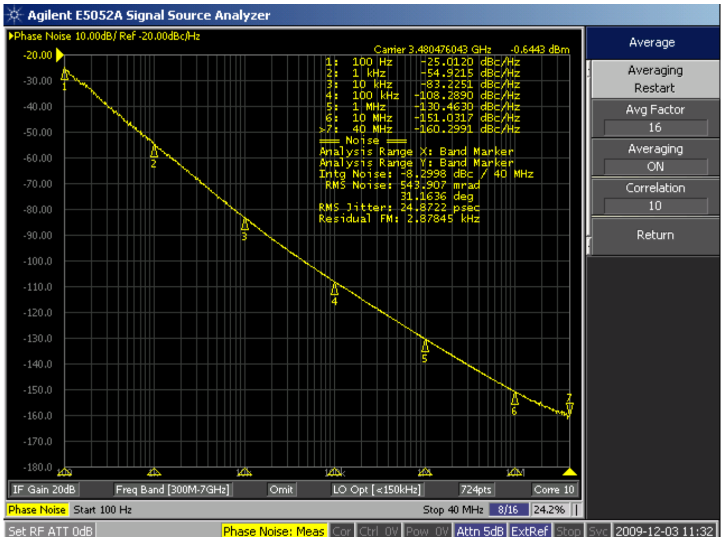


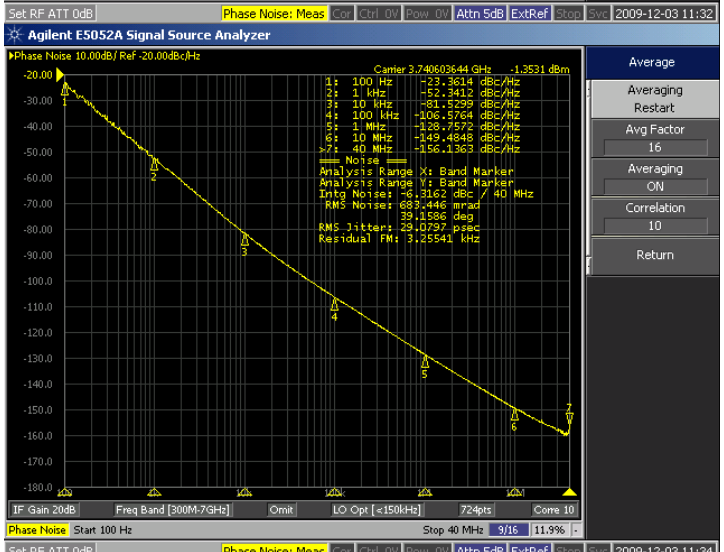
LMX2541S3740E Spurs for WORST CASE Channels (Fraction = 1/100)

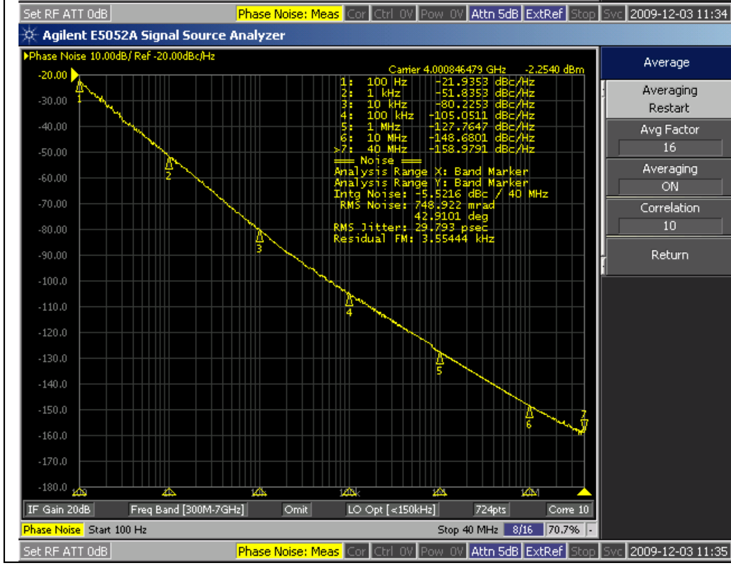


Note that the graphs have all been normalized the average carrier power.

LMX2541SQ3740E VCO Phase Noise







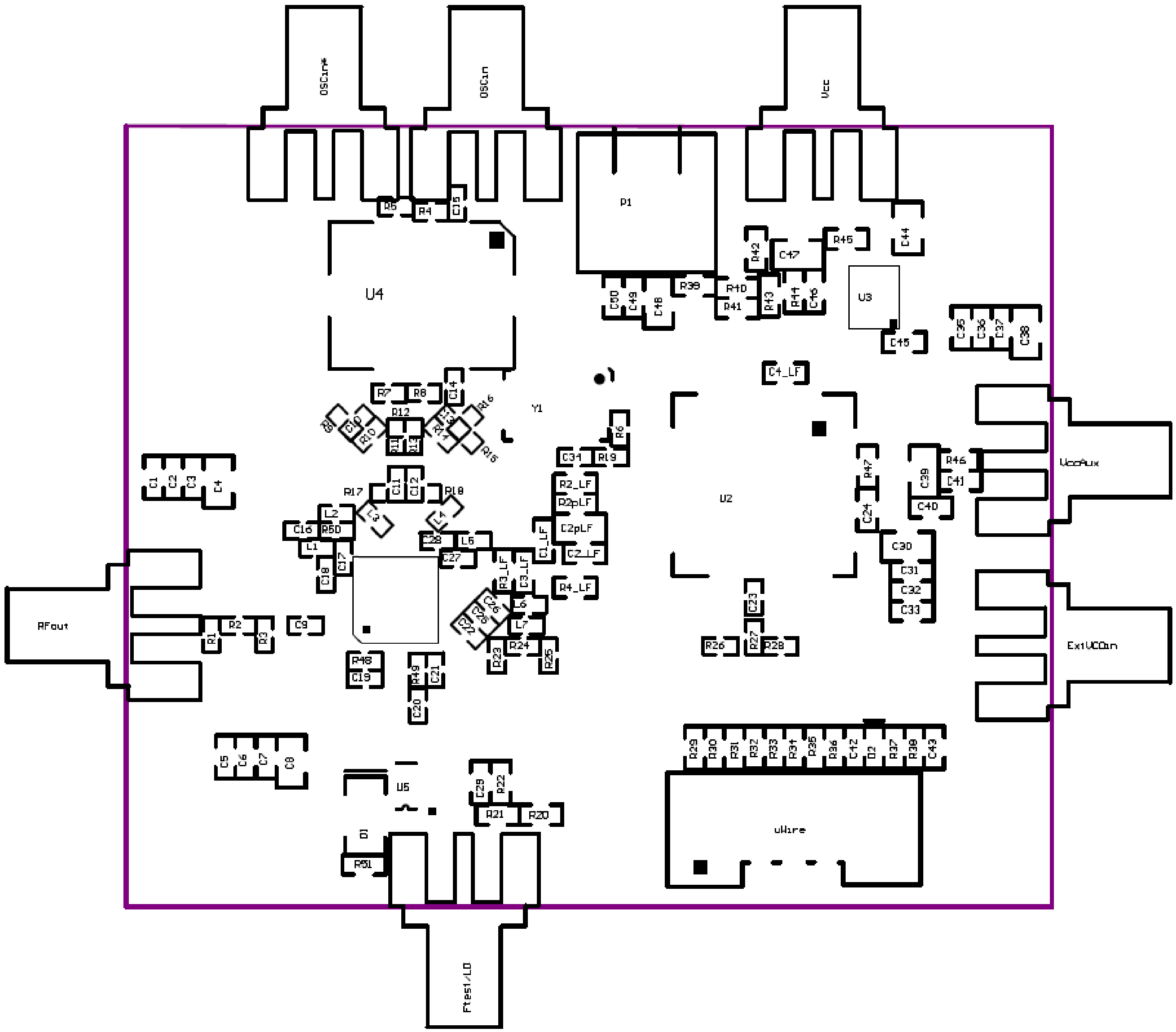
The plots show the VCO phase noise at low, middle, and high frequency.

To measure the VCO phase noise, a simple technique is to lock the PLL to the desired frequency and set the charge pump state to “Tri-State”, by clicking this on the PLL tab on Codeloader. If the phase noise analyzer can track the signal, a reasonable measurement can be made. To ensure that this measurement is of the VCO noise, omit the the spurs and disconnect the microwire programming cable.

Bill of Materials

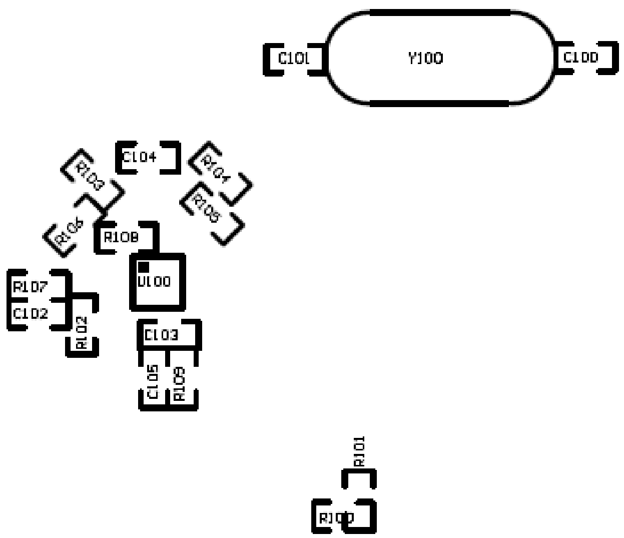
Revision	9/30/2009			
Part	**Manufacturer**	**Part Number**	**Qty**	**Identifier**
Capacitors				
100 pF	Kemet	C0603C101J5GAC	4	C1, C5, C33, C35
2.2 nF	Kemet	C0603C222J5GAC	1	C3_LF
22 nF	Kemet	C0603C223K5RAC	1	C2_LF
0.1 uF	Kemet	C0603C104K5RAC	19	C2, C6, C9, C10, C11, C12, C13, C17, C18, C21, C24, C25, C26, C27, C28, C32, C36, C40, C49
1 uF	Kemet	C0603C105K8VAC	10	C3, C7, C16, C19, C31, C37, C41, C42, C43, C50
4.7 uF	Kemet	C0603C475K9PAC	4	C14, C15, C20, C34
10 uF	Kemet	C0805C106K9PAC	6	C4, C8, C30, C38, C39, C48
Resistors				
0 ohm	Vishay/Dale	CRCW06030000Z0EA	7	R3_LF, R12, R21, R39, R41, R42, R46
4.7 ohm	Vishay/Dale	CRCW06034R7JNEA	2	R49, R50
10 ohm	Vishay/Dale	CRCW060310R0JNEA	3	R6, R47, R48
18 ohm	Vishay/Dale	CRCW060318R0JNEA	1	R2
51 ohm	Vishay/Dale	CRCW060351R0JNEA	2	R10, R14
120 ohm	Vishay/Dale	CRCW0603120RJNEA	3	R7, R8, R51
180 ohm	Vishay/Dale	CRCW0603180RJNEA	1	R36
330 ohm	Vishay/Dale	CRCW0603330RJNEA	2	R1, R3
470 ohm	Vishay/Dale	CRCW0603470RJNEA	1	R2_LF
2.2 k	Vishay/Dale	CRCW06032K20JNEA	1	R35
15 k	Vishay/Dale	CRCW060315K0JNEA	3	R30, R32, R34
27 k	Vishay/Dale	CRCW060327K0JNEA	5	R29, R31, R33, R37, R38
100 k	Vishay/Dale	CRCW0603100KJNEA	2	R4, R5
Other				
Ferrite	Digikey	490-1015-1-ND	7	L1, L2, L3, L4, L5, L6, L7
3.3 V zener	Comchip	CZRU52C3V3	1	D2
HEADER_2X5 (POLARIZED)	FCI Electronics	52601-S10-8	1	uWire
Green LED	Lumex	SML-LX2832GC-TR	1	D1
POWER_SMALL	Weidmuller	1594540000.0	1	P1
SMA	Johnson Components	142-0701-851	4	OSCin, OSCin*, RFout, Vcc
TCXO - 100 MHz	Connor-Winfield	CWX813 - 100 MHz	1	Y1
NFET	Fairchild	BSS138	1	U5
VCXO - 100 MHz	CRYSTEK	CVPD-920 – 100 MHz	1	U4
LMX2541	National Semiconductor	LMX2541SQxxxx	1	U1
Standoffs	SPC Technology	SPCS-6	4	Place in Holes at the corners of the board.
Open				
Open	-	Open Capacitor	14	C1_LF, C2pLF, C4_LF, C22, C23, C29, C44, C45, C46, C47
Open		Open Capacitor	6	C100, C101, C102, C103, C104, C105
Open	-	Open Resistor	22	R2pLF,R4_LF, R9, R11, R13, R15, R16, R17, R18, R19, R20, R22, R23, R24, R25, R26, R27, R28, R40, R43, R44, R45
Open	-	Open Resistor	9	R100, R101, R102, R103, R104, R105, R106, R107, R108, R109
Open	-	Open Crystal	1	Y100
Open	-	Open IC	3	U2, U3, U100
Open	-	Open SMA	3	ExtVCOin, Ftest/LD, VccAux

Top Assembly Diagram



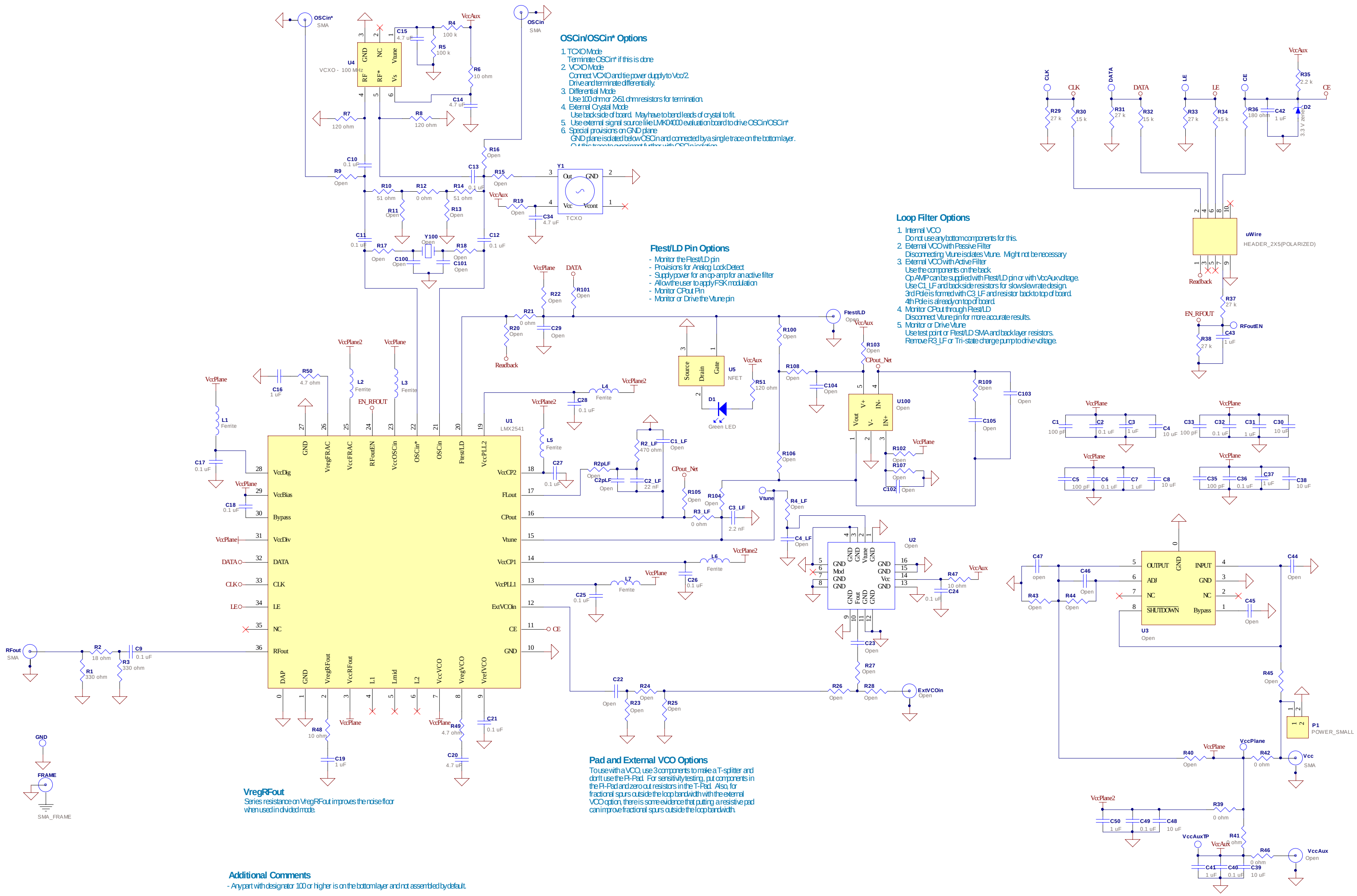
234

Bottom Assembly Diagram



No Components are assembled on the bottom layer in the default setup.

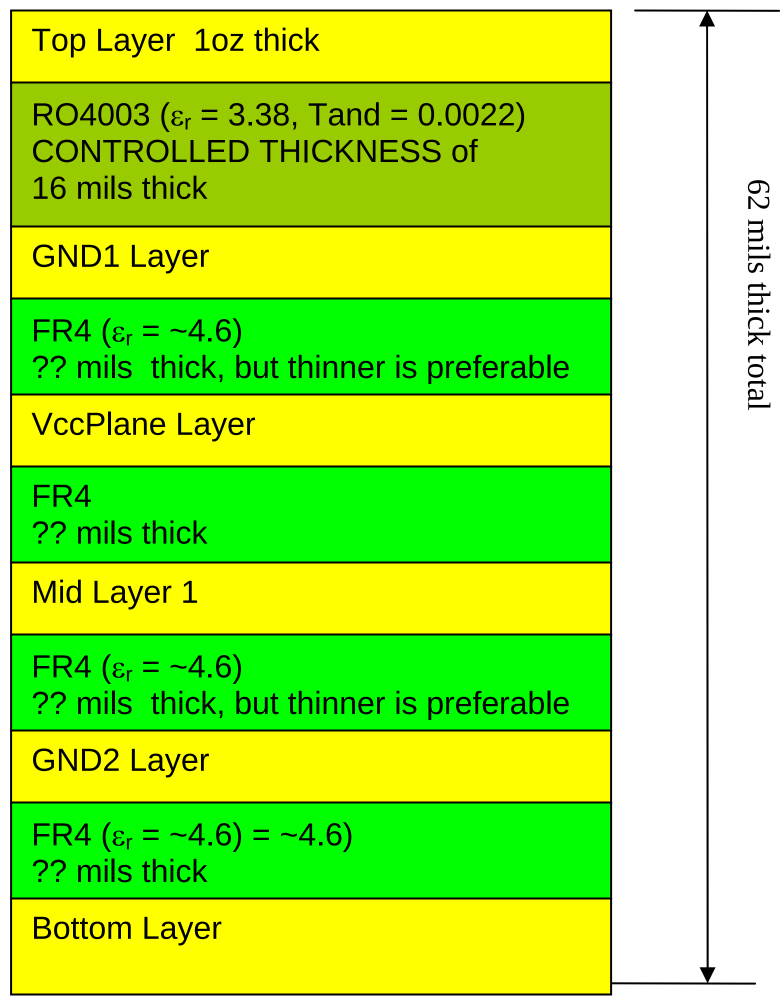
Schematic



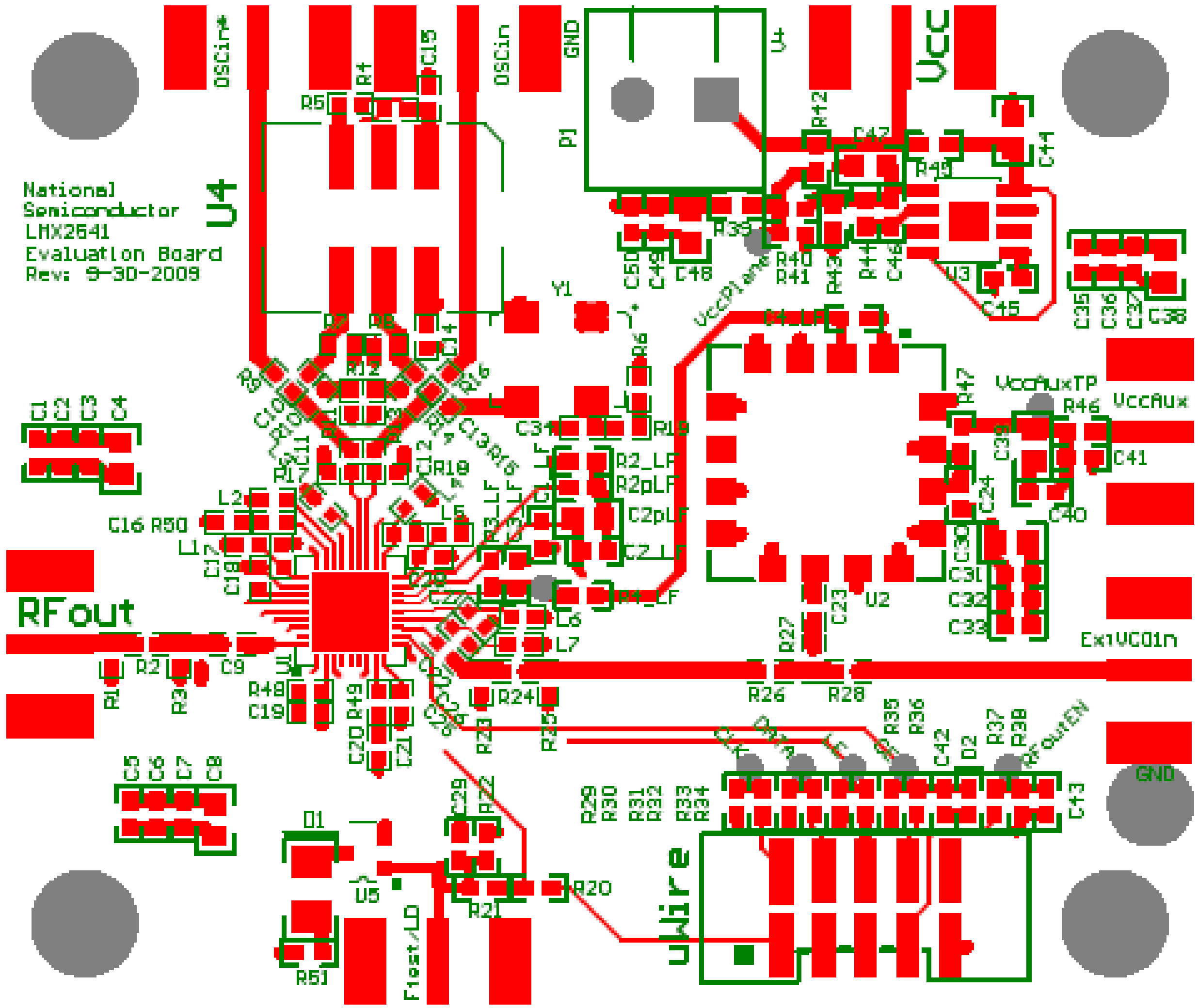
OSCin/OSCin* Options
1. TCXO Mode
Terminate OSCin* if this is done
2. VCXO Mode
Connect VCXO and tie power dupply to Vcc/2.
Drive and terminate differentially.
3. Differential Mode
Use 100 ohm or 2x51 ohm resistors for termination.
4. External Crystal Mode
Use back side of board. May have to bend leads of crystal to fit.
5. Use external signal source like LMK04000 evaluation board to drive OSCin/OSCin*
6. Special provisions on GND plane
GND plane isolated below OSCin and connected by a single trace on the bottom layer.
Ftest/LD Pin Options
- Monitor the Ftest/LD pin
- Provisions for Analog Lock Detect
- Supply power for an op-amp for an active filter
- Allow the user to apply FSK modulation
- Monitor CPout Pin
- Monitor or Drive the Vtune pin
Loop Filter Options
1. Internal VCO
Do not use any bottom components for this.
2. External VCO with Passive Filter
Disconnecting Vtune isolates Vtune. Might not be necessary
3. External VCO with Active Filter
Use the components on the back.
Op AMP can be supplied with Ftest/LD pin or with VccAux voltage.
Use C1_LF and back side resistors for slow slew rate design.
3rd Pole is formed with C3_LF and resistor back to top of board.
4th Pole is already on top of board.
4. Monitor CPout through Ftest/LD
Disconnect Vtune pin for more accurate results.
5. Monitor or Drive Vtune
Use test point or Ftest/LD SMA and back layer resistors.
Remove R3_LF or Tri-state charge pump to drive voltage.
VregRFout
Series resistance on VregRFout improves the noise floor when used in divided mode.
Pad and External VCO Options
To use with a VCO, use 3 components to make a T-splitter and don't use the Pi-Pad. For sensitivity testing, put components in the Pi-Pad and zero out resistors in the T-Pad. Also, for fractional spurs outside the loop bandwidth with the external VCO option, there is some evidence that putting a resistive pad can improve fractional spurs outside the loop bandwidth.
Additional Comments
- Any part with designator 100 or higher is on the bottom layer and not assembled by default.

Board Layer Stackup

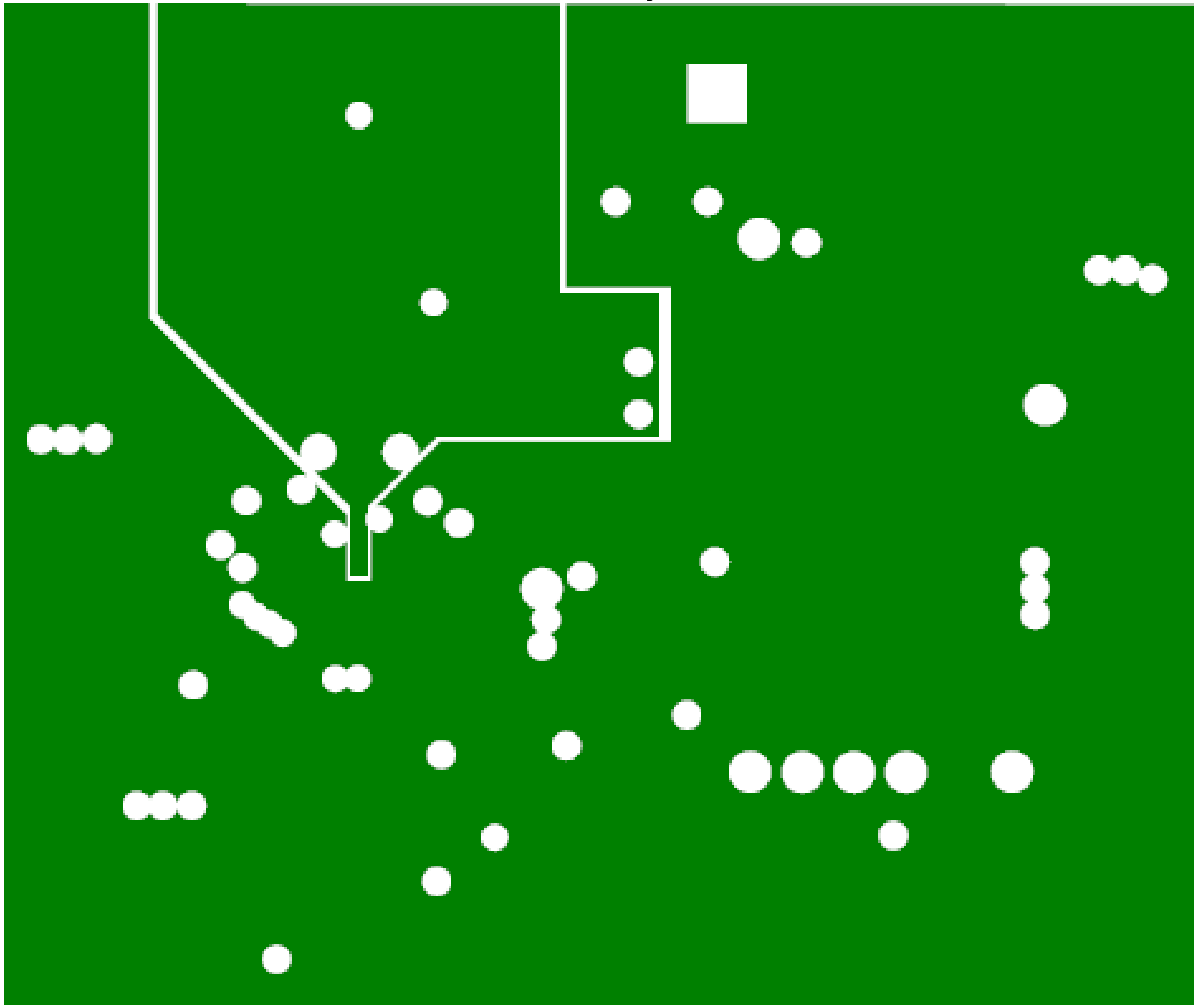
Board Material	Rogers RO4003
Number of Layers	6
Board Thickness	0.062”
Copper Weight	1 oz Finished
Finish	Immersion Gold
Solder Mask Color	Green/Gloss
Testing	100% Electrical Testing



Top Layer and Silkscreen

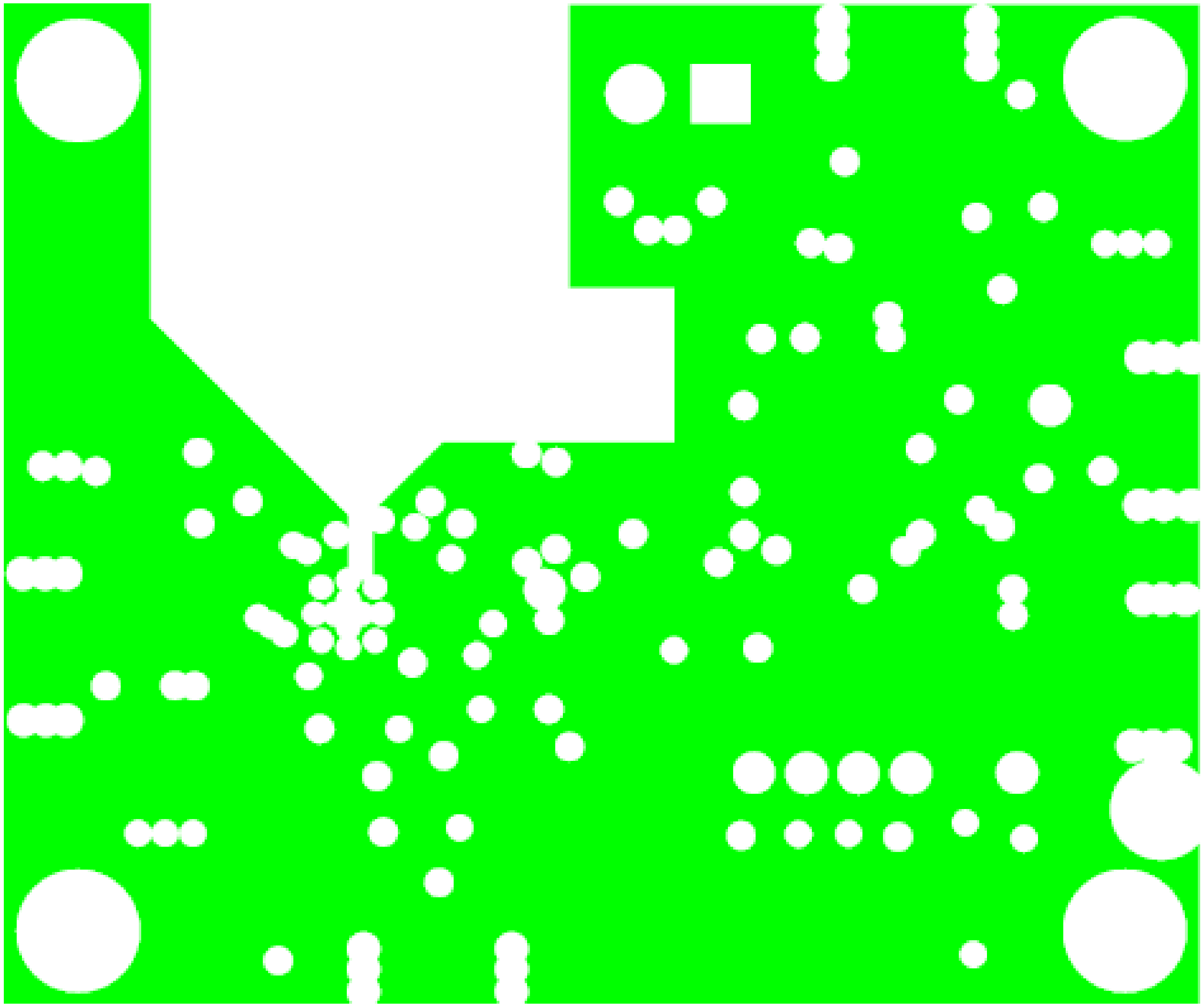


GND1 Layer



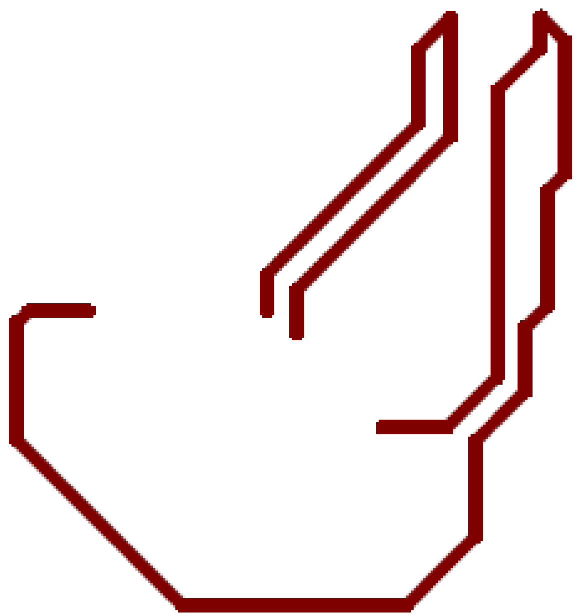
Beneath the TCXO, the ground plane is separated. It is believed that this may improve spurs, especially at offset frequencies equal to the TCXO frequency. These planes are connected on the bottom layer by a small trace.

VccPlane Layer



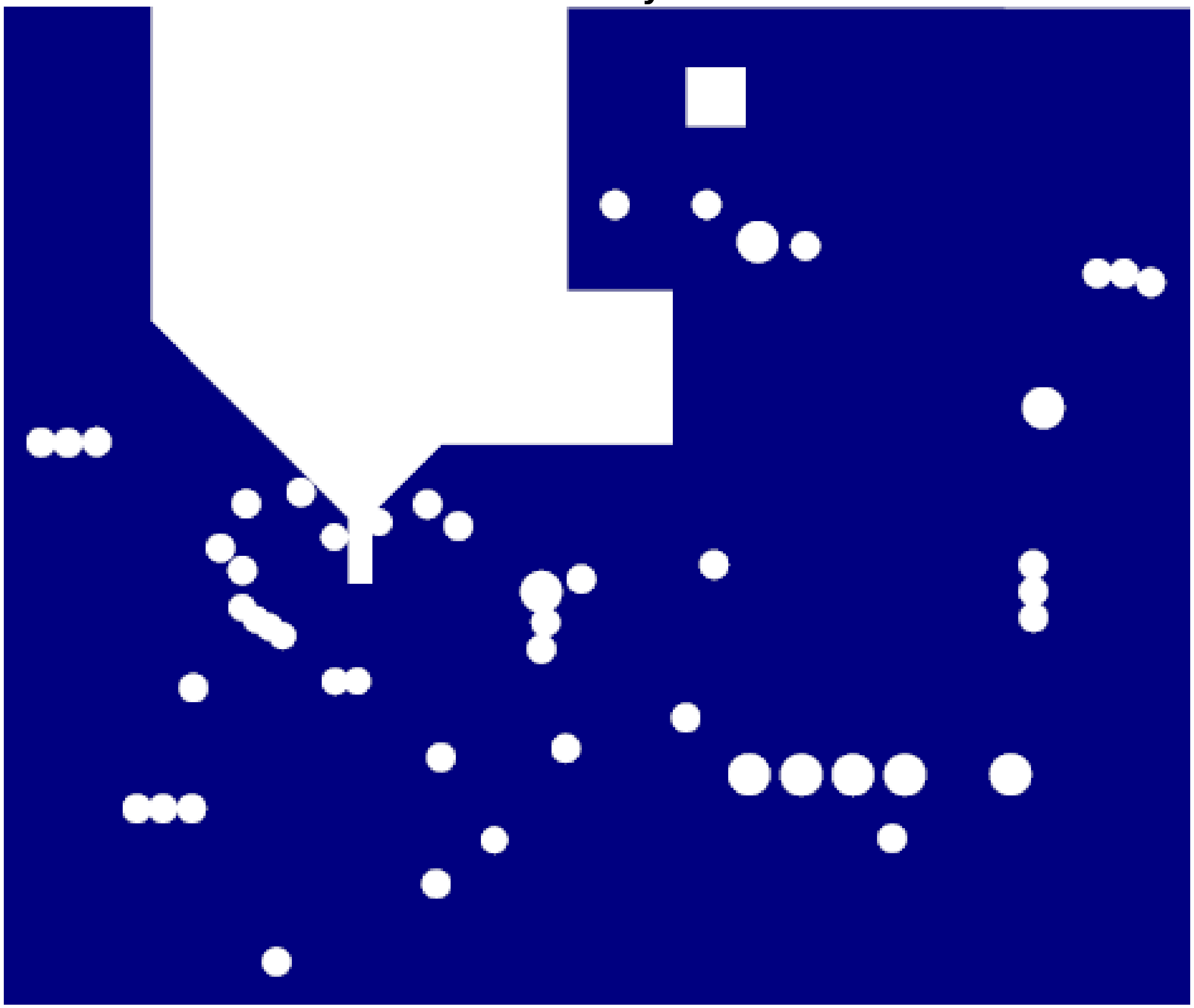
Beneath the TCXO, the power plane is removed to minimize the chance of any noise getting onto this plane.

MidLayer 1



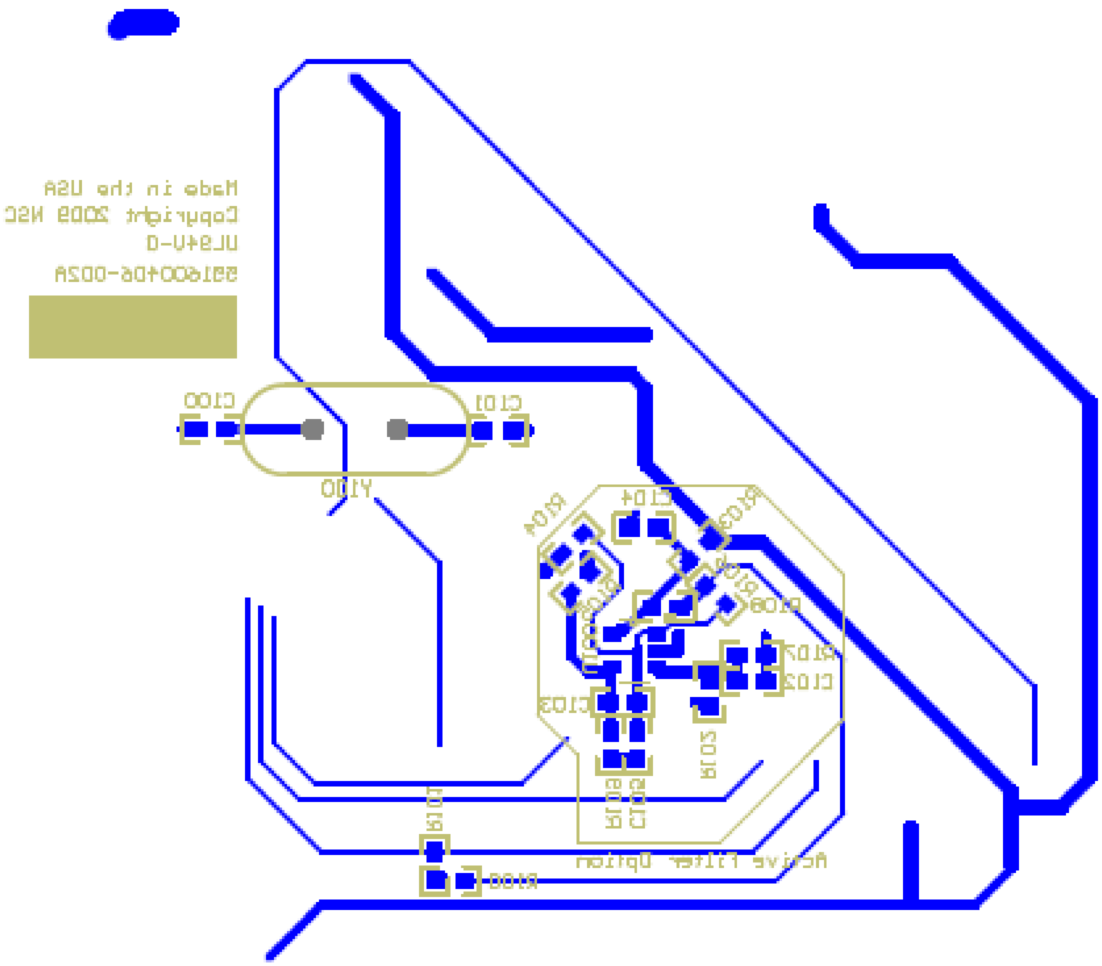
Certain pins like VccFRAC and the TCXO supply pins could potentially be sources of noise. These traces were put on this separate layer to try to isolate them more from the

GND2 Layer



Beneath the TCXO, the ground plane is separated. It is believed that this may improve spurs, especially at offset frequencies equal to the TCXO frequency. These planes are connected on the bottom layer by a small trace.

Bottom Layer and Silkscreen



This layer has the small trace that connects the grounded pieces in the GND1 layer. It has options for an active filter and crystal as well.