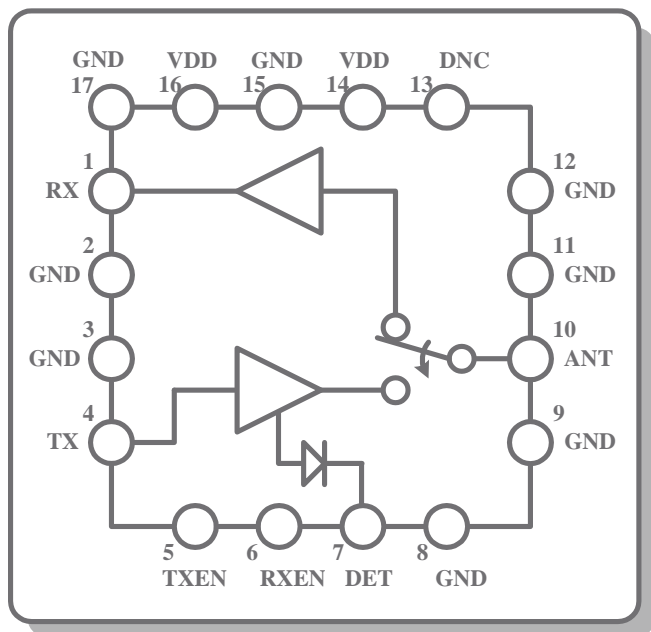


CMOS 2.4GHZ TRANSMIT/RECEIVE WLAN RFIC



Description

The RFX2402E is a fully integrated, single-chip, single-die RFIC (RF Front-end Integrated Circuit) which incorporates all the RF functionality needed for today's wireless communications.

The RFX2402E architecture integrates the PA, LNA, Transmit and Receive switching circuitry, the associated matching network, and a harmonic filter all in a CMOS single-chip device.

This RFIC is designed for use in 802.11b/g/n/ac applications operating at 2.4GHz. Combining superior performance, high sensitivity and efficiency, low noise, small form factor, and low cost, the RFX2402E is the ideal solution for single antenna applications, and the ideal building block for MIMO applications.

The RFX2402E has simple and low-voltage CMOS control logic, and requires minimal external components for system implementation. The PA power detector circuit is also integrated.

Applications

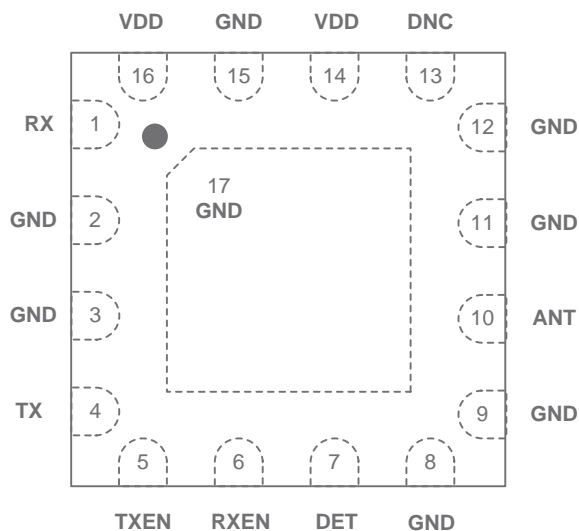
- ▶ 802.11b/g/n/ac Multimedia Applications
- ▶ 802.11b/g/n/ac Embedded Applications
- ▶ 802.11b/g/n/ac Mobile Platforms
- ▶ 802.11b/g/n/ac NIC PC Card
- ▶ Other 2.4GHz ISM Radios
- ▶ 802.11b/g/n/ac Access Point

FEATURES

- ▶ 2.4GHz ISM, Single Chip, Single-Die RF Front-End IC
- ▶ Separate TX and RX Transceiver Port and Single Antenna Port
- ▶ 2.4GHz Power Amplifier with Low-Pass Harmonic Filter
- ▶ Low Noise Amplifier
- ▶ Transmit/Receive Switch Circuitry
- ▶ High Transmit Signal Linearity Meeting Standards for OFDM and CCK modulation
- ▶ Integrated Power Detector for Transmit Power Monitor and Control
- ▶ Compatible with Low Voltage (1.2V) CMOS Control Logic or levels up to VDD
- ▶ ESD Protection Circuitry on All Ports
- ▶ DC Decoupled RF Ports
- ▶ Internal RF Decoupling on All VDD Bias Pins
- ▶ Low Noise Figure for Receive Channels
- ▶ High Power Capability for Received Signals
- ▶ Very Low DC Power Consumption
- ▶ Full On-chip Matching and Decoupling Circuitry
- ▶ Minimal External Components Required
- ▶ 50-Ohm Input / Output Matching
- ▶ Market Proven CMOS Technology
- ▶ 3mm x 3mm x 0.55mm Small Outline 16L-QFN Package with Exposed Ground Pad

PIN ASSIGNMENTS:

| Pin Number | Pin Name | Description |
|------------------------------|----------|---|
| 1 | RX | Received RF Signal from the LNA to the Transceiver; DC Shorted to GND |
| 2, 3, 8, 9, 11,12, 15, 17 | GND | Ground – Must be connected to Ground in the Application Circuit |
| 4 | TX | Transmitted RF signal from the Transceiver to the PA; DC Shorted to GND |
| 5 | TXEN | CMOS Input to Enable the PA |
| 6 | RXEN | CMOS Input to Enable the LNA |
| 7 | DET | Analog Voltage Proportional to the PA Power Output |
| 10 | ANT | Antenna port RF Signal from the PA or RF Signal Applied to the LNA; DC Shorted to GND |
| 13 | DNC | Reserved pin, Do not connect in the Application Circuit |
| 14, 16 | VDD | Voltage Supply Connection |

PINOUT DIAGRAM:


(Top "See-Through" View)

ABSOLUTE MAXIMUM RATINGS:

| Parameters | Units | Min | Max | Conditions |
|------------------------------------|-------|-----|------|---|
| DC VDD Voltage Supply | V | 0 | 4.5 | All VDD Pins |
| DC Control Pin Voltage | V | 0 | 3.6 | Through 1Kohm resistor |
| DC VDD Current Consumption | mA | | 350 | Through VDD Pins when TX is "ON" |
| DC Control Pin Current Consumption | μA | | 1 | |
| TX RF Input Power | dBm | | +10 | All Operating Modes |
| ANT RF Input Power | dBm | | +5 | When RX is "ON" |
| Junction Temperature | °C | | +150 | |
| Storage Ambient Temperature | °C | -50 | +150 | No RF and DC Voltages Applied Appropriate care required according to JEDEC Standards |

Note: Sustained operation at or above the Absolute Maximum Ratings for any one or combinations of the above parameters may result in permanent damage to the device and is not recommended. All Maximum RF Input Power Ratings assume 50-Ohm terminal impedance.

NOMINAL OPERATING CONDITIONS:

| Parameters | Units | Min | Typ | Max | Conditions |
|---|-------|-----|-----|------|-------------------------|
| DC VDD Voltage Supply | V | 2.7 | 3.3 | 3.6 | All VDD Pins |
| Control Voltage "High" (Note 1) | V | 1.2 | | | Through Series Resistor |
| Control Voltage "Low" | V | | | 0.3 | |
| DC Control Pin Current Consumption | uA | | 1 | | |
| DC Shutdown Current | uA | | 2 | | All Control Lines "Low" |
| PA Turn On/Off Time | usec | | 0.5 | | |
| LNA Turn On/Off Time | usec | | 0.8 | | |
| Shut-Down and "ON" State Switching Time | usec | | 0.5 | | |
| Operating Ambient Temperature | °C | -40 | | +125 | See note 2 |
| θja | °C/W | | 35 | | |

Note 1: If control voltage can exceed 1.8V, a 1KΩ – 10KΩ series resistor is recommended for the application circuit on each control line.

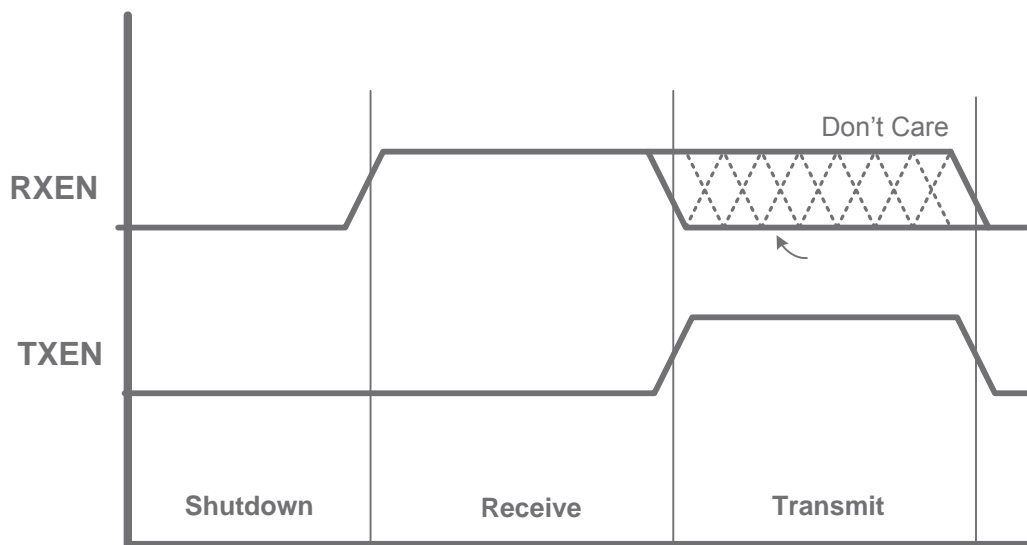
Note2: For operation above +85 °C, use the θja as guidance for system design to assure the junction temperature will not exceed the maximum of +150 °C.

TRANSMIT TECHNICAL PARAMETERS (VDD=3.3V, T=+25 °C)

| Parameters | Units | Min | Typ | Max | Conditions |
|--------------------------------------|---------|-----|----------|-----|--|
| Operating Frequency Band | GHz | 2.4 | | 2.5 | All RF Pins Terminated by 50 Ohms |
| Output P1dB | dBm | | +24 | | CW |
| Linear Output Power 802.11b | dBm | | +21 | | 1Mbps CCK, Mask Compliance |
| Linear Output Power 802.11n | dBm | | +17 | | 54Mbps OFDM, EVM< -33dB at ANT |
| Linear Output Power 802.11g | dBm | | +18 | | 54Mbps OFDM, EVM<-30 dB at ANT |
| Large-Signal Power Gain in All Modes | dB | | 28 | | P _{OUT} = +18dBm |
| Small-Signal Power Gain in All Modes | dB | | 28.5 | | P _{OUT} = 0dBm |
| TX Quiescent Current | mA | | 80 | | No RF Applied |
| TX Linear Current | mA | | 140 | | P _{OUT} = +18dBm |
| Power Detector Voltage Output | V | | 0.25-1.6 | | P _{OUT} = +5 to +20dBm |
| Second Harmonic (CW) | dBc | | -30 | | P _{OUT} = +20dBm, CW at ANT Pin |
| Third Harmonic (CW) | dBc | | -35 | | P _{OUT} = +20dBm, CW at ANT Pin |
| Modulated Second Harmonic | dBm/MHz | | -26 | | P _{OUT} = +20dBm, 802.11n HT40 |
| Modulated Third Harmonic | dBm/MHz | | -30 | | P _{OUT} = +20dBm, 802.11n HT40 |
| Input Return Loss | dB | | -10 | | |
| Output Return Loss | dB | | -12 | | |
| Input Output Impedance Single-Ended | Ohm | | 50 | | |
| TX Leakage to RX Port | dBm | | -7 | | P _{OUT} = +20dBm at ANT |

RECEIVE TECHNICAL PARAMETERS (VDD=3.3V, T=+25 °C)

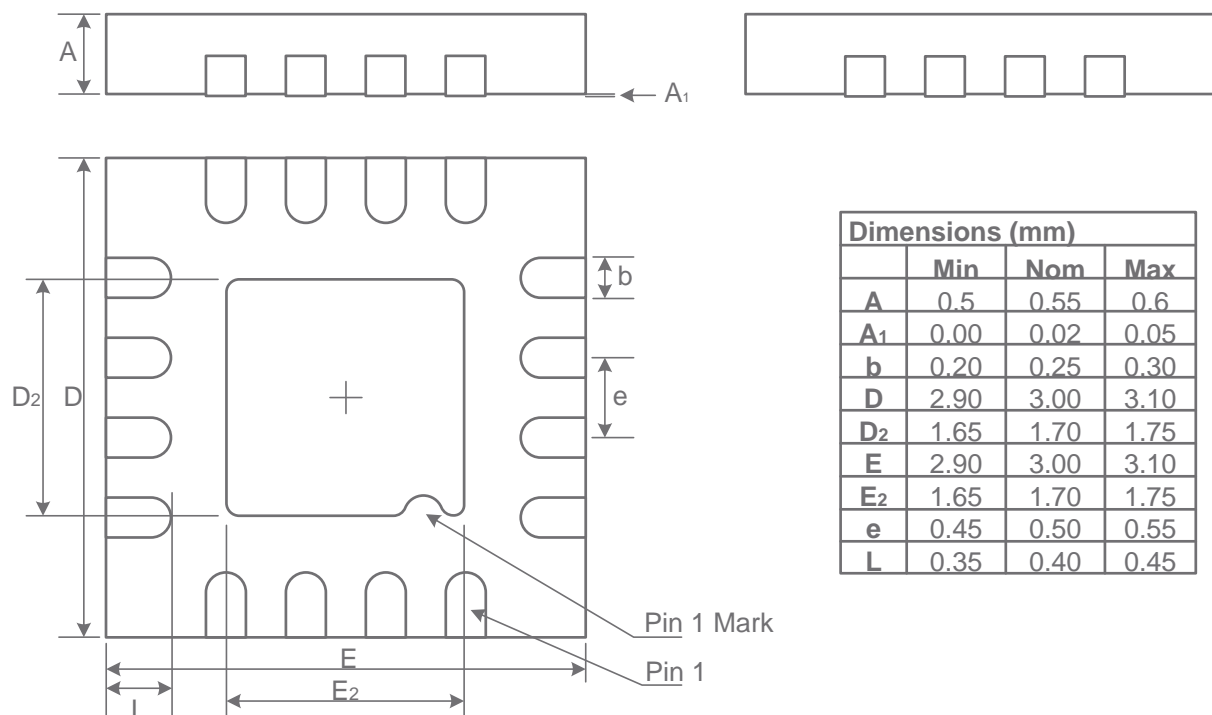
| Parameters | Units | Min | Typ | Max | Conditions |
|--------------------------|-------|-----|-----|-----|--------------------------------------|
| Operating Frequency Band | GHz | 2.4 | | 2.5 | All RF Pins are Terminated by 50 Ohm |
| Gain | dB | | 11 | | |
| Noise Figure | dB | | 3 | | |
| Input Return Loss | dB | | -12 | | |
| Output Return Loss | dB | | -10 | | |
| RF Port Impedance | Ohm | | 50 | | |
| RX Quiescent Current | mA | | 9 | | No RF Applied |
| Input P _{1dB} | dBm | | -5 | | |

CONTROL SIGNAL DIAGRAM:

CONTROL LOGIC TRUTH TABLE:

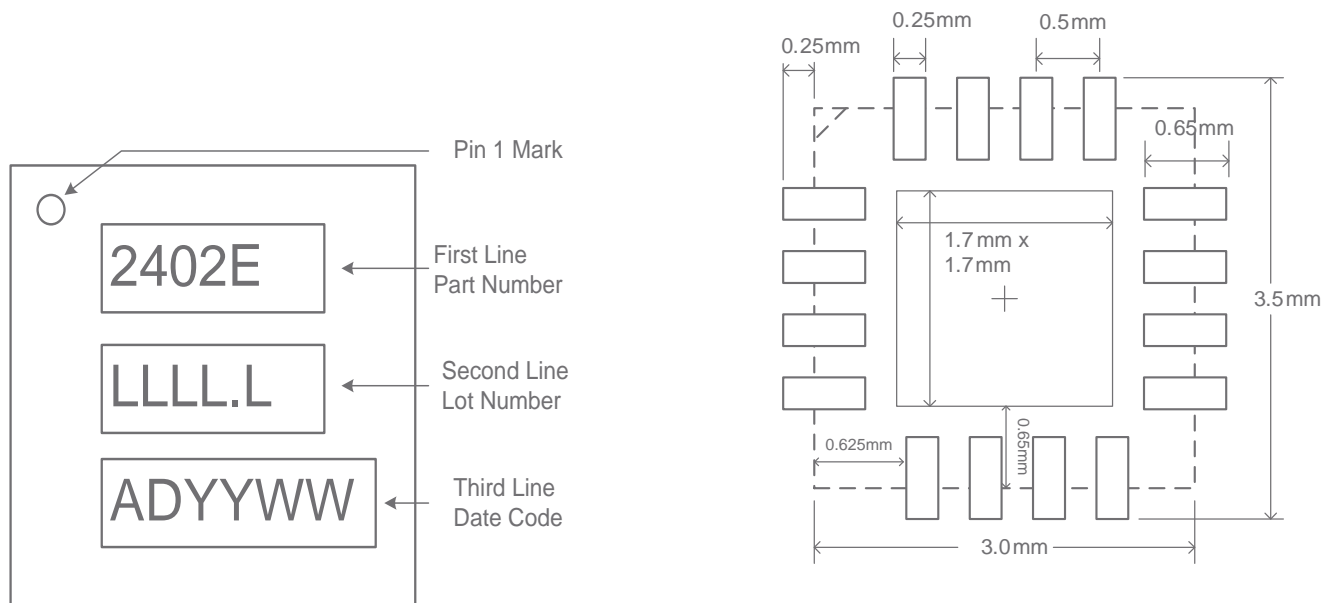
| TXEN | RXEN | Operating Conditions |
|------|------|----------------------|
| 0 | 0 | Shut-down |
| 0 | 1 | RX Active |
| 1 | X | TX Active |

Note: "1" denotes high voltage state ($> 1.2V$)
 "0" denotes low voltage stage ($< 0.3V$) at Control Pins
 "X" denotes the don't care state

PACKAGE DIMENSIONS:



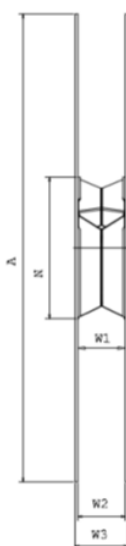
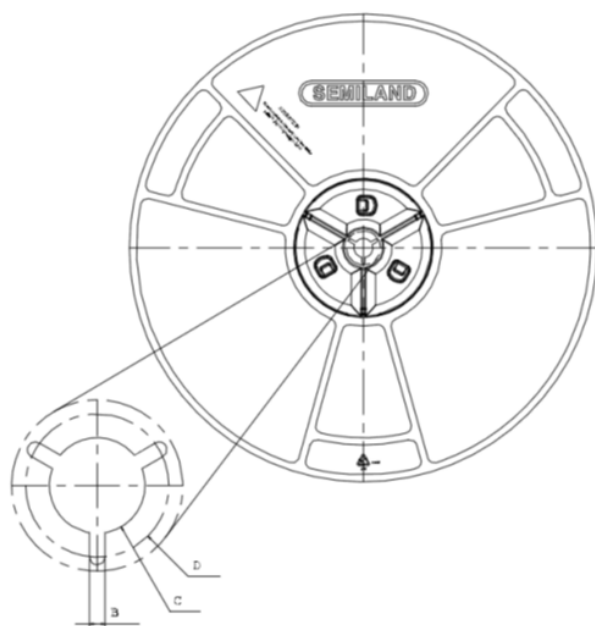
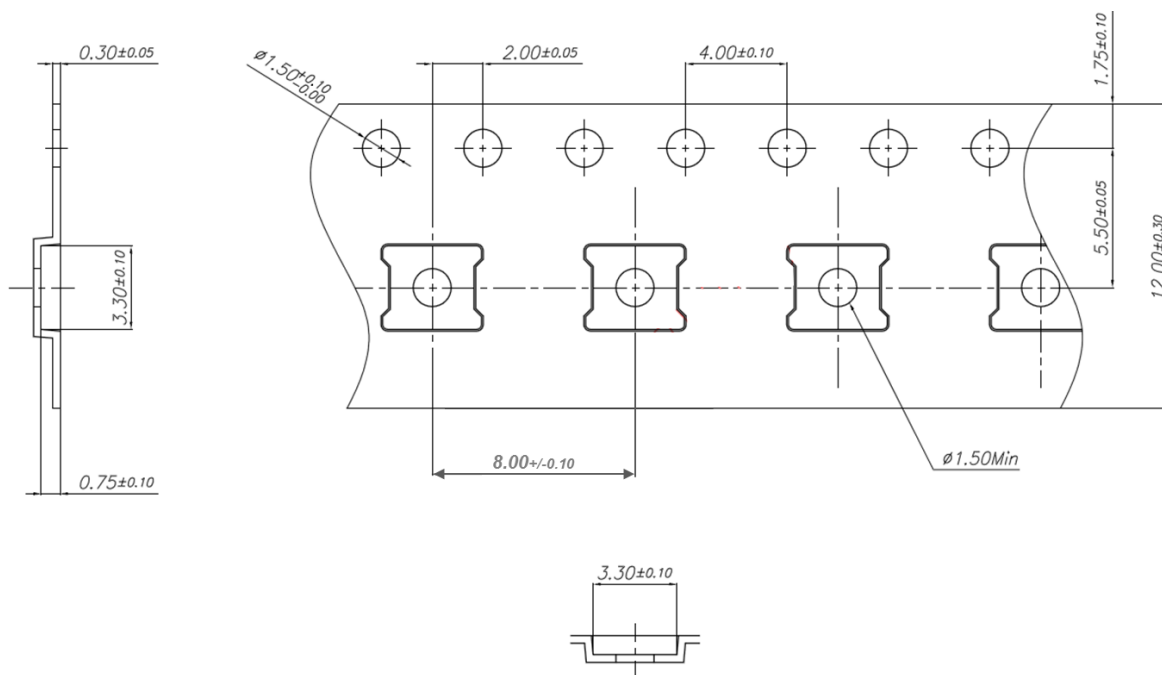
PACKAGE MARKING



PCB LAND PATTERN

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TAPE AND REEL INFORMATION:



| | |
|-------|--------------------------------------|
| Size | 12mm |
| A | 330 ^{+0.2} _{-2.0} |
| B | 1.5min |
| C | 13.0 ^{+0.5} _{-0.2} |
| D | 20.2min |
| N | 100 ^{+2.0} _{-0.0} |
| W1 | 12.4 ^{+3.0} _{-0.0} |
| W2 | 12.4 ^{+3.0} _{-0.0} |
| W3 | 16.4 ^{+2.0} _{-2.0} |
| PART# | SRL-12134H |