

TLP705A

1. Applications

- Transistor Inverters
- Air Conditioner Inverters
- MOSFET Gate Drivers
- IGBT Gate Drivers

2. General

The TLP705A is a photocoupler in a SDIP6 package that consists of a GaAlAs infrared light-emitting diode (LED) optically coupled to an integrated high-gain, high-speed photodetector IC chip. The TLP705A is physically smaller than the one in an 8-pin DIP package and compliant with international safety standards for reinforced insulation. It thus provides a smaller footprint solution for applications that require safety standard certification. The TLP705A has an internal Faraday shield that provides a guaranteed Common-mode transient immunity of 20 kV/ μ s. It has a totem-pole output that can both sink and source current. It is ideal for IGBT and power MOSFET gate drive.

3. Features

- (1) Output peak current: ± 0.6 A (max)
- (2) Operating temperature: -40 to 100°C
- (3) Supply current: 3 mA (max)
- (4) Supply voltage: 10 to 30 V
- (5) Threshold input current: 7.5 mA (max)
- (6) Propagation delay time: $t_{pHL}/t_{pLH} = 200$ ns (max)
- (7) Common-mode transient immunity: ± 20 kV/ μ s (min)
- (8) Isolation voltage: 5000 Vrms (min)
- (9) Safety standards

UL-approved: UL1577 File No.E67349

cUL-approved: CSA Component Acceptance Service No.5A, File No.E67349

VDE-approved: Option (D4) EN60747-5-2 (Note)

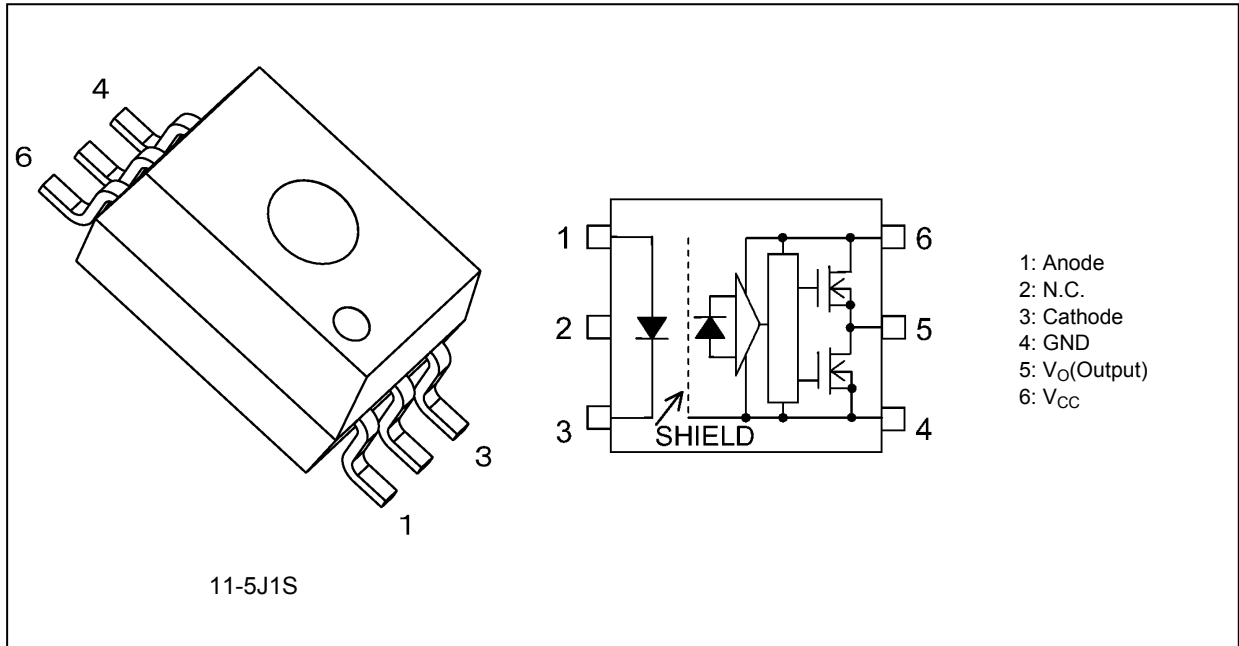
Certificate no. 40009302

Maximum operating insulation voltage: 890 Vpk

Highest permissible over voltage: 8000 Vpk

Note: When an EN60747-5-2 approved type is needed, please designate the Option (D4).

4. Packaging and Pin Configuration



5. Internal Circuit (Note)

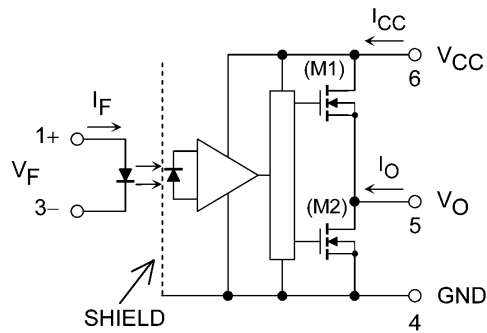


Fig. 5.1 Internal Circuit

Note: A 0.1- μ F bypass capacitor must be connected between pin 6 and pin 4.

6. Principle of Operation

6.1. Truth Table

Input	LED	M1	M2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

6.2. Mechanical Parameters

Characteristics	7.62-mm Pitch TLP705A	10.16-mm Pitch TLP705AF	Unit
Creepage distances	7.0 (min)	8.0 (min)	mm
Clearance distances	7.0 (min)	8.0 (min)	
Internal isolation thickness	0.4 (min)	0.4 (min)	

7. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25°C)

	Characteristics	Symbol	Note	Rating	Unit
LED	Input forward current	I _F		25	mA
	Input forward current derating (T _a ≥ 85°C)	ΔI _F /ΔT _a		-0.67	mA/°C
	Peak transient input forward current	I _{FPT}	(Note 1)	1	A
	Peak transient input forward current derating (T _a ≥ 85°C)	ΔI _{FPT} /ΔT _a		-25	mA/°C
	Input reverse voltage	V _R		5	V
	Input power dissipation	P _D		40	mW
	Input power dissipation derating (T _a ≥ 85°C)	ΔP _D /ΔT _a		-1.0	mW/°C
Detector	Peak high-level output current (T _a = -40 to 100°C)	I _{OPH}	(Note 2)	-0.6	A
	Peak low-level output current (T _a = -40 to 100°C)	I _{OPL}	(Note 2)	+0.6	
	Output voltage	V _O		35	V
	Supply voltage	V _{CC}		35	
Common	Operating temperature	T _{opr}		-40 to 100	°C
	Storage temperature	T _{stg}		-55 to 125	
	Lead soldering temperature (10 s)	T _{sol}	(Note 3)	260	
	Isolation voltage AC, 1 min, R.H. ≤ 60%, T _a = 25°C	BV _S	(Note 4)	5000	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width (PW) ≤ 1 μs, 300 pps

Note 2: Exponential waveform. Pulse width ≤ 2 μs, f ≤ 15 kHz

Note 3: ≥ 2 mm below seating plane.

Note 4: This device is considered as a two-terminal device: Pins 1, 2 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

8. Recommended Operating Conditions (Note)

Characteristics	Symbol	Note	Min	Typ.	Max	Unit
Input on-state current	I _{F(ON)}	(Note 1)	10	—	15	mA
Input off-state voltage	V _{F(OFF)}		0	—	0.8	V
Supply voltage	V _{CC}	(Note 2)	10	—	30	
Peak high-level output current	I _{OPH}		—	—	-0.2	A
Peak low-level output current	I _{OPL}		—	—	+0.2	
Operating frequency	f	(Note 3)	—	—	250	kHz

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this datasheet should also be considered.

Note: A ceramic capacitor (0.1 μF) should be connected between pin 6 and pin 4 to stabilize the operation of a high-gain linear amplifier. Otherwise, this photocoupler may not switch properly. The bypass capacitor should be placed within 1 cm of each pin.

Note 1: The rise and fall times of the input on-current should be less than 0.5 μs.

Note 2: Denotes the operating range, not the recommended operating condition.

Note 3: Exponential waveform. I_{OPH} ≥ -0.25 A (≤ 90 ns), I_{OPL} ≤ 0.25 A (≤ 90 ns), T_a = 100°C

9. Electrical Characteristics (Note)
(Unless otherwise specified, $T_a = -40$ to 100°C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	V_F		—	$I_F = 10 \text{ mA}$, $T_a = 25^\circ\text{C}$	1.40	1.57	1.80	V
Input forward voltage temperature coefficient	$\Delta V_F / \Delta T_a$		—	$I_F = 10 \text{ mA}$	—	-1.8	—	mV/ $^\circ\text{C}$
Input reverse current	I_R		—	$V_R = 5 \text{ V}$, $T_a = 25^\circ\text{C}$	—	—	10	μA
Input capacitance	C_t		—	$V = 0 \text{ V}$, $f = 1 \text{ MHz}$, $T_a = 25^\circ\text{C}$	—	60	—	pF
Peak high-level output current	I_{OPH}	(Note 1)	Fig. 12.1.1	$I_F = 10 \text{ mA}$, $V_{CC} = 15 \text{ V}$, $V_{6-5} = 4 \text{ V}$	—	-0.32	-0.2	A
				$I_F = 10 \text{ mA}$, $V_{CC} = 15 \text{ V}$, $V_{6-5} = 10 \text{ V}$	—	-0.6	-0.4	
Peak low-level output current	I_{OPL}	(Note 1)	Fig. 12.1.2	$I_F = 0 \text{ mA}$, $V_{CC} = 15 \text{ V}$, $V_{5-4} = 2 \text{ V}$	0.2	0.32	—	A
				$I_F = 0 \text{ mA}$, $V_{CC} = 15 \text{ V}$, $V_{5-4} = 10 \text{ V}$	0.4	0.6	—	
High-level output voltage	V_{OH}		Fig. 12.1.3	$I_F = 10 \text{ mA}$, $V_{CC} = 10 \text{ V}$, $I_O = -100 \text{ mA}$	6.0	8.5	—	V
Low-level output voltage	V_{OL}		Fig. 12.1.4	$V_F = 0.8 \text{ V}$, $V_{CC} = 10 \text{ V}$, $I_O = 100 \text{ mA}$	—	0.35	1.0	V
High-level supply current	I_{CCH}		Fig. 12.1.5	$I_F = 10 \text{ mA}$, $V_{CC} = 10$ to 30 V , $V_O = \text{Open}$	—	—	3.0	mA
Low-level supply current	I_{CCL}		Fig. 12.1.6	$I_F = 0 \text{ mA}$, $V_{CC} = 10$ to 30 V , $V_O = \text{Open}$	—	—	3.0	
Threshold input current (L/H)	I_{FLH}		—	$V_{CC} = 15 \text{ V}$, $V_O > 1 \text{ V}$	—	—	7.5	V
Threshold input voltage (H/L)	V_{FHL}		—	$V_{CC} = 15 \text{ V}$, $V_O < 1 \text{ V}$	0.8	—	—	
Supply voltage	V_{CC}		—	—	10	—	30	V

Note: All typical values are at $T_a = 25^\circ\text{C}$.

Note: This device is designed for low power consumption, making it more sensitive to ESD than its predecessors.

Extra care should be taken in the design of circuitry and pc board implementation to avoid ESD problems.

Note 1: I_O application time $\leq 50 \mu\text{s}$, single pulse.

10. Isolation Characteristics (Unless otherwise specified, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Note	Test Conditions	Min	Typ.	Max	Unit
Total capacitance (input to output)	C_S	(Note 1)	$V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$	—	1.0	—	pF
Isolation resistance	R_S	(Note 1)	$V_S = 500 \text{ V}$, R.H. $\leq 60\%$	1×10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	(Note 1)	AC, 1 min	5000	—	—	Vrms
			AC, 1 s, in oil	—	10000	—	
			DC, 1 min, in oil	—	10000	—	Vdc

Note 1: This device is considered as a two-terminal device: Pins 1, 2 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

11. Switching Characteristics (Note)
(Unless otherwise specified, $T_a = -40$ to 100°C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (L/H)	t_{pLH}	(Note 1)	Fig. 12.1.7	$I_F = 0 \rightarrow 10 \text{ mA}$, $V_{CC} = 20 \text{ V}$, $R_g = 30 \Omega$, $C_g = 1 \text{ nF}$, $T_a = 25^\circ\text{C}$	—	125	170	ns
Propagation delay time (H/L)	t_{pHL}	(Note 1)		$I_F = 10 \rightarrow 0 \text{ mA}$, $V_{CC} = 20 \text{ V}$, $R_g = 30 \Omega$, $C_g = 1 \text{ nF}$, $T_a = 25^\circ\text{C}$	—	120	170	
Propagation delay time (L/H)	t_{pLH}	(Note 1)		$I_F = 0 \rightarrow 10 \text{ mA}$, $V_{CC} = 20 \text{ V}$, $R_g = 30 \Omega$, $C_g = 1 \text{ nF}$	50	125	200	
Propagation delay time (H/L)	t_{pHL}	(Note 1)		$I_F = 10 \rightarrow 0 \text{ mA}$, $V_{CC} = 20 \text{ V}$, $R_g = 30 \Omega$, $C_g = 1 \text{ nF}$	50	120	200	
Propagation delay skew (device to device)	t_{psk}	(Note 1) (Note 4)		$I_F = 0 \leftrightarrow 10 \text{ mA}$, $V_{CC} = 20 \text{ V}$, $R_g = 30 \Omega$, $C_g = 1 \text{ nF}$	-85	—	85	
Pulse width distortion	$ t_{pHL} - t_{pLH} $	(Note 1)		$I_F = 0 \leftrightarrow 10 \text{ mA}$, $V_{CC} = 20 \text{ V}$, $R_g = 30 \Omega$, $C_g = 1 \text{ nF}$	—	5	50	
Rise time	t_r	(Note 1)		$I_F = 0 \rightarrow 10 \text{ mA}$, $V_{CC} = 20 \text{ V}$, $R_g = 30 \Omega$, $C_g = 1 \text{ nF}$	—	35	—	
Fall time	t_f	(Note 1)		$I_F = 10 \rightarrow 0 \text{ mA}$, $V_{CC} = 20 \text{ V}$, $R_g = 30 \Omega$, $C_g = 1 \text{ nF}$	—	15	—	
Common-mode transient immunity at output high	CM_H	(Note 2)	Fig. 12.1.8	$V_{CM} = 1000 V_{p-p}$, $I_F = 10 \text{ mA}$, $V_{CC} = 20 \text{ V}$, $T_a = 25^\circ\text{C}$, $V_{O(min)} = 16 \text{ V}$	± 20	—	—	kV/ μs
Common-mode transient immunity at output low	CM_L	(Note 3)		$V_{CM} = 1000 V_{p-p}$, $I_F = 0 \text{ mA}$, $V_{CC} = 20 \text{ V}$, $T_a = 25^\circ\text{C}$, $V_{O(max)} = 1 \text{ V}$	± 20	—	—	

Note: All typical values are at $T_a = 25^\circ\text{C}$.

Note 1: Input signal ($f = 250 \text{ kHz}$, duty = 50%, $t_r = t_f = 5 \text{ ns}$ or less).

CL is approximately 15 pF which includes probe and stray wiring capacitance.

Note 2: CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 16 \text{ V}$).

Note 3: CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 1 \text{ V}$).

Note 4: The propagation delay skew, t_{psk} , is equal to the magnitude of the worst-case difference in t_{pHL} and/or t_{pLH} that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

12. Test Circuits and Characteristics Curves

12.1. Test Circuits

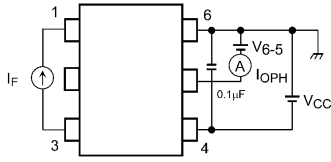


Fig. 12.1.1 IOPH Test Circuit

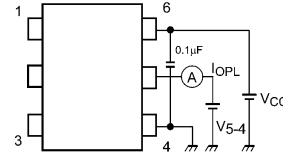


Fig. 12.1.2 IOL Test Circuit

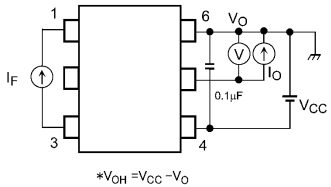


Fig. 12.1.3 VOH Test Circuit

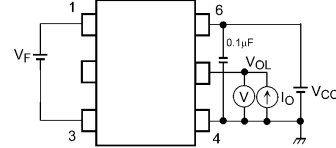


Fig. 12.1.4 VOL Test Circuit

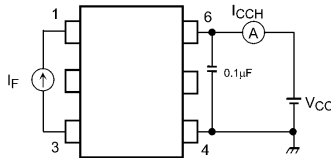


Fig. 12.1.5 ICCH Test Circuit

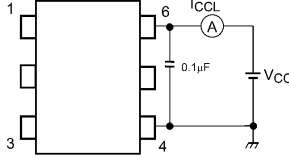


Fig. 12.1.6 ICCL Test Circuit

$I_F = 10 \text{ mA (P.G.)}$
 $(f = 250 \text{ kHz, duty} = 50\%, t_r = t_f = 5 \text{ ns or less})$

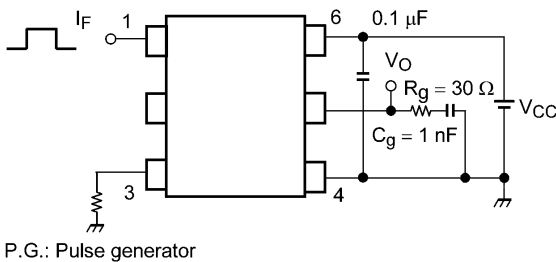


Fig. 12.1.7 Switching Time Test Circuit and Waveform

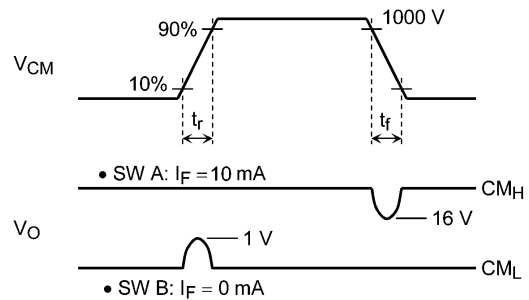
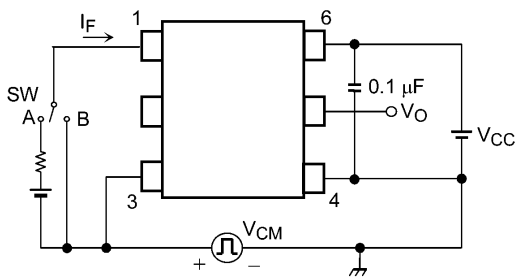


Fig. 12.1.8 Common-Mode Transient Immunity Test Circuit and Waveform

$$CM_H = -\frac{800 \text{ V}}{t_f (\mu\text{s})} \quad CM_L = \frac{800 \text{ V}}{t_r (\mu\text{s})}$$

12.2. Characteristics Curves (Note)

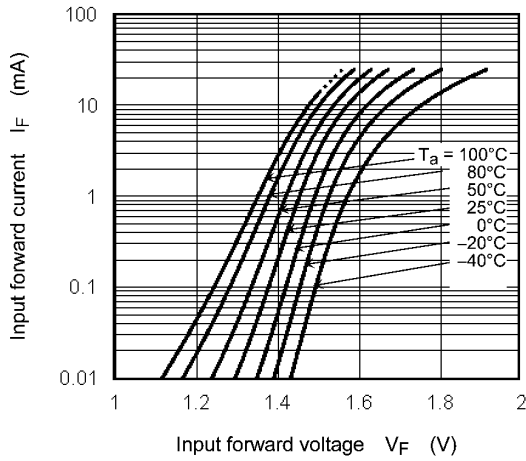


Fig. 12.2.1 $I_F - V_F$

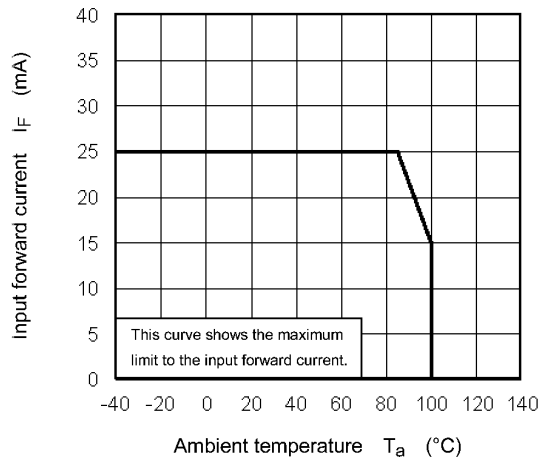


Fig. 12.2.2 $I_F - T_a$

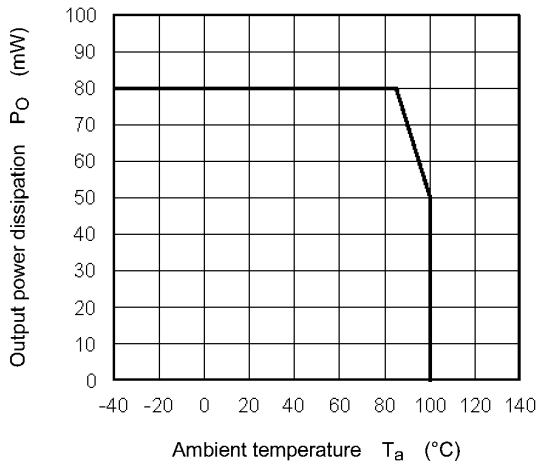


Fig. 12.2.3 $P_O - T_a$

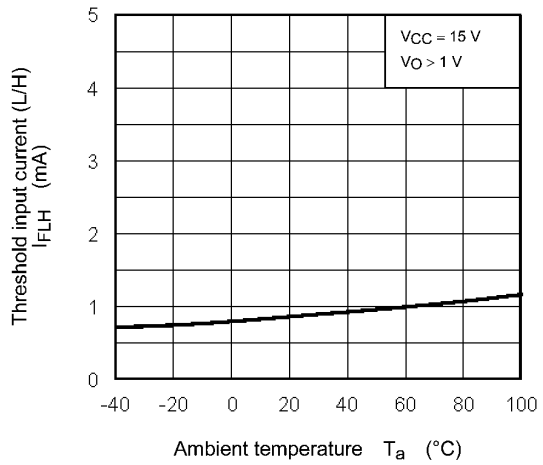


Fig. 12.2.4 $I_{FLH} - T_a$

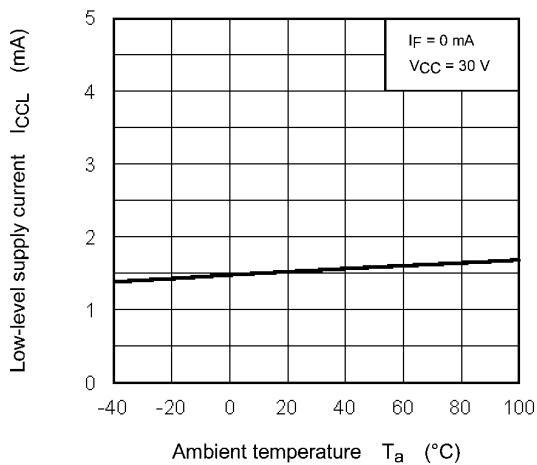


Fig. 12.2.5 $I_{CCL} - T_a$

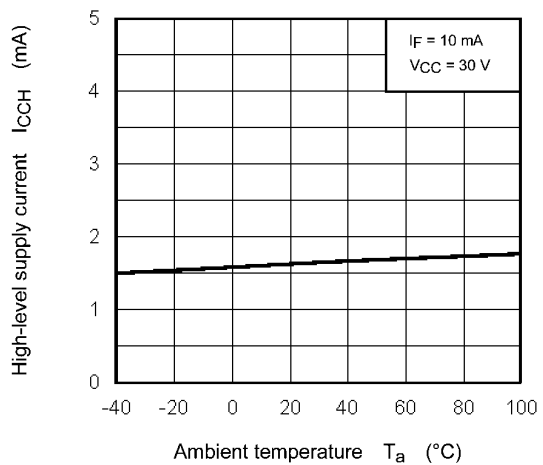


Fig. 12.2.6 $I_{CCH} - T_a$

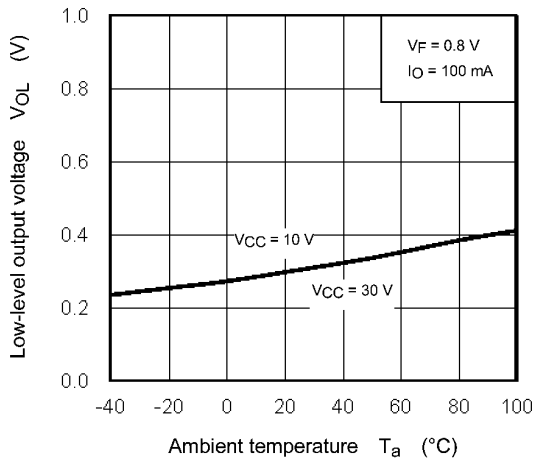


Fig. 12.2.7 $V_{OL} - T_a$

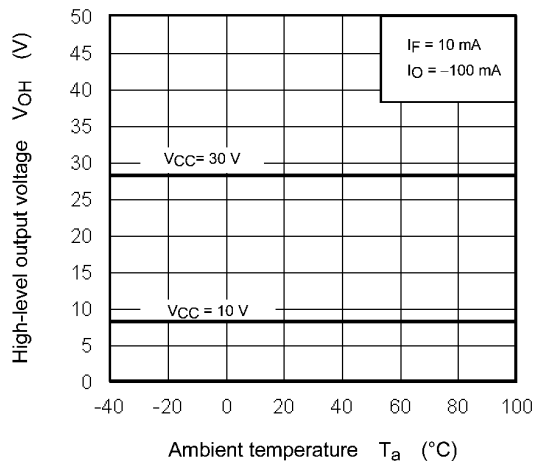


Fig. 12.2.8 $V_{OH} - T_a$

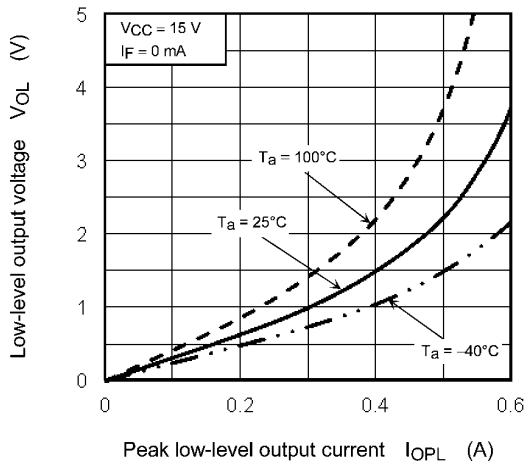


Fig. 12.2.9 $V_{OL} - I_{OPL}$

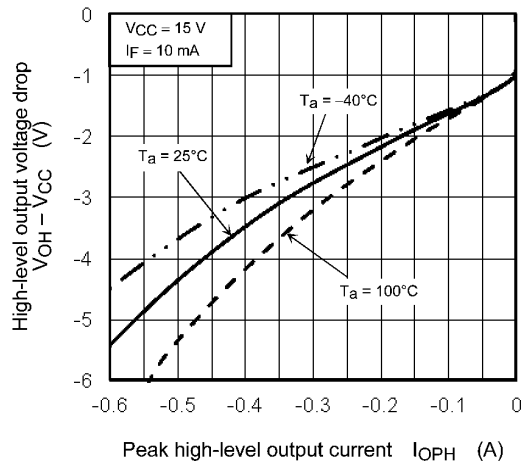


Fig. 12.2.10 $(V_{OH} - V_{CC}) - I_{OPH}$

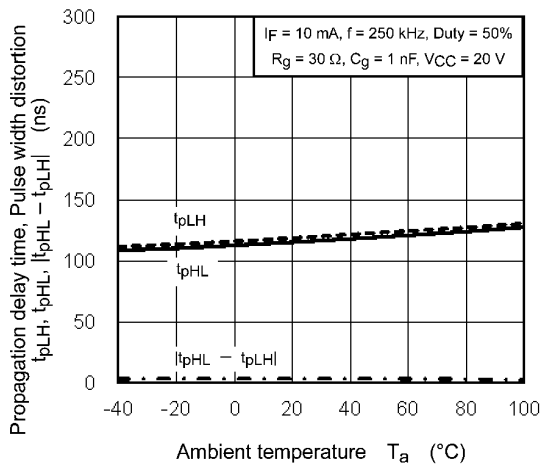


Fig. 12.2.11 $t_{pLH}, t_{pHL}, |t_{pHL} - t_{pLH}| - T_a$

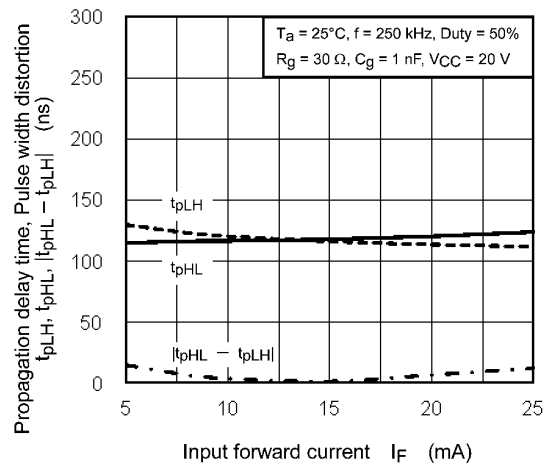


Fig. 12.2.12 $t_{pLH}, t_{pHL}, |t_{pHL} - t_{pLH}| - I_F$

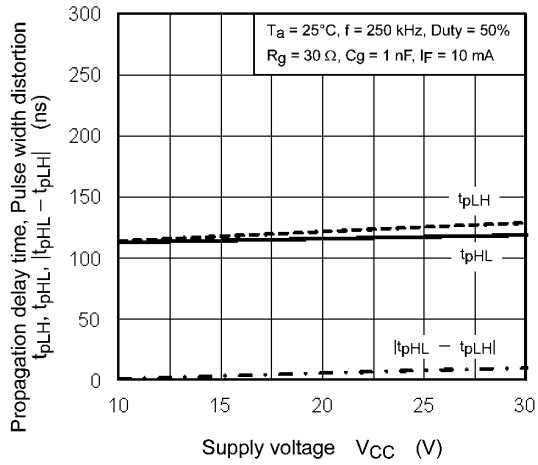


Fig. 12.2.13 $t_{pLH}, t_{pHL}, |t_{pHL} - t_{pLH}| - V_{CC}$

NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

13. Soldering and Storage

13.1. Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

- When using soldering reflow (See Fig. 13.1.1 and 13.1.2)

Reflow soldering must be performed once or twice.

The mounting should be completed with the interval from the first to the last mountings being 2 weeks.

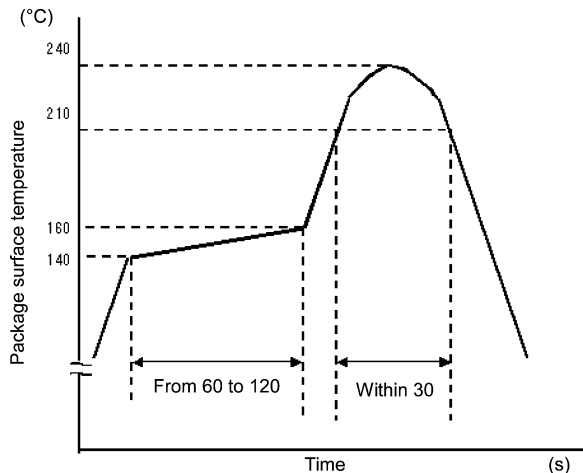


Fig. 13.1.1 An Example of a Temperature Profile When Sn-Pb Eutectic Solder Is Used

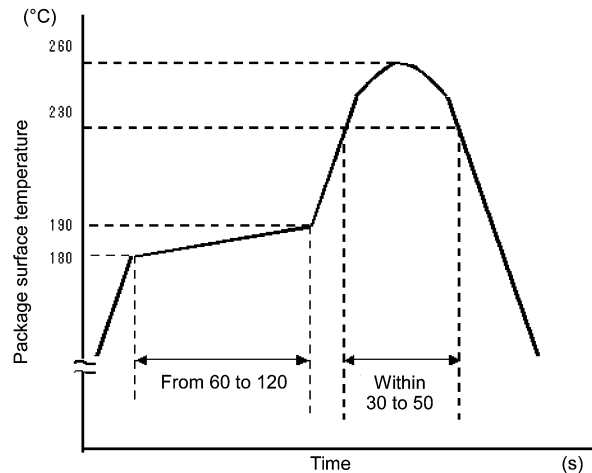


Fig. 13.1.2 An Example of a Temperature Profile When Lead(Pb)-Free Solder Is Used

- When using soldering flow (Applicable to both eutectic solder and Lead(Pb)-Free solder)
Apply preheating of 150°C for 60 to 120 seconds.
Mounting condition of 260°C within 10 seconds is recommended.
Flow soldering must be performed once.
- When using soldering Iron (Applicable to both eutectic solder and Lead(Pb)-Free solder)
Complete soldering within 10 seconds for lead temperature not exceeding 260°C or within 3 seconds not exceeding 350°C
Heating by soldering iron must be done only once per lead.

13.2. Precautions for General Storage

- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5°C to 35°C and 45% to 75%, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

14. Land Pattern Dimensions for Reference Only

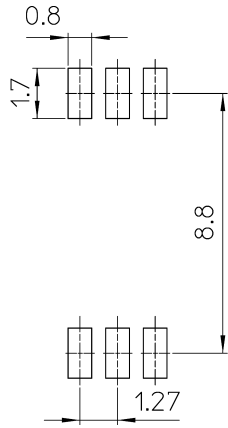


Fig. 14.1 7.62 mm Pitch (unit: mm)

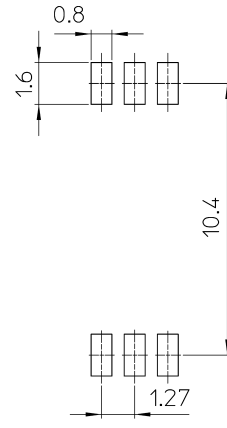


Fig. 14.2 10.16 mm Pitch (unit: mm)

15. Marking

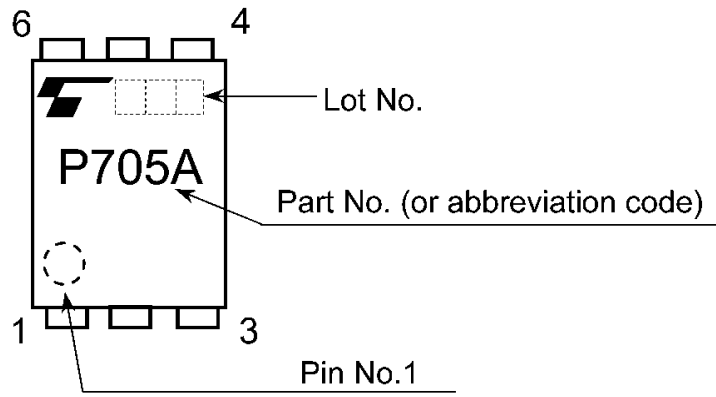


Fig. 15.1 Marking

16. EN60747-5-2 Option (D4) Specification

- Part number: TLP705A, TLP705AF (Note)
- The following part naming conventions are used for the devices that have been qualified according to option (D4) of EN60747.

Example: TLP705A(D4-TP, F)

D4: EN60747 option

TP: Tape type

F: [[G]]/RoHS COMPATIBLE (Note 1)

Note: Use TOSHIBA standard type number for safety standard application.

e.g., TLP705A(D4-TP,F) → TLP705A

Note 1: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.

RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronics equipment.

Description		Symbol	Rating	Unit
Application classification			I-IV I-III	—
for rated mains voltage ≤ 300 Vrms for rated mains voltage ≤ 600 Vrms				
Climatic classification			40/100/21	—
Pollution degree			2	—
Maximum operating insulation voltage	TLPxxx type	V_{IORM}	890	Vpeak
	TLPxxxF type		1140	
Input to output test voltage, method A $V_{pr} = 1.5 \times V_{IORM}$, type and sample test $t_p = 10$ s, partial discharge < 5 pC	TLPxxx type	V_{pr}	1335	Vpeak
	TLPxxxF type		1710	
Input to output test voltage, method B $V_{pr} = 1.875 \times V_{IORM}$, 100% production test $t_p = 1$ s, partial discharge < 5 pC	TLPxxx type	V_{pr}	1670	Vpeak
	TLPxxxF type		2140	
Highest permissible overvoltage (transient overvoltage, $t_{pr} = 60$ s)		V_{TR}	8000	Vpeak
Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve)				
current (input current I_F , $P_{so} = 0$)		I_s	300	mA
power (output or total power dissipation)		P_{so}	700	mW
temperature		T_s	150	°C
Insulation resistance, Input-output	$V_{IO} = 500$ V, $T_a = 25^\circ\text{C}$ $V_{IO} = 500$ V, $T_a = 100^\circ\text{C}$ $V_{IO} = 500$ V, $T_a = T_s$	R_{si}	$\geq 10^{12}$ $\geq 10^{11}$ $\geq 10^9$	Ω

Fig. 16.1 EN60747 Isolation Characteristics



		 7.62-mm pitch TLPxxx type	 10.16-mm pitch TLPxxxF type
Minimum creepage distance	Cr	7.0 mm	8.0 mm
Minimum clearance	Cl	7.0 mm	8.0 mm
Minimum insulation thickness	ti	0.4 mm	
Comparative tracking index	CTI	175	

Fig. 16.2 Insulation Related Specifications (Note)

Note: If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. (e. g., at a standard distance between soldering eye centers of 3.5 mm). If this is not permissible, the user shall take suitable measures.

Note: This photocoupler is suitable for **safe electrical isolation** only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

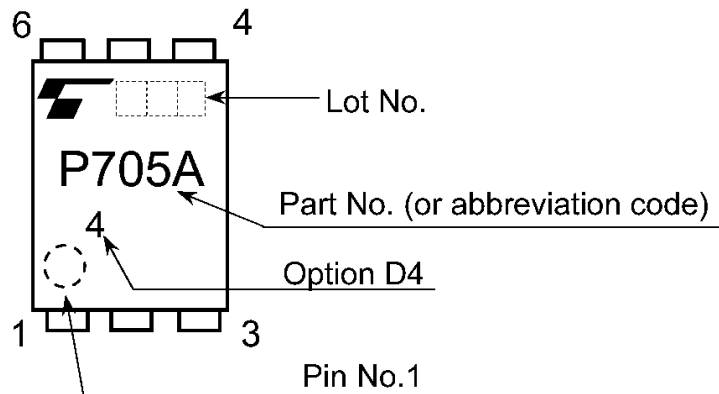


Fig. 16.3 Marking Example (Note)

Note: The above marking is applied to the photocouplers that have been qualified according to option (D4) of EN60747.

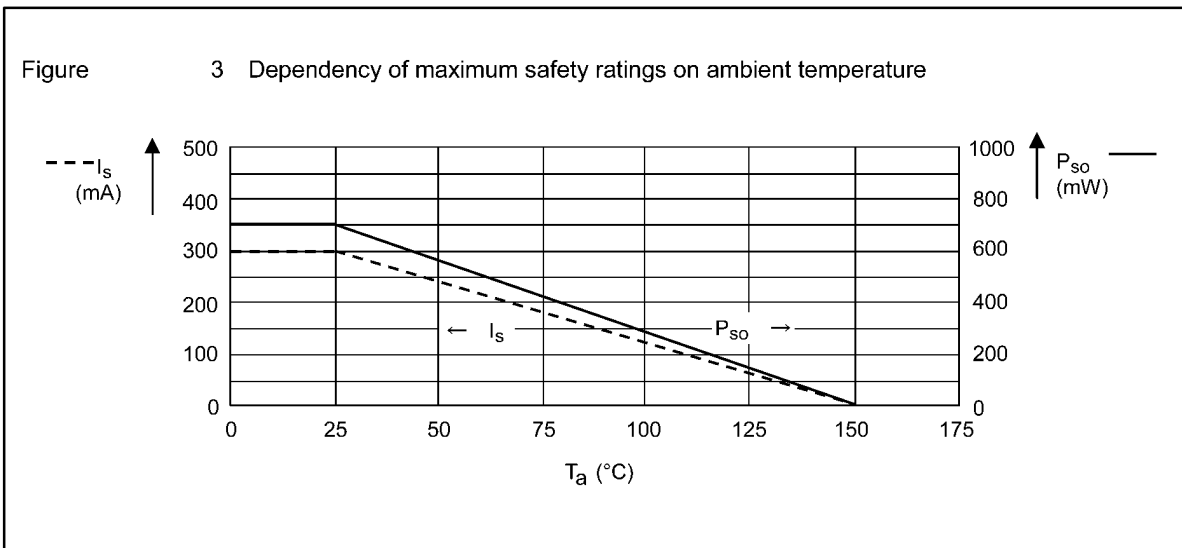
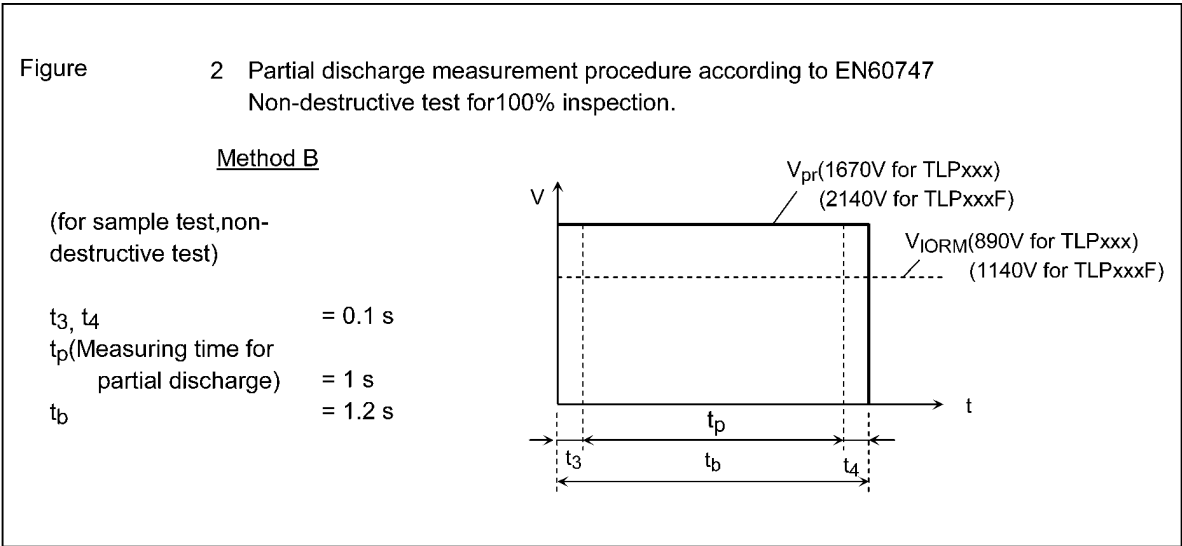
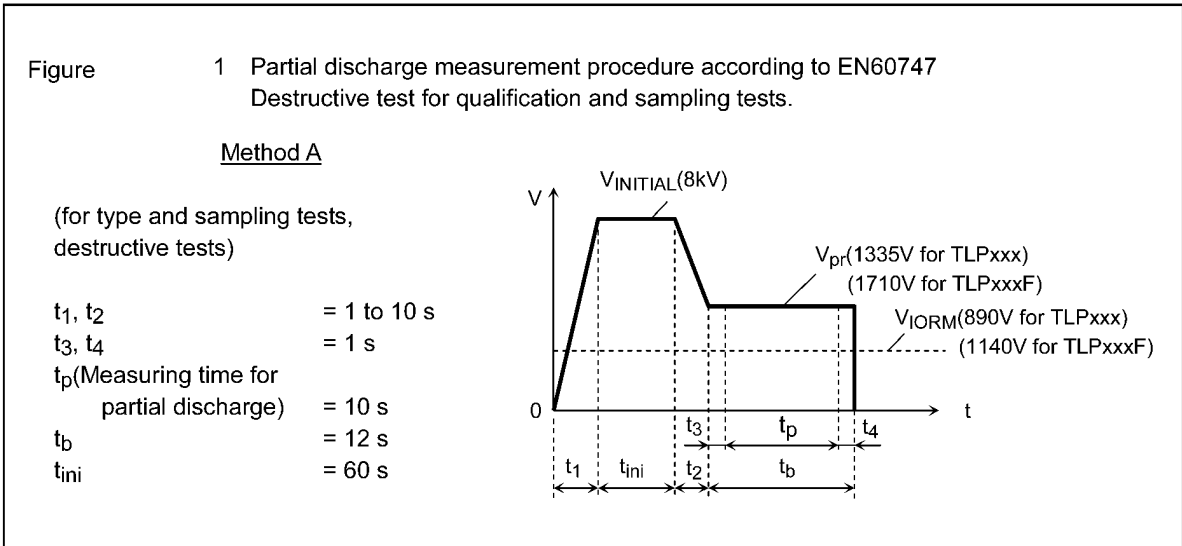
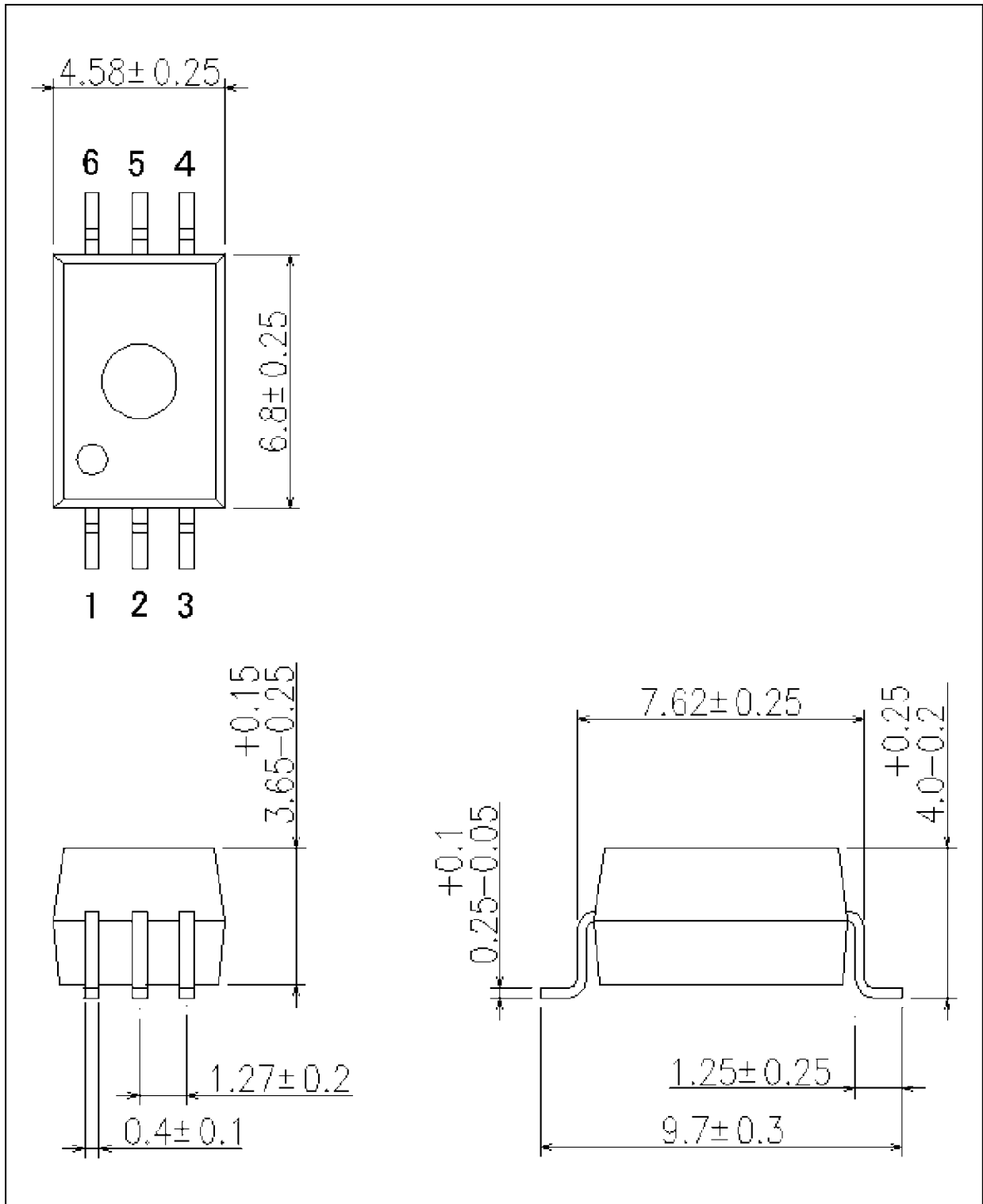


Fig. 16.4 Measurement Procedure

Package Dimensions

Unit: mm



Weight: 0.26 g (typ.)

Package Name(s)
TOSHIBA: 11-5J1S

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