



ADG611/ADG612/ADG613

FEATURES

- 1 pC charge injection
- ± 2.7 V to ± 5.5 V dual-supply operation
- +2.7 V to +5.5 V single-supply operation
- Automotive temperature range: -40°C to $+125^{\circ}\text{C}$
- 100 pA maximum at 25°C leakage currents
- 85 Ω on resistance
- Rail-to-rail switching operation
- Fast switching times
- 16-lead TSSOP and SOIC packages
- Typical power consumption: <0.1 μW
- TTL-/CMOS-compatible inputs

APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Communications systems
- Sample-and-hold systems
- Audio signal routing
- Relay replacement
- Avionics

GENERAL DESCRIPTION

The ADG611/ADG612/ADG613 are monolithic CMOS devices containing four independently selectable switches. These switches offer ultralow charge injection of 1 pC over the full input signal range and typical leakage currents of 10 pA at 25°C .

The devices are fully specified for ± 5 V, +5 V, and +3 V supplies. Each contains four independent single-pole, single-throw (SPST) switches. The ADG611 and ADG612 differ only in that the digital control logic is inverted. The ADG611 switches are turned on with a logic low on the appropriate control input, whereas a logic high is required to turn on the switches of the ADG612. The ADG613 contains two switches with digital control logic similar to that of the ADG611 and two switches in which the logic is inverted.

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. SWITCHES SHOWN FOR A LOGIC 1 INPUT.

Figure 1.

02753-001

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The ADG613 exhibits break-before-make switching action. The ADG611/ADG612/ADG613 are available in a small, 16-lead TSSOP package, and the ADG611 is also available in a 16-lead SOIC package.

PRODUCT HIGHLIGHTS

1. Ultralow charge injection (1 pC typically).
2. Dual ± 2.7 V to ± 5.5 V or single +2.7 V to +5.5 V operation.
3. Automotive temperature range: -40°C to $+125^{\circ}\text{C}$.
4. Small, 16-lead TSSOP and SOIC packages.

Rev. A

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REVISION HISTORY

11/09—Rev. 0 to Rev. A

| | |
|--|----|
| Changes to Analog Signal Range Parameter and to On Resistance, R_{ON} Parameter, Table 1..... | 3 |
| Change to Digital Input Capacitance, C_{IN} Parameter, Table 2.... | 4 |
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| Added Table 5; Renumbered Sequentially | 7 |
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1/02—Revision 0: Initial Version

SPECIFICATIONS

DUAL-SUPPLY OPERATION

$V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C ¹ | Unit | Test Conditions/Comments |
|--|------------|----------------|------------------------------|-------------------|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | V_{SS} to V_{DD} | V | |
| On Resistance, R_{ON} | 85 | | | Ω typ | $V_S = \pm 3\text{ V}$, $I_S = -1\text{ mA}$; see Figure 14 |
| | 115 | 140 | 160 | Ω max | $V_S = \pm 3\text{ V}$, $I_S = -1\text{ mA}$; see Figure 14 |
| On-Resistance Match Between Channels, ΔR_{ON} | 2 | | | Ω typ | $V_S = \pm 3\text{ V}$, $I_S = -1\text{ mA}$ |
| On-Resistance Flatness, $R_{FLAT(ON)}$ | 4 | 5.5 | 6.5 | Ω max | $V_S = \pm 3\text{ V}$, $I_S = -1\text{ mA}$ |
| | 25 | | | Ω typ | $V_S = \pm 3\text{ V}$, $I_S = -1\text{ mA}$ |
| | 40 | 55 | 60 | Ω max | $V_S = \pm 3\text{ V}$, $I_S = -1\text{ mA}$ |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, $I_{S(OFF)}$ | ± 0.01 | | | nA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ $V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$; see Figure 15 |
| | ± 0.1 | ± 0.25 | ± 2 | nA max | $V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$; see Figure 15 |
| Drain Off Leakage, $I_{D(OFF)}$ | ± 0.01 | | | nA typ | $V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$; see Figure 15 |
| | ± 0.1 | ± 0.25 | ± 2 | nA max | $V_D = \pm 4.5\text{ V}$, $V_S = \mp 4.5\text{ V}$; see Figure 15 |
| Channel On Leakage, $I_{D(ON)}$, $I_{S(ON)}$ | ± 0.01 | | | nA typ | $V_D = V_S = \pm 4.5\text{ V}$; see Figure 16 |
| | ± 0.1 | ± 0.25 | ± 6 | nA max | $V_D = V_S = \pm 4.5\text{ V}$; see Figure 16 |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | | ± 0.1 | μA max | $V_{IN} = V_{INL}$ or V_{INH} |
| Digital Input Capacitance, C_{IN} | 2 | | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | | |
| t_{ON} | 45 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3.0\text{ V}$; see Figure 17 |
| | 65 | 75 | 90 | ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3.0\text{ V}$; see Figure 17 |
| t_{OFF} | 25 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3.0\text{ V}$; see Figure 17 |
| | 40 | 45 | 50 | ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3.0\text{ V}$; see Figure 17 |
| Break-Before-Make Time Delay, t_{BBM} | 15 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3.0\text{ V}$; see Figure 18 |
| | | | 10 | ns min | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3.0\text{ V}$; see Figure 18 |
| Charge Injection | -0.5 | | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 19 |
| Off Isolation | -65 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; see Figure 20 |
| Channel-to-Channel Crosstalk | -90 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; see Figure 21 |
| -3 dB Bandwidth | 680 | | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 22 |
| $C_{S(OFF)}$ | 5 | | | pF typ | $f = 1\text{ MHz}$ |
| $C_{D(OFF)}$ | 5 | | | pF typ | $f = 1\text{ MHz}$ |
| $C_{D(ON)}$, $C_{S(ON)}$ | 5 | | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.001 | | | μA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ Digital inputs = 0 V or 5.5 V |
| | | | 1.0 | μA max | Digital inputs = 0 V or 5.5 V |
| I_{SS} | 0.001 | | | μA typ | Digital inputs = 0 V or 5.5 V |
| | | | 1.0 | μA max | Digital inputs = 0 V or 5.5 V |

¹ The temperature range for the Y version is -40°C to +125°C.

² Guaranteed by design; not subject to production test.

ADG611/ADG612/ADG613

SINGLE-SUPPLY OPERATION

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C ¹ | Unit | Test Conditions/Comments |
|--|------------|----------------|------------------------------|-------------------|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 to V_{DD} | V | |
| On Resistance, R_{ON} | 210 | | | Ω typ | $V_S = 3.5\text{ V}$, $I_S = -1\text{ mA}$; see Figure 14 |
| | 290 | 350 | 380 | Ω max | $V_S = 3.5\text{ V}$, $I_S = -1\text{ mA}$; see Figure 14 |
| On-Resistance Match Between Channels, ΔR_{ON} | 3 | | | Ω typ | $V_S = 3.5\text{ V}$, $I_S = -1\text{ mA}$ |
| | 10 | 12 | 13 | Ω max | $V_S = 3.5\text{ V}$, $I_S = -1\text{ mA}$ |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, $I_{S(OFF)}$ | ± 0.01 | | | nA typ | $V_{DD} = 5.5\text{ V}$ $V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 15 |
| | ± 0.1 | ± 0.25 | ± 2 | nA max | $V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 15 |
| Drain Off Leakage, $I_{D(OFF)}$ | ± 0.01 | | | nA typ | $V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 15 |
| | ± 0.1 | ± 0.25 | ± 2 | nA max | $V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 15 |
| Channel On Leakage, $I_{D(ON)}$, $I_{S(ON)}$ | ± 0.01 | | | nA typ | $V_S = V_D = 1\text{ V}$ or 4.5 V ; see Figure 16 |
| | ± 0.1 | ± 0.25 | ± 6 | nA max | $V_S = V_D = 1\text{ V}$ or 4.5 V ; see Figure 16 |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | | ± 0.1 | μA max | $V_{IN} = V_{INL}$ or V_{INH} |
| Digital Input Capacitance, C_{IN} | 2 | | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | | |
| t_{ON} | 70 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3.0\text{ V}$; see Figure 17 |
| | 100 | 130 | 150 | ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3.0\text{ V}$; see Figure 17 |
| t_{OFF} | 25 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3.0\text{ V}$; see Figure 17 |
| | 40 | 45 | 50 | ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3.0\text{ V}$; see Figure 17 |
| Break-Before-Make Time Delay, t_{BBM} | 25 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3.0\text{ V}$; see Figure 18 |
| | | | 10 | ns min | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3.0\text{ V}$; see Figure 18 |
| Charge Injection | 1 | | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 19 |
| Off Isolation | −62 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; see Figure 20 |
| Channel-to-Channel Crosstalk | −90 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; see Figure 21 |
| −3 dB Bandwidth | 680 | | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 22 |
| $C_{S(OFF)}$ | 5 | | | pF typ | $f = 1\text{ MHz}$ |
| $C_{D(OFF)}$ | 5 | | | pF typ | $f = 1\text{ MHz}$ |
| $C_{D(ON)}$, $C_{S(ON)}$ | 5 | | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.001 | | | μA typ | $V_{DD} = 5.5\text{ V}$ Digital inputs = 0 V or 5.5 V |
| | | | 1.0 | μA max | Digital inputs = 0 V or 5.5 V |

¹ The temperature range for the Y version is -40°C to $+125^\circ\text{C}$.

² Guaranteed by design; not subject to production test.

$V_{DD} = 3\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

| Parameter | +25°C | -40°C to +85°C | -40°C to +125°C ¹ | Unit | Test Conditions/Comments |
|---|------------|----------------|------------------------------|-------------------|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 to V_{DD} | V | |
| On Resistance, R_{ON} | 380 | 420 | 460 | Ω typ | $V_S = 1.5\text{ V}$, $I_S = -1\text{ mA}$; see Figure 14 |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, $I_{S(OFF)}$ | ± 0.01 | | | nA typ | $V_{DD} = 3.3\text{ V}$ $V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$; see Figure 15 |
| | ± 0.1 | ± 0.25 | ± 2 | nA max | $V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$; see Figure 15 |
| Drain Off Leakage, $I_{D(OFF)}$ | ± 0.01 | | | nA typ | $V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$; see Figure 15 |
| | ± 0.1 | ± 0.25 | ± 2 | nA max | $V_S = 1\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/1\text{ V}$; see Figure 15 |
| Channel On Leakage, $I_{D(ON)}$, $I_{S(ON)}$ | ± 0.01 | | | nA typ | $V_S = V_D = 1\text{ V}$ or 3 V ; see Figure 16 |
| | ± 0.1 | ± 0.25 | ± 6 | nA max | $V_S = V_D = 1\text{ V}$ or 3 V ; see Figure 16 |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | | ± 0.1 | μA max | $V_{IN} = V_{INL}$ or V_{INH} |
| Digital Input Capacitance, C_{IN} | 2 | | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | | |
| t_{ON} | 130 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 2\text{ V}$; see Figure 17 |
| | 185 | 230 | 260 | ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 2\text{ V}$; see Figure 17 |
| t_{OFF} | 40 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 2\text{ V}$; see Figure 17 |
| | 55 | 60 | 65 | ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 2\text{ V}$; see Figure 17 |
| Break-Before-Make Time Delay, t_{BBM} | 50 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 2\text{ V}$; see Figure 18 |
| | | | 10 | ns min | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 2\text{ V}$; see Figure 18 |
| Charge Injection | 1.5 | | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 19 |
| Off Isolation | -62 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; see Figure 20 |
| Channel-to-Channel Crosstalk | -90 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 10\text{ MHz}$; see Figure 21 |
| -3 dB Bandwidth | 680 | | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 22 |
| $C_{S(OFF)}$ | 5 | | | pF typ | $f = 1\text{ MHz}$ |
| $C_{D(OFF)}$ | 5 | | | pF typ | $f = 1\text{ MHz}$ |
| $C_{D(ON)}$, $C_{S(ON)}$ | 5 | | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.001 | | | μA typ | $V_{DD} = 3.3\text{ V}$ Digital inputs = 0 V or 3.3 V |
| | | | 1.0 | μA max | Digital inputs = 0 V or 3.3 V |

¹ The temperature range for the Y version is -40°C to +125°C.

² Guaranteed by design; not subject to production test.

ADG611/ADG612/ADG613

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted

Table 4.

| Parameter | Rating |
|---|--|
| V _{DD} to V _{SS} | 13 V |
| V _{DD} to GND | −0.3 V to +6.5 V |
| V _{SS} to GND | +0.3 V to −6.5 V |
| Analog Inputs ¹ | V _{SS} − 0.3 V to V _{DD} + 0.3 V |
| Digital Inputs ¹ | GND − 0.3 V to V _{DD} + 0.3 V or 30 mA, whichever occurs first |
| Peak Current, S or D | 20 mA (pulsed at 1 ms, 10% duty cycle maximum) |
| Continuous Current, S or D | 10 mA |
| 3 V operation 85°C to 125°C | 7.5 mA |
| Operating Temperature Range Automotive (Y Version) | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| θ _{JA} Thermal Impedance | |
| 16-Lead TSSOP | 150.4°C/W |
| 16-Lead SOIC, 4-Layer Board | 80.6°C/W |
| Lead Soldering | |
| Lead Temperature, Soldering (10 sec) | 300°C |
| IR Reflow, Peak Temperature (<20 sec) | 220°C |
| (Pb-Free) Soldering | |
| Reflow, Peak Temperature | 260(+0/−5)°C |
| Time at Peak Temperature | 20 sec to 40 sec |

¹Overvoltages at IN, S, or D are clamped by internal diodes. The current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

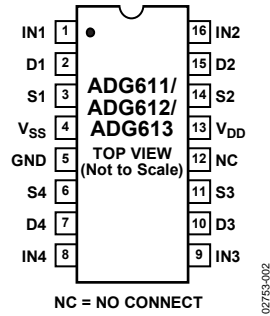


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-----------------|---|
| 1 | IN1 | Switch 1 Digital Control Input. |
| 2 | D1 | Drain Terminal of Switch 1. Can be an input or output. |
| 3 | S1 | Source Terminal of Switch 1. Can be an input or output. |
| 4 | V _{SS} | Most Negative Power Supply Terminal. Tie this pin to GND when using the device with single-supply voltages. |
| 5 | GND | Ground (0 V) Reference. |
| 6 | S4 | Source Terminal of Switch 4. Can be an input or output. |
| 7 | D4 | Drain Terminal of Switch 4. Can be an input or output. |
| 8 | IN4 | Switch 4 Digital Control Input. |
| 9 | IN3 | Switch 3 Digital Control Input. |
| 10 | D3 | Drain Terminal of Switch 3. Can be an input or output. |
| 11 | S3 | Source Terminal of Switch 3. Can be an input or output. |
| 12 | NC | Not Internally Connected. |
| 13 | V _{DD} | Most Positive Power Supply Terminal. |
| 14 | S2 | Source Terminal of Switch 2. Can be an input or output. |
| 15 | D2 | Drain Terminal of Switch 2. Can be an input or output. |
| 16 | IN2 | Switch 2 Digital Control Input. |

Table 6. ADG611/ADG612 Truth Table

| ADG611 Input | ADG612 Input | Switch Condition |
|--------------|--------------|------------------|
| 0 | 1 | On |
| 1 | 0 | Off |

Table 7. ADG613 Truth Table

| Logic | Switch 1, Switch 4 | Switch 2, Switch 3 |
|-------|--------------------|--------------------|
| 0 | Off | On |
| 1 | On | Off |

TYPICAL PERFORMANCE CHARACTERISTICS



Figure 3. On Resistance vs. V_D (V_S), Dual Supplies



Figure 6. On Resistance vs. V_D (V_S) for Various Temperatures, Single Supply



Figure 4. On Resistance vs. V_D (V_S), Single Supply



Figure 7. Leakage Current vs. Temperature, Dual Supplies



Figure 5. On Resistance vs. V_D (V_S) for Various Temperatures, Dual Supplies



Figure 8. Leakage Current vs. Temperature, Single Supply



Figure 9. Charge Injection vs. Source Voltage



Figure 12. Off Isolation vs. Frequency



Figure 10. t_{ON}/t_{OFF} Times vs. Temperature



Figure 13. Crosstalk vs. Frequency



Figure 11. On Response vs. Frequency

TERMINOLOGY

| | |
|---|--|
| V_{DD} Most positive power supply potential. | V_{INH} Minimum input voltage for Logic 1. |
| V_{SS} Most negative power supply potential. | I_{INL}, I_{INH} Input current of the digital input. |
| I_{DD} Positive supply current. | C_{S(OFF)} Off switch source capacitance. Measured with reference to ground. |
| I_{SS} Negative supply current. | C_{D(OFF)} Off switch drain capacitance. Measured with reference to ground. |
| GND Ground (0 V) reference. | C_{D(ON)}, C_{S(ON)} On switch capacitance. Measured with reference to ground. |
| S Source terminal. Can be an input or output. | C_{IN} Digital input capacitance. |
| D Drain terminal. Can be an input or output. | t_{ON} Delay between applying the digital control input and the output switching on (see Figure 17). |
| IN Logic control input. | t_{OFF} Delay between applying the digital control input and the output switching off (see Figure 17). |
| V_D (V_S) Analog voltage on Terminal D and Terminal S. | Charge Injection A measure of the glitch impulse transferred from the digital input to the analog output during switching. |
| R_{ON} Ohmic resistance between Terminal D and Terminal S. | Off Isolation A measure of unwanted signal coupling through an off switch. |
| ΔR_{ON} On-resistance match between any two channels, that is, R _{ONMAX} – R _{ONMIN} . | Crosstalk A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. |
| R_{FLAT(ON)} Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range. | On Response Frequency response of the on switch. |
| I_{S(OFF)} Source leakage current with the switch off. | Insertion Loss Loss due to the on resistance of the switch. |
| I_{D(OFF)} Drain leakage current with the switch off. | |
| I_{D(ON)}, I_{S(ON)} Channel leakage current with the switch on. | |
| V_{INL} Maximum input voltage for Logic 0. | |

TEST CIRCUITS

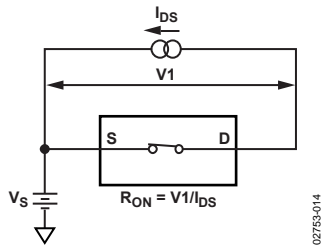


Figure 14. On Resistance

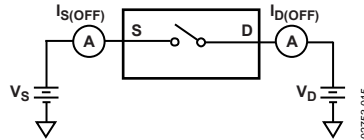


Figure 15. Off Leakage

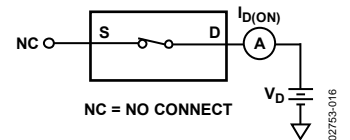


Figure 16. On Leakage

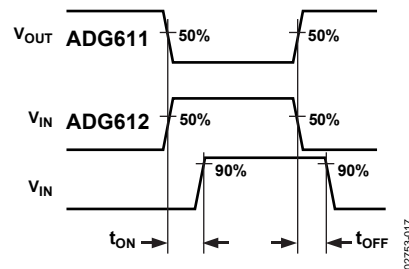
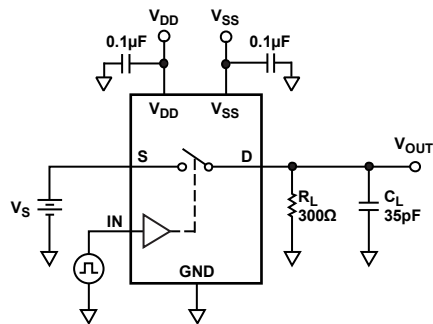


Figure 17. Switching Times

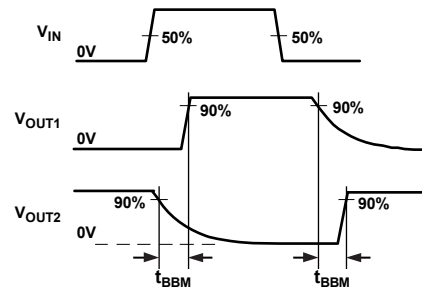
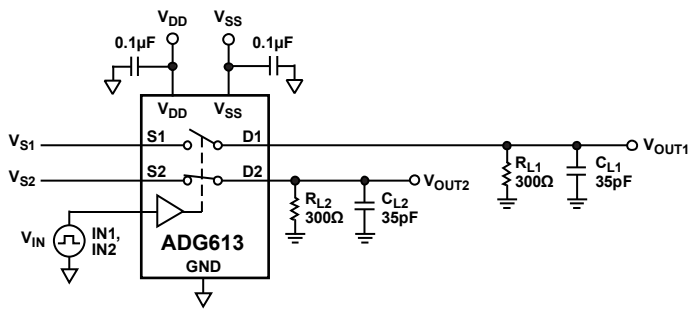


Figure 18. Break-Before-Make Time Delay

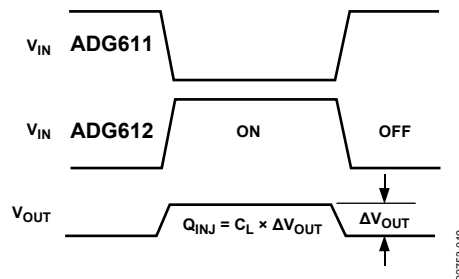
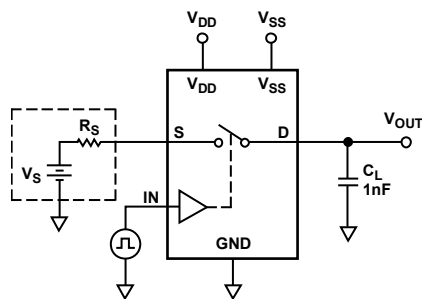


Figure 19. Charge Injection

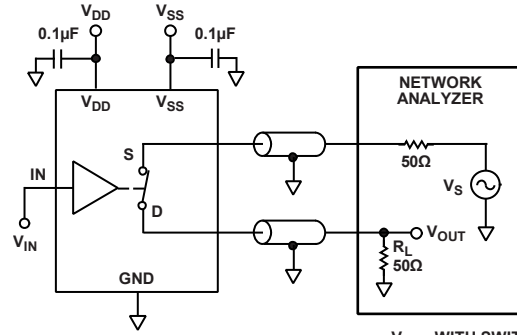
ADG611/ADG612/ADG613



$$\text{OFF ISOLATION} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

02753-020

Figure 20. Off Isolation



$$\text{INSERTION LOSS} = 20 \log \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

02753-022

Figure 22. Bandwidth



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log |V_s/V_{\text{OUT}}|$$

02753-021

Figure 21. Channel-to-Channel Crosstalk

APPLICATIONS INFORMATION

Figure 23 illustrates a photodetector circuit with programmable gain. With the resistor values shown in this figure, gains in the range of 2 to 16 can be achieved by using different combinations of switches.



Figure 23. Photodetector Circuit with Programmable Gain

02753-023

ADG611/ADG612/ADG613

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 24. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 25. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)

Dimensions shown in millimeters and (inches)

060606-A

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|-------------------------------|-------------------|---|----------------|
| ADG611YRUZ ¹ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG611YRUZ-REEL ¹ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG611YRUZ-REEL7 ¹ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG611YRZ ¹ | -40°C to +125°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG612YRUZ ¹ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG612YRUZ-REEL ¹ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG612YRUZ-REEL7 ¹ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG612WRUZ-REEL ¹ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG613YRUZ ¹ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG613YRUZ-REEL ¹ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG613YRUZ-REEL7 ¹ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |

¹ Z = RoHS Compliant Part.

NOTES

NOTES