# INA322
# INA2322

SBOS174B – DECEMBER 2000 – REVISED FEBRUARY 2006

# *micro*Power, Single-Supply, CMOS INSTRUMENTATION AMPLIFIER

## FEATURES

- LOW COST
- LOW QUIESCENT CURRENT: 40μA/channel
  Shut Down: < 1μA
- HIGH GAIN ACCURACY: G = 5, 0.07%, 2ppm/°C
- GAIN SET WITH EXTERNAL RESISTORS
- LOW BIAS CURRENT: 10pA
- BANDWIDTH: 500kHz, G = 5V/V
- RAIL-TO-RAIL OUTPUT SWING: (V+) – 0.02V
- WIDE TEMPERATURE RANGE:
  –55°C to +125°C
- SINGLE VERSION IN MSOP-8 PACKAGE AND DUAL VERSION IN TSSOP-14 PACKAGE

## APPLICATIONS

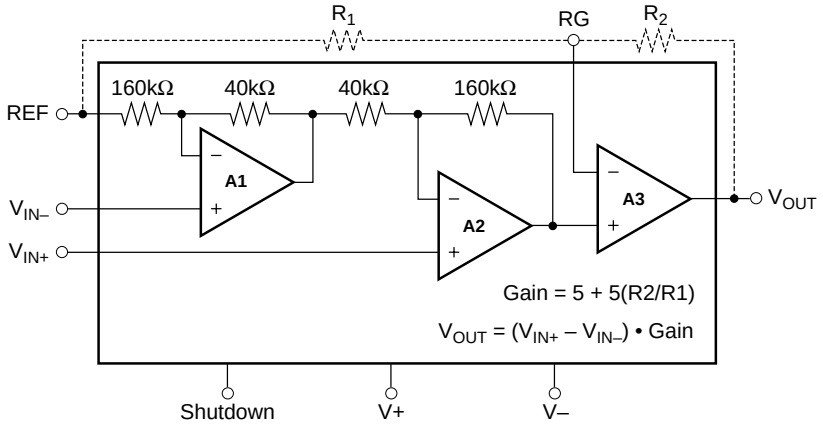
- INDUSTRIAL SENSOR AMPLIFIERS:
  Bridge, RTD, Thermistor, Position
- PHYSIOLOGICAL AMPLIFIERS:
  ECG, EEG, EMG
- A/D CONVERTER SIGNAL CONDITIONING
- DIFFERENTIAL LINE RECEIVERS WITH GAIN
- FIELD UTILITY METERS
- PCMCIA CARDS
- COMMUNICATION SYSTEMS
- TEST EQUIPMENT
- AUTOMOTIVE INSTRUMENTATION

## DESCRIPTION

The INA322 family is a series of low cost, rail-to-rail output, micropower CMOS instrumentation amplifiers that offer wide-range, single-supply, as well as bipolar-supply operation. The INA322 family provides low-cost, low-noise amplification of differential signals with micropower current consumption of 40μA. When shutdown the INA322 has a quiescent current of less than 1μA. Returning to normal operations within microseconds, the shutdown feature makes the INA322 optimal for low-power battery or multiplexing applications.

Configured internally for 5V/V gain, the INA322 offers exceptional flexibility with user-programmable external gain resistors. The INA322 reduces common-mode error over frequency and with CMRR remaining high up to 3kHz, line noise and line harmonics are rejected.

The low-power design does not compromise on bandwidth or slew rate, making the INA322 ideal for driving sampling Analog-to-Digital (A/D) converters as well as general-purpose applications. With high precision, low cost, and small packaging, the INA322 outperforms discrete designs, while offering reliability and performance.



## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| Supply Voltage, V+ to V– | 7.5V |
| Signal Input Terminals, Voltage(2) | (V–) – 0.5V to (V+) + 0.5V |
| Current(2) | 10mA |
| Output Short-Circuit(3) | Continuous |
| Operating Temperature | –65°C to +150°C |
| Storage Temperature | –65°C to +150°C |
| Junction Temperature | +150°C |

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION(1)

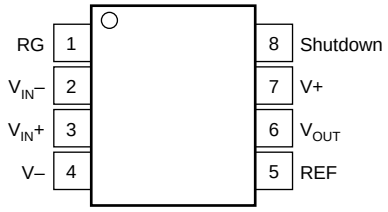
| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | PACKAGE MARKING |
|---|---|---|---|
| **SINGLE** INA322EA | MSOP-8 | DGK | C22 |
| **DUAL** INA2322EA | TSSOP-14 | PW | INA2322EA |

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## PIN CONFIGURATIONS

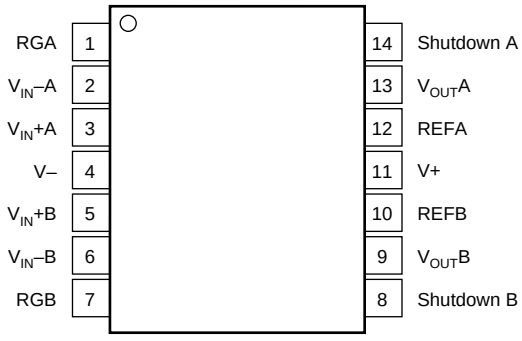
**Top View**

**INA322**




MSOP-8 (EA)

**INA2322**




Dual, TSSOP-14 (EA)

# ELECTRICAL CHARACTERISTICS: $V_S$ = +2.7V TO +5.5V

**BOLDFACE** limits apply over the specified temperature range, **$T_A$ = –55°C TO +125°C**

At $T_A$ = +25°C, $R_L$ = 25kΩ, G = 25, and $I_A$ common = $V_S$/2, unless otherwise noted.

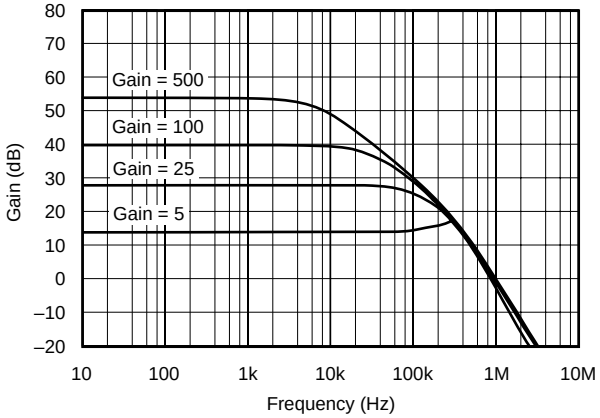
| PARAMETER | | CONDITION | INA322EA INA2322EA MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INPUT** | | | | | | |
| Input Offset Voltage, RTI | | $V_S$ = +5V | | ±2 | ±10 | mV |
| **Over Temperature** | **$V_{OS}$** | | | | **±11** | mV |
| **vs Temperature** | **$dV_{OS}/dT$** | | | **±7** | | µV/°C |
| vs Power Supply | PSRR | $V_S$ = +2.7V to +5.5V | | ±50 | ±250 | µV/V |
| **Over Temperature** | | | | | **±260** | µV/V |
| Long-Term Stability | | | | ±0.4 | | µV/month |
| Input Impedance | | | | $10^{13}$ \|\| 3 | | Ω \|\| pF |
| Input Common-Mode Range | | $V_S$ = 2.7V | 0.35 | | 1.5 | V |
| | | $V_S$ = 5V | 0.55 | | 3.8 | V |
| Common-Mode Rejection | CMRR | $V_S$ = 5V, $V_{CM}$ = 0.55V to 3.8V | 60 | 73 | | dB |
| **Over Temperature** | | **$V_S$ = 5V, $V_{CM}$ = 0.55V to 3.8V** | **60** | | | dB |
| | | $V_S$ = 2.7V, $V_{CM}$ = 0.35V to 1.5V | | 73 | | dB |
| Crosstalk, Dual | | | | 110 | | dB |
| **INPUT BIAS CURRENT** | | | | | | |
| Bias Current | $I_B$ | | | ±0.5 | ±10 | pA |
| Offset Current | $I_{OS}$ | | | ±0.5 | ±10 | pA |
| **NOISE, RTI** | **$e_n$** | **$R_S$ = 0Ω** | | | | |
| Voltage Noise: f = 10Hz | | | | 500 | | nV/√Hz |
| f = 100Hz | | | | 190 | | nV/√Hz |
| f = 1kHz | | | | 100 | | nV/√Hz |
| f = 0.1Hz to 10Hz | | | | 20 | | µVp-p |
| Current Noise: f = 1kHz | | | | 3 | | fA/√Hz |
| **GAIN**[1] | | | | | | |
| Gain Equation, Externally Set | | G > 5 | | G = 5 + 5(R2/R1) | | |
| Range of Gain | | | 5 | | 1000 | V/V |
| Gain Error | | | | ±0.07 | ±0.4 | % |
| **vs Temperature** | | **G = 5** | | **±2** | **±10** | ppm/°C |
| Nonlinearity | | G = 25, $V_S$ = 5V, $V_O$ = 0.05 to 4.95 | | ±0.001 | ±0.010 | % of FS |
| **Over Temperature** | | | | **±0.002** | **±0.015** | % of FS |
| **OUTPUT** | | | | | | |
| Output Voltage Swing from Rail[2, 5] | | G ≥ 10 | 50 | 25 | | mV |
| **Over Temperature** | | | **50** | | | mV |
| Capacitance Load Drive | | | | See Typical Characteristic[3] | | pF |
| Short-Circuit Current | $I_{SC–}$ | | | 8 | | |
| | $I_{SC+}$ | | | 16 | | mA |
| **FREQUENCY RESPONSE** | | | | | | |
| Bandwidth, –3dB | BW | G = 5 | | 500 | | kHz |
| Slew Rate | SR | $V_S$ = 5V, G = 25 | | 0.4 | | V/µs |
| Settling Time, 0.1% | $t_S$ | G = 5, $C_L$ = 50pF, $V_O$ = 2V step | | 8 | | µs |
| 0.01% | | | | 12 | | µs |
| Overload Recovery | | 50% Input Overload G = 25 | | 2 | | µs |
| **POWER SUPPLY** | | | | | | |
| Specified Voltage Range | | | +2.7 | | +5.5 | V |
| Operating Voltage Range | | | | +2.5 to +5.5 | | V |
| Quiescent Current per Channel | $I_Q$ | $V_{SD}$ > 2.5[4] | | 40 | 60 | µA |
| **Over Temperature** | | | | | **70** | µA |
| Shutdown Quiescent Current/Chan | $I_{SD}$ | $V_{SD}$ < 0.8[4] | | 0.01 | 1 | µA |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Range | | | –55 | | +125 | °C |
| Operating/Storage Range | | | –65 | | +150 | °C |
| Thermal Resistance | $\theta_{JA}$ | MSOP-8, TSSOP-14 Surface Mount | | 150 | | °C/W |

NOTES: (1) Does not include errors from external gain setting resistors (2) Output voltage swings are measured between the output and power-supply rails. Output swings and rail only if G ≥ 10. (3) See typical characteristic *Percent Overshoot vs Load Capacitance*. (4) See typical characteristic *Shutdown Voltage vs Supply Voltage*. (5) Output does not swing to positive rail if gain is less than 10.

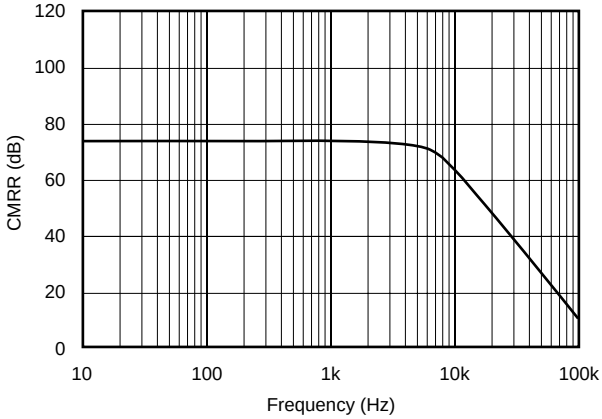
# TYPICAL CHARACTERISTICS

At $T_A$ = +25°C, $V_S$ = 5V, $V_{CM}$ = 1/2$V_S$, $R_L$ = 25kΩ, $C_L$ = 50pF, unless otherwise noted.

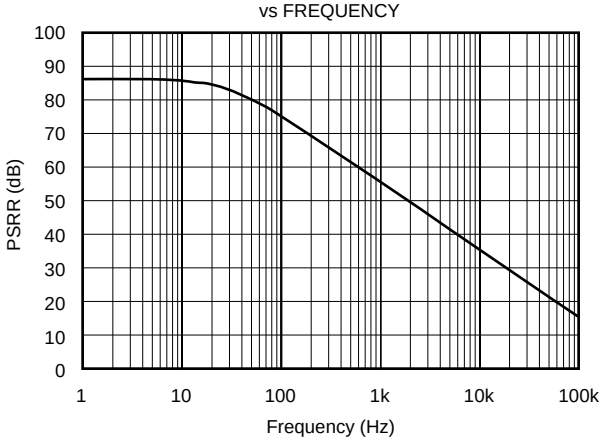
GAIN vs FREQUENCY



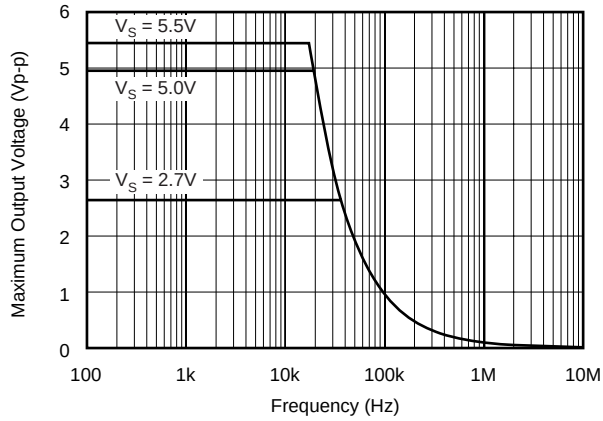

COMMON-MODE REJECTION RATIO vs FREQUENCY



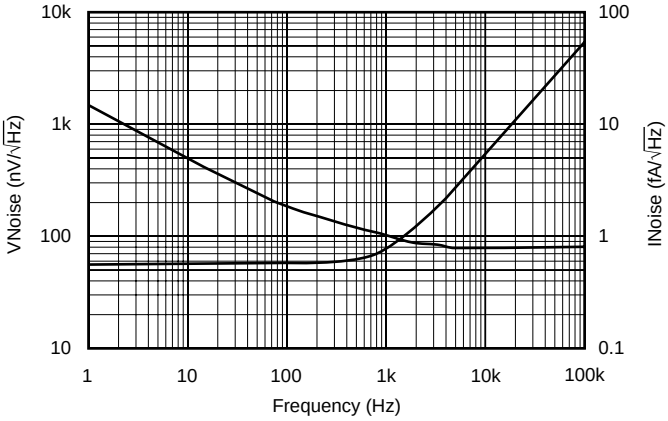

POWER-SUPPLY REJECTION RATIO vs FREQUENCY



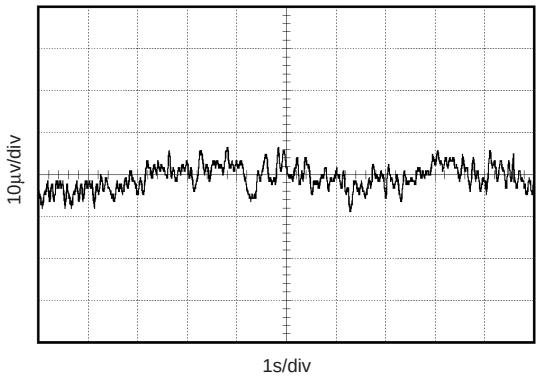

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY




NOISE vs FREQUENCY



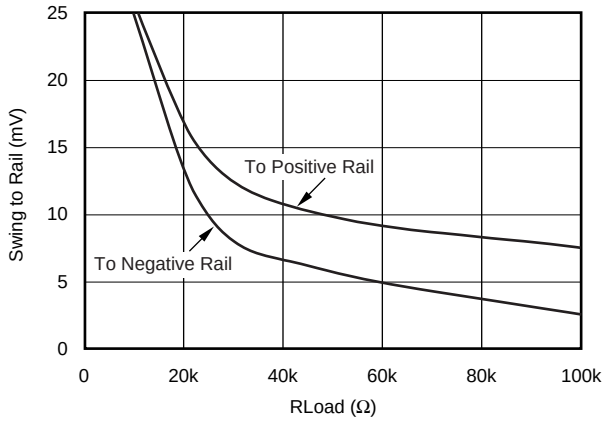

0.1Hz TO 10Hz VOLTAGE NOISE



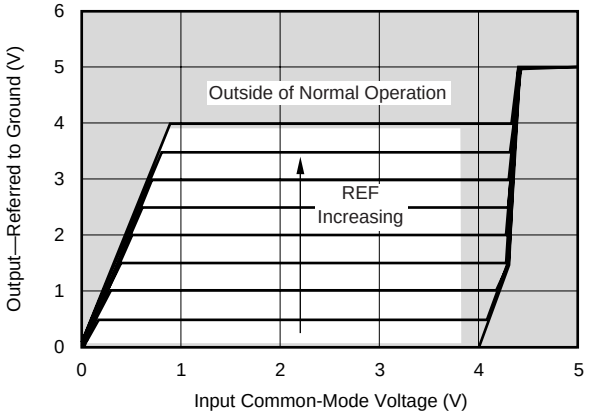
# TYPICAL CHARACTERISTICS (Cont.)

At $T_A$ = +25°C, $V_S$ = 5V, $V_{CM}$ = 1/2$V_S$, $R_L$ = 25kΩ, $C_L$ = 50pF, unless otherwise noted.

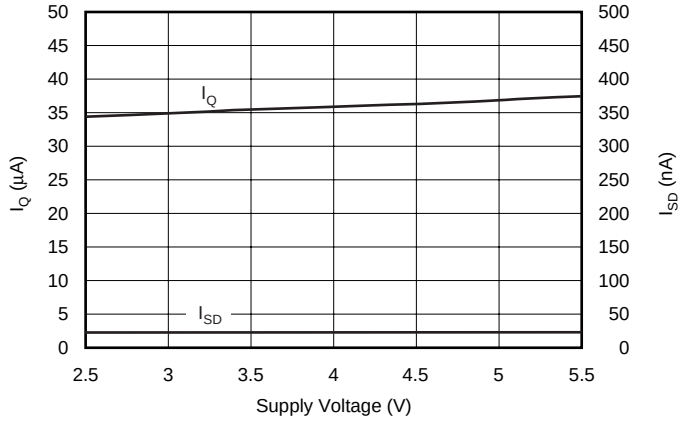
OUTPUT SWING vs LOAD RESISTANCE



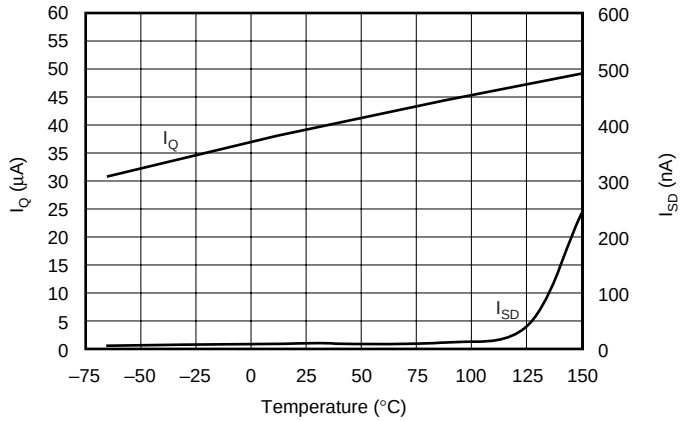

COMMON-MODE INPUT RANGE vs REFERENCE VOLTAGE



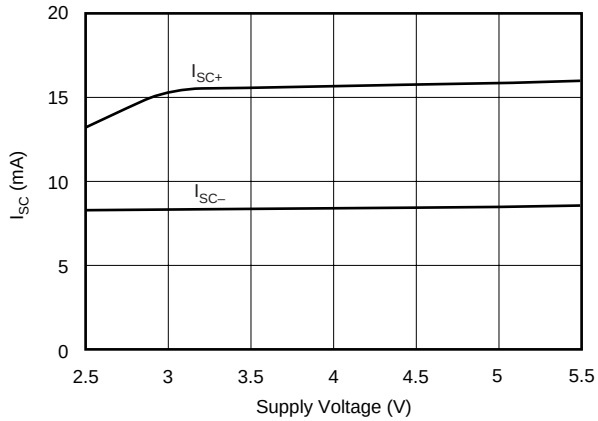

QUIESCENT CURRENT AND SHUTDOWN CURRENT vs POWER SUPPLY



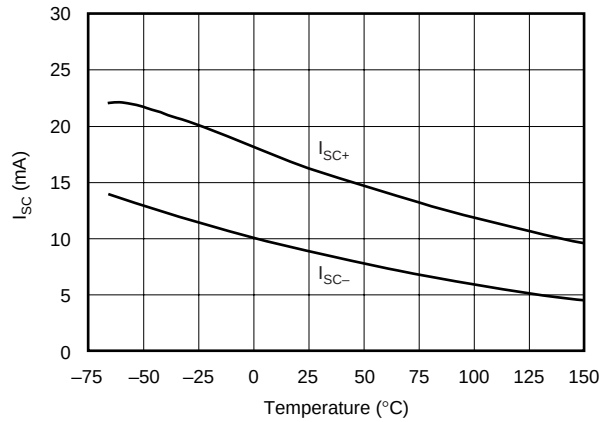

QUIESCENT CURRENT AND SHUTDOWN CURRENT vs TEMPERATURE




SHORT-CIRCUIT CURRENT vs POWER SUPPLY



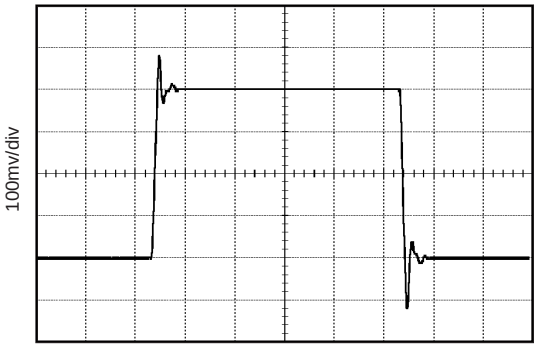

SHORT-CIRCUIT CURRENT vs TEMPERATURE



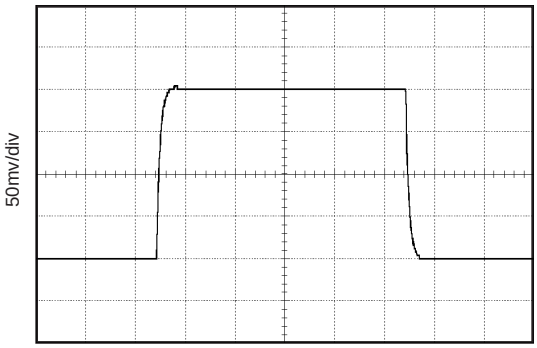
# TYPICAL CHARACTERISTICS (Cont.)

At $T_A$ = +25°C, $V_S$ = 5V, $V_{CM}$ = 1/2$V_S$, $R_L$ = 25kΩ, $C_L$ = 50pF, unless otherwise noted.

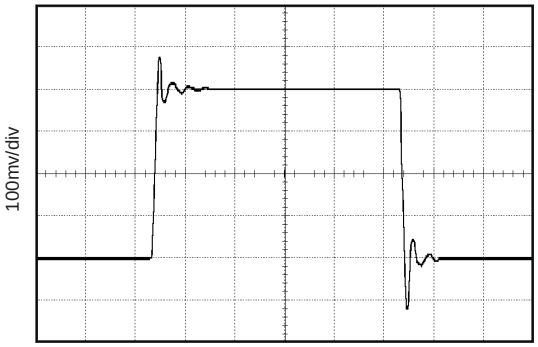
SMALL-SIGNAL STEP RESPONSE (G = 5)



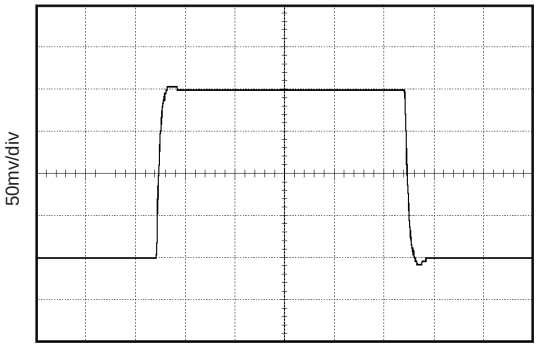

SMALL-SIGNAL STEP RESPONSE (G = 100)



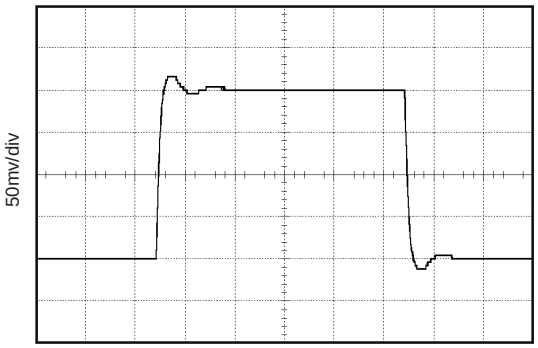

SMALL-SIGNAL STEP RESPONSE
(G = 5, $C_L$ = 1000pF)



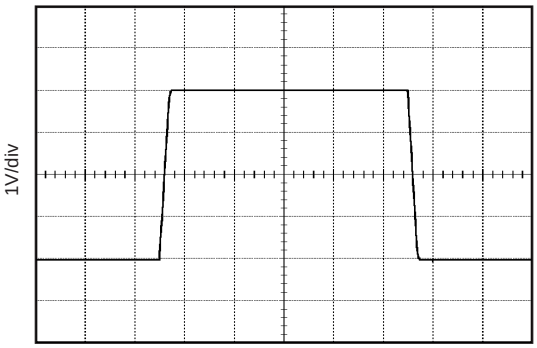

SMALL-SIGNAL STEP RESPONSE
(G = 100, $C_L$ = 1000pF)




SMALL-SIGNAL STEP RESPONSE
(G = 100, $C_L$ = 5000pF)



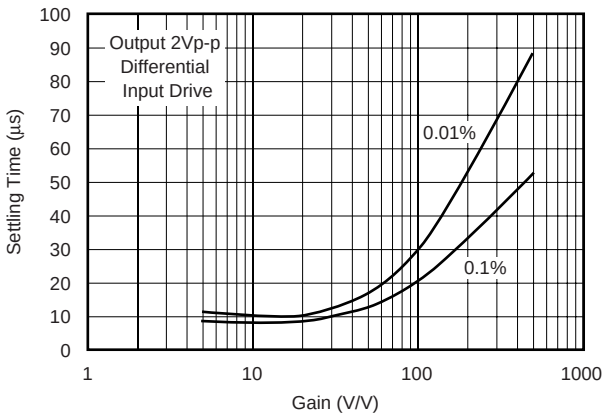

LARGE-SIGNAL STEP RESPONSE
(G = 25, $C_L$ = 50pF)



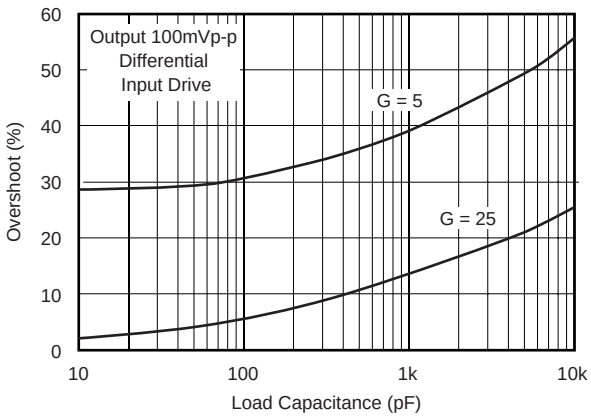
# TYPICAL CHARACTERISTICS (Cont.)

At $T_A$ = +25°C, $V_S$ = 5V, $V_{CM}$ = 1/2$V_S$, $R_L$ = 25kΩ, $C_L$ = 50pF, unless otherwise noted.

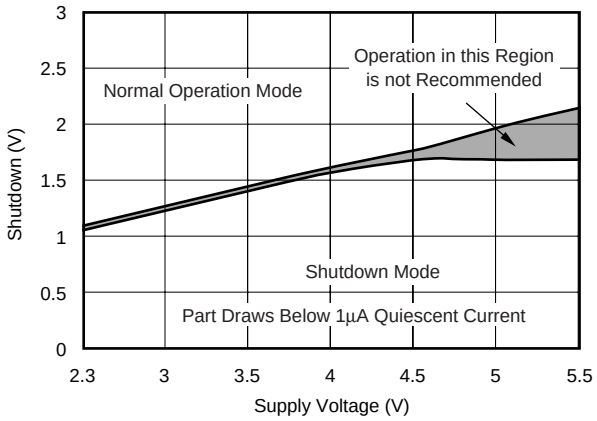
SETTLING TIME vs GAIN



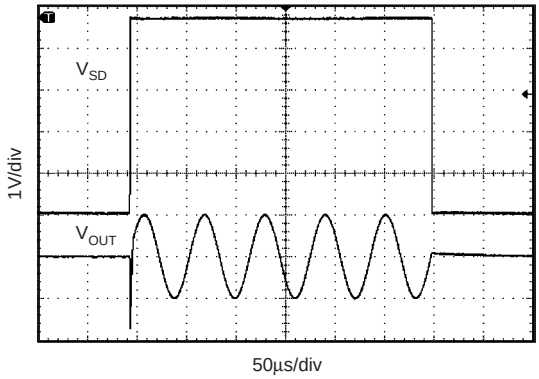

PERCENT OVERSHOOT vs LOAD CAPACITANCE



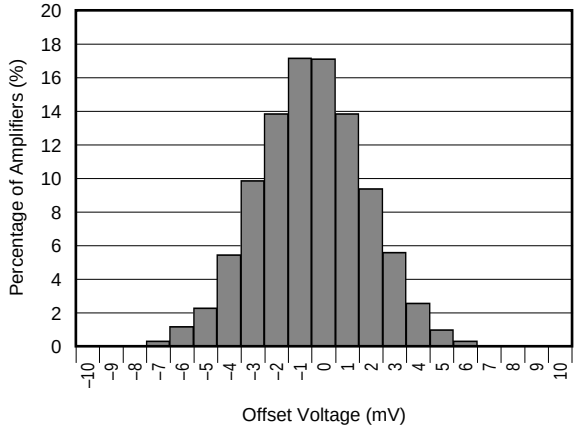

SHUTDOWN VOLTAGE vs SUPPLY VOLTAGE



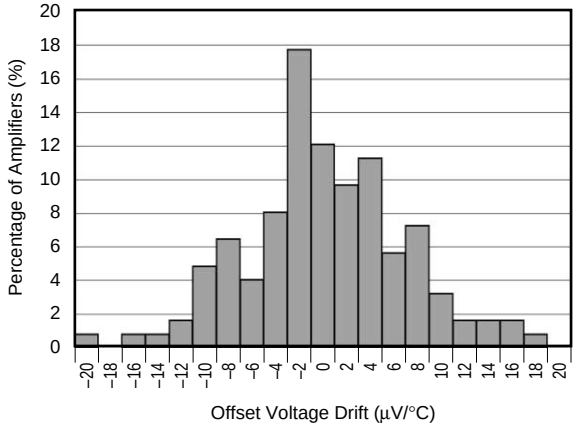

SHUTDOWN TRANSIENT BEHAVIOR




OFFSET VOLTAGE PRODUCTION DISTRIBUTION



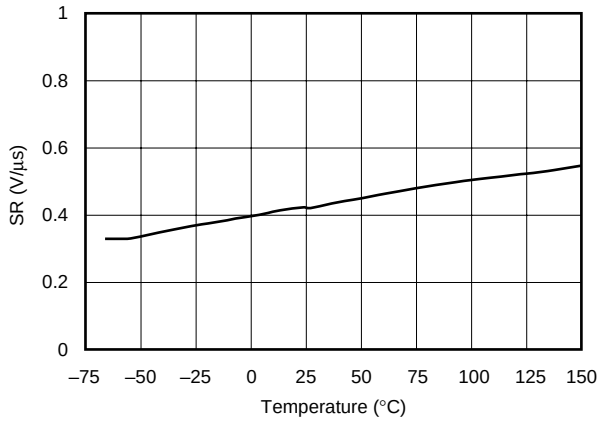

OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



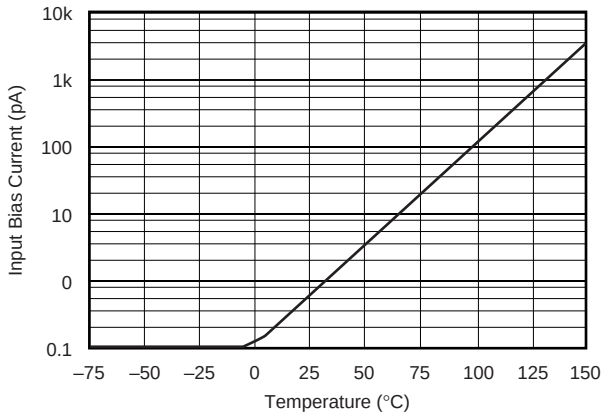
# TYPICAL CHARACTERISTICS (Cont.)

At $T_A$ = +25°C, $V_S$ = 5V, $V_{CM}$ = 1/2$V_S$, $R_L$ = 25kΩ, $C_L$ = 50pF, unless otherwise noted.

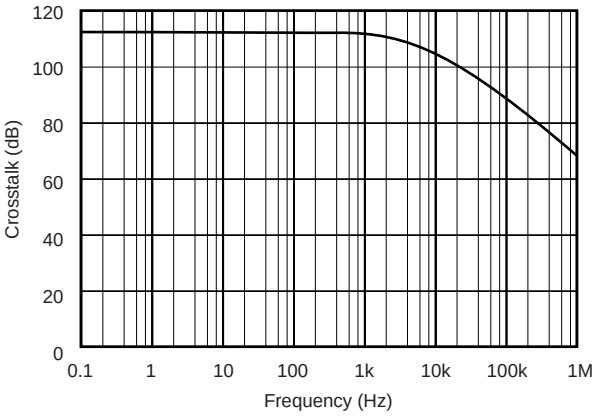
SLEW RATE vs TEMPERATURE



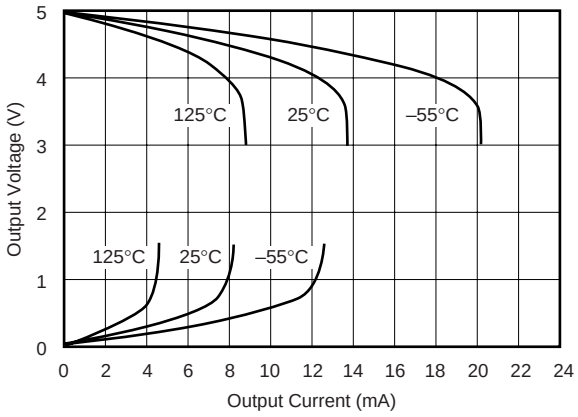

INPUT BIAS CURRENT vs TEMPERATURE




CROSSTALK vs FREQUENCY




OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



# APPLICATIONS INFORMATION

The INA322 is a modified version of the classic "two op amp" instrumentation amplifier, with an additional gain amplifier.

Figure 1 shows the basic connections for the operation of the INA322 and INA2322. The power supply should be capacitively decoupled with 0.1µF capacitors as close to the INA322 as possible for noisy or high-impedance applications.

The output is referred to the reference terminal, which must be at least 1.2V below the positive supply rail.

## OPERATING VOLTAGE

The INA322 family is fully specified over a supply range of +2.7V to +5.5V, with key parameters specified over the temperature range of -55°C to +125°C. Parameters that vary significantly with operating conditions, such as load conditions or temperature, are shown in the Typical Characteristic Curves.

The INA322 may be operated on a single supply. Figure 2 shows a bridge amplifier circuit operated from a single +5V supply. The bridge provides a small differential voltage riding on an input common-mode voltage.

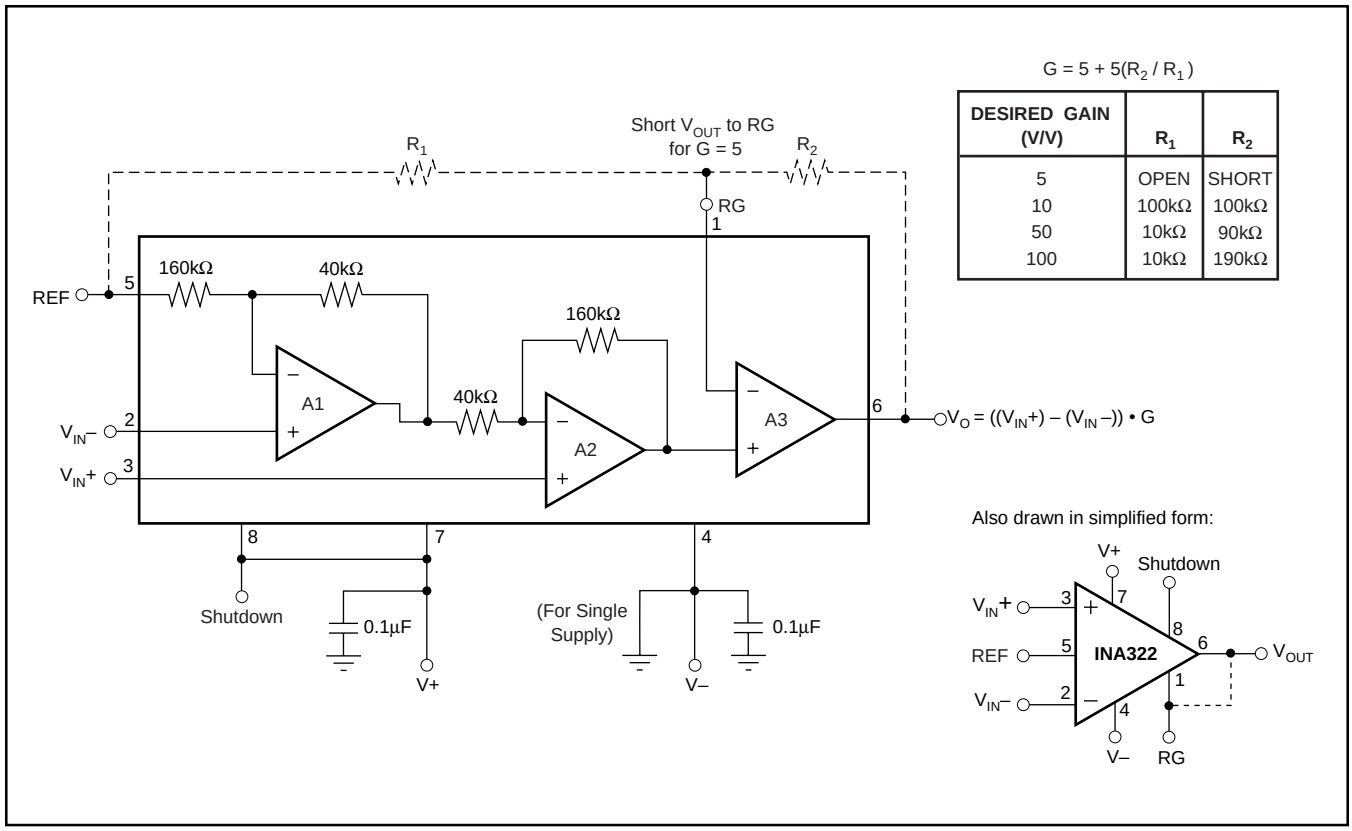



FIGURE 1. Basic Connections.

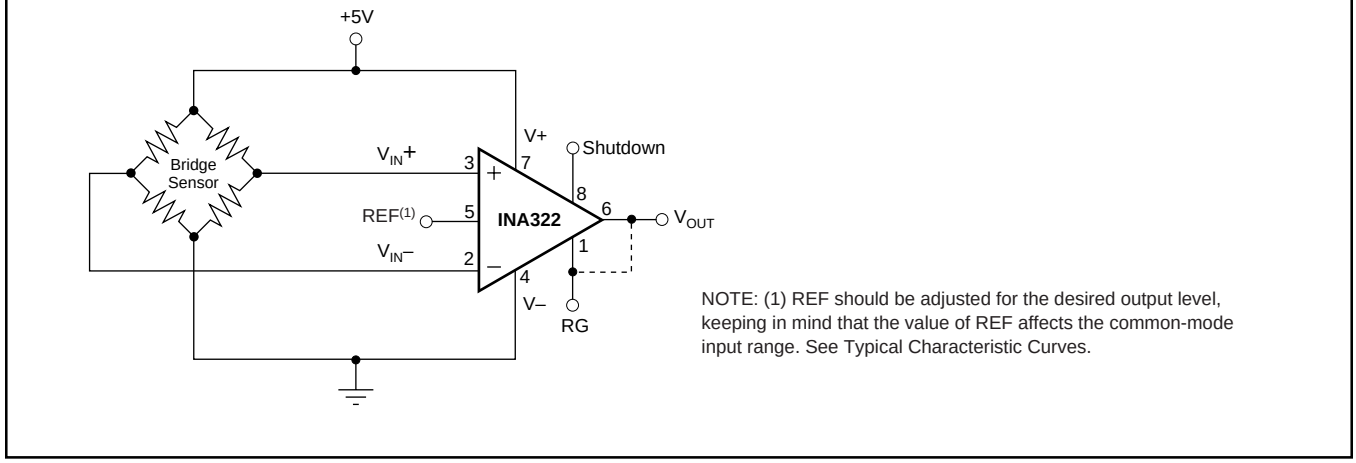



FIGURE 2. Bridge Amplifier of the INA322.

## SETTING THE GAIN

The ratio of $R_2$ to $R_1$, or the impedance between pins 1, 5, and 6, determines the gain of the INA322. With an internally set gain of 5, the INA322 can be programmed for gains greater than 5 according to the following equation:

$$G = 5 + 5(R_2/R_1)$$

The INA322 is designed to provide accurate gain, with gain error specified to be less than 0.4%. Setting gain with matching TC resistors will minimize gain drift. Errors from external resistors will add directly to the error, and may become dominant error sources.

## INPUT COMMON-MODE RANGE

The upper limit of the common mode input range is set by the common-mode input range of the second amplifier, A2, to 1.2V below positive supply. Under most conditions, the amplifier operates beyond this point with reduced performance. The lower limit of the input range is bounded by the output swing of amplifier A1, and is a function of the reference voltage according to the following equation:

$$V_{OA1} = 5/4\, V_{CM} - 1/4\, V_{REF}$$

(See Typical Characteristic Curves for Input Common-Mode Range vs Reference Voltage).

## REFERENCE

The reference terminal defines the zero output voltage level. In setting the reference voltage, the common mode input of A3 should be considered according to the following equation:

$$V_{OA2} = V_{REF} + 5(V_{IN}+ - V_{IN}-)$$

$V_{OA2}$ should be less than $V_{DD} - 1.2V$.

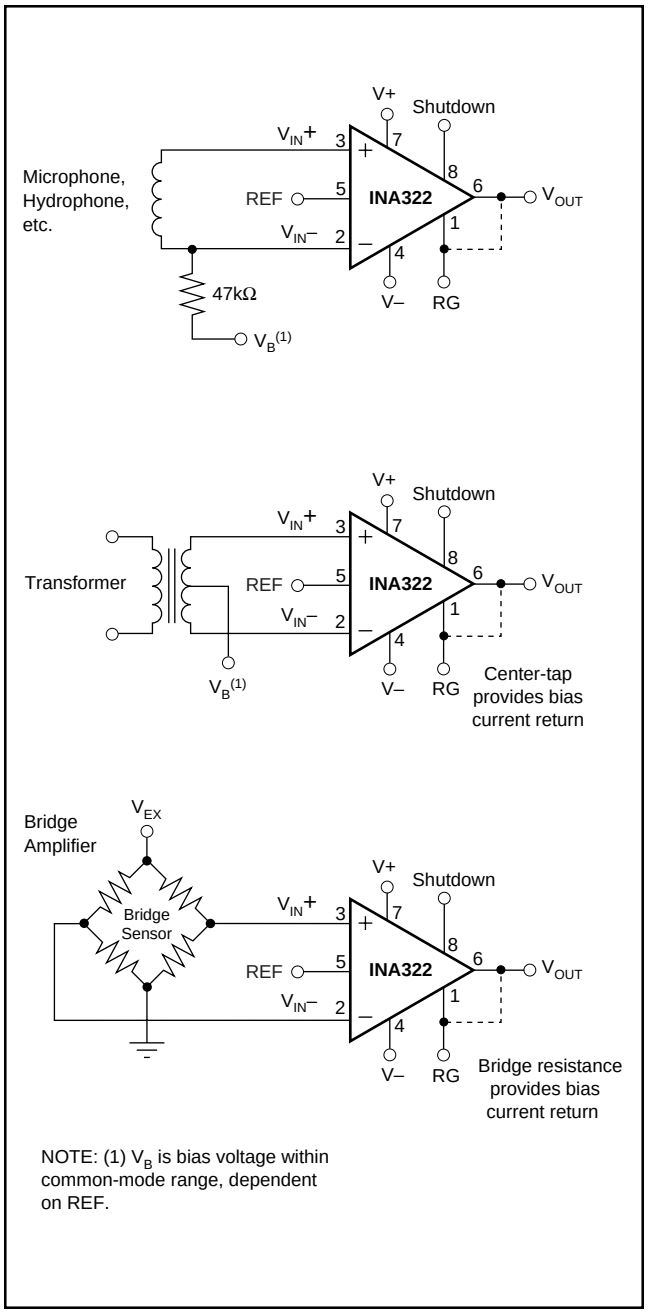
The reference pin requires a low-impedance connection. Any resistance in series with the reference pin will degrade the CMRR. The reference pin may be used to compensate for the offset voltage (see Offset Trimming section). The reference voltage level also influences the common-mode input range (see Common-Mode Input Range section).

## INPUT BIAS CURRENT RETURN

With a high input impedance of $10^{13}\Omega$, the INA322 is ideal for use with high-impedance sources. The input bias current of less than 10pA makes the INA322 nearly independent of input impedance and ideal for low-power applications.

For proper operation, a path must be provided for input bias currents for both inputs. Without input bias current paths, the inputs will "float" to a potential that exceeds common-mode range and the input amplifier will saturate. Figure 3 shows how bias current path can be provided in the cases of microphone applications, thermistor applications, ground returns, and dc-coupled resistive bridge applications.

When differential source impedance is low, the bias current return path can be connected to one input. With higher source impedance, two equal resistors will provide a balanced input. The advantages are lower input offset voltage due to bias current flowing through the source impedance and better high-frequency gain.




NOTE: (1) $V_B$ is bias voltage within common-mode range, dependent on REF.

FIGURE 3. Providing an Input Common-Mode Path.

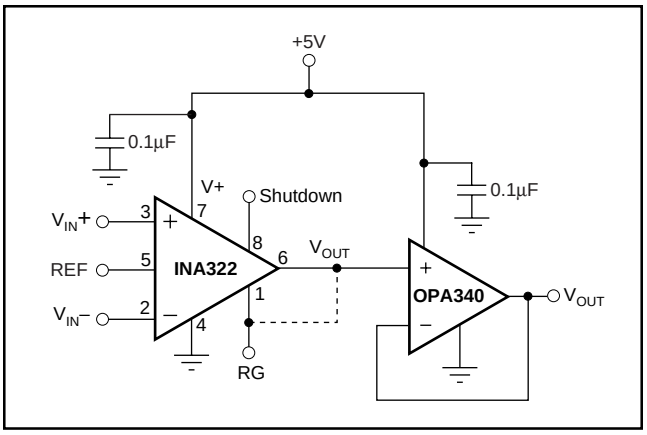



FIGURE 4. Output Buffering Circuit. Able to drive loads as low as 600Ω.

## SHUTDOWN MODE

The shutdown pin of the INA322 is nominally connected to V+. When the pin is pulled below 0.8V on a 5V supply, the INA322 goes into sleep mode within nanoseconds. For actual shutdown threshold, see typical characteristic curve "Shutdown Voltage vs Supply Voltage". Drawing less than 1µA of current, and returning from sleep mode in microseconds, the shutdown feature is useful for portable applications. Once in 'sleep-mode' the amplifier has high output impedance, making the INA322 suitable for multiplexing.

## RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output for gains of 10 or greater. When the amplifier is in G = 5 the output will not swing to positive rail. For resistive loads greater than 25kΩ, the output voltage can swing to within a few millivolts of the supply rail while maintaining low gain error. For heavier loads and over temperature, see the typical characteristic curve "Output Voltage Swing vs Output Current." The INA322's low output impedance at high frequencies makes it suitable for directly driving Capacitive Digital-to-Analog (CDAC) input A/D converters, as shown in Figure 5.

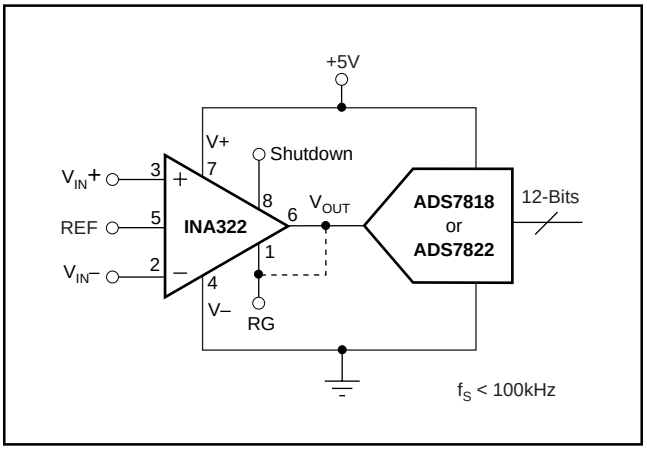



FIGURE 5. INA322 Directly Drives a Capacitive-Input, A/D Converter.

## OUTPUT BUFFERING

The INA322 is optimized for a load impedance of 10kΩ or greater. For higher output current the INA322 can be buffered using the OPA340, as shown in Figure 4. The OPA340 can swing within 50mV of the supply rail, driving a 600Ω load. The OPA340 is available in the tiny MSOP-8 package.

## OFFSET TRIMMING

In the event that external offset adjustment is required, the offset can be adjusted by applying a correction voltage to the reference terminal. Figure 6 shows an optional circuit for trimming offset voltage. The voltage applied to the REF terminal is added to the output signal. The gain from REF to $V_{OUT}$ is +1. An op-amp buffer is used to provide low impedance at the REF terminal to preserve good common-mode rejection.

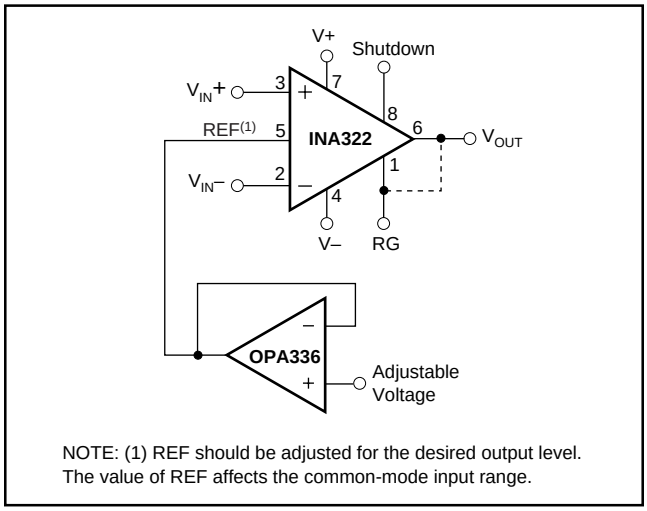



FIGURE 6. Optional Offset Trimming Voltage.

## INPUT PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than 500mV. Momentary voltages greater than 500mV beyond the power supply can be tolerated if the current through the input pins is limited to 10mA. This is easily accomplished with input resistor $R_{LIM}$, as shown in Figure 7. Many input signals are inherently current-limited to less than 10mA, therefore, a limiting resistor is not required.

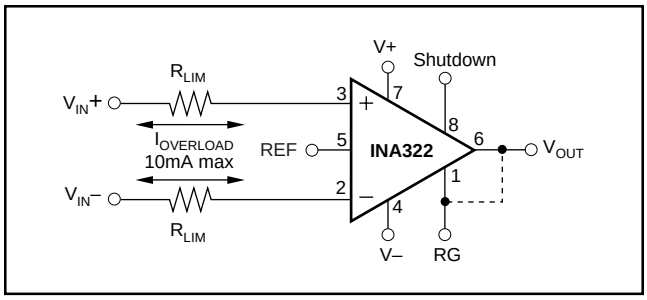



FIGURE 7. Input Protection.

## OFFSET VOLTAGE ERROR CALCULATION

The offset voltage ($V_{OS}$) of the INA322EA has a specified maximum of 10mV with a +5V power supply and the common-mode voltage at $V_S/2$. Additional specifications for power-supply rejection and common-mode rejection are provided to allow the user to easily calculate worst-case expected offset under the conditions of a given application.

Power Supply Rejection Ratio (PSRR) is specified in µV/V. For the INA322, worst case PSRR is 250µV/V, which means for each volt of change in power supply, the offset may shift up to 250µV. Common-Mode Rejection Ratio (CMRR) is specified in dB, which can be converted to µV/V using the following equation:

$$\text{CMRR (in } \mu\text{V/V)} = 10^{[(\text{CMRR in dB})/-20]} \bullet 10^6$$

For the INA322, the worst case CMRR over the specified common-mode range is 60dB (at G = 25) or about 1mV/V This means that for every volt of change in common-mode, the offset will shift less than 1mV.

These numbers can be used to calculate excursions from the specified offset voltage under different application conditions. For example, an application might configure the amplifier with a 3.3V supply with 1V common-mode. This configuration varies from the specified configuration, representing a 1.7V variation in power supply (5V in the offset specification versus 3.3V in the application) and a 0.65V variation in common-mode voltage from the specified $V_S/2$.

Calculation of the worst-case expected offset would be as follows:

Adjusted $V_{OS}$ = Maximum specified $V_{OS}$ +
(power-supply variation) • PSRR +
(common-mode variation) • CMRR

$V_{OS}$ = 10mV + (1.7V • 0.250mV/V) + (0.65V • 1mV/V)
= ±11.075mV

However, the typical value will be closer to 2.2mV (calculated using the typical values).

## FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, $R_F$, as shown in Figure 8. This capacitor compensates for the zero created by the feedback network impedance and the INA322's RG-pin input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks. Also, $R_X$ and $C_L$ can be added to reduce high-frequency noise.

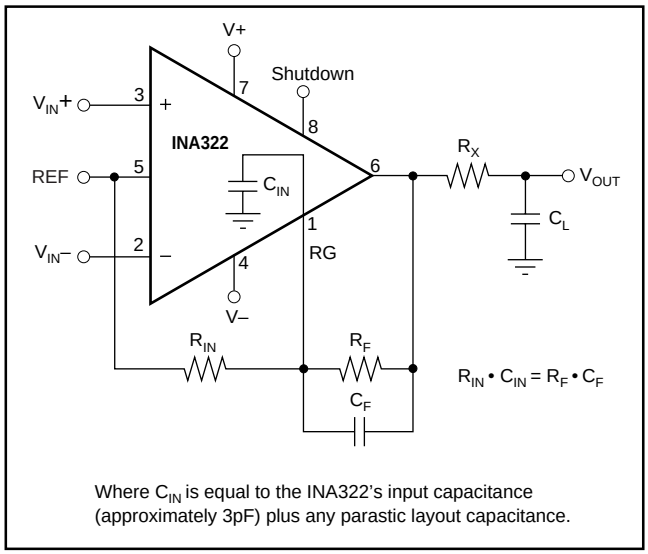



FIGURE 8. Feedback Capacitor Improves Dynamic Performance.

It is suggested that a variable capacitor be used for the feedback capacitor since input capacitance may vary between instrumentation amplifiers, and layout capacitance is difficult to determine. For the circuit shown in Figure 8, the value of the variable feedback capacitor should be chosen by the following equation:

$$R_{IN} \bullet C_{IN} = R_F \bullet C_F$$

Where $C_{IN}$ is equal to the INA322's RG-pin input capacitance (typically 3pF) plus the layout capacitance. The capacitor can be varied until optimum performance is obtained.

## APPLICATION CIRCUITS

### Medical ECG Applications

Figure 9 shows the INA322 configured to serve as a low-cost ECG amplifier, suitable for moderate accuracy heart-rate applications such as fitness equipment. The input signals are obtained from the left and right arms of the patient. The common-mode voltage is set by two 2MΩ resistors. This potential through a buffer, provides optional right leg drive. Filtering can be modified to suit application needs by changing the capacitor value of the output filter.

### Low-Power, Single-Supply Data Acquisition Systems

Refer to Figure 5 to see the INA322 configured to drive an ADS7818. Functioning at frequencies of up to 500kHz, the INA322 is ideal for low-power data acquisition.

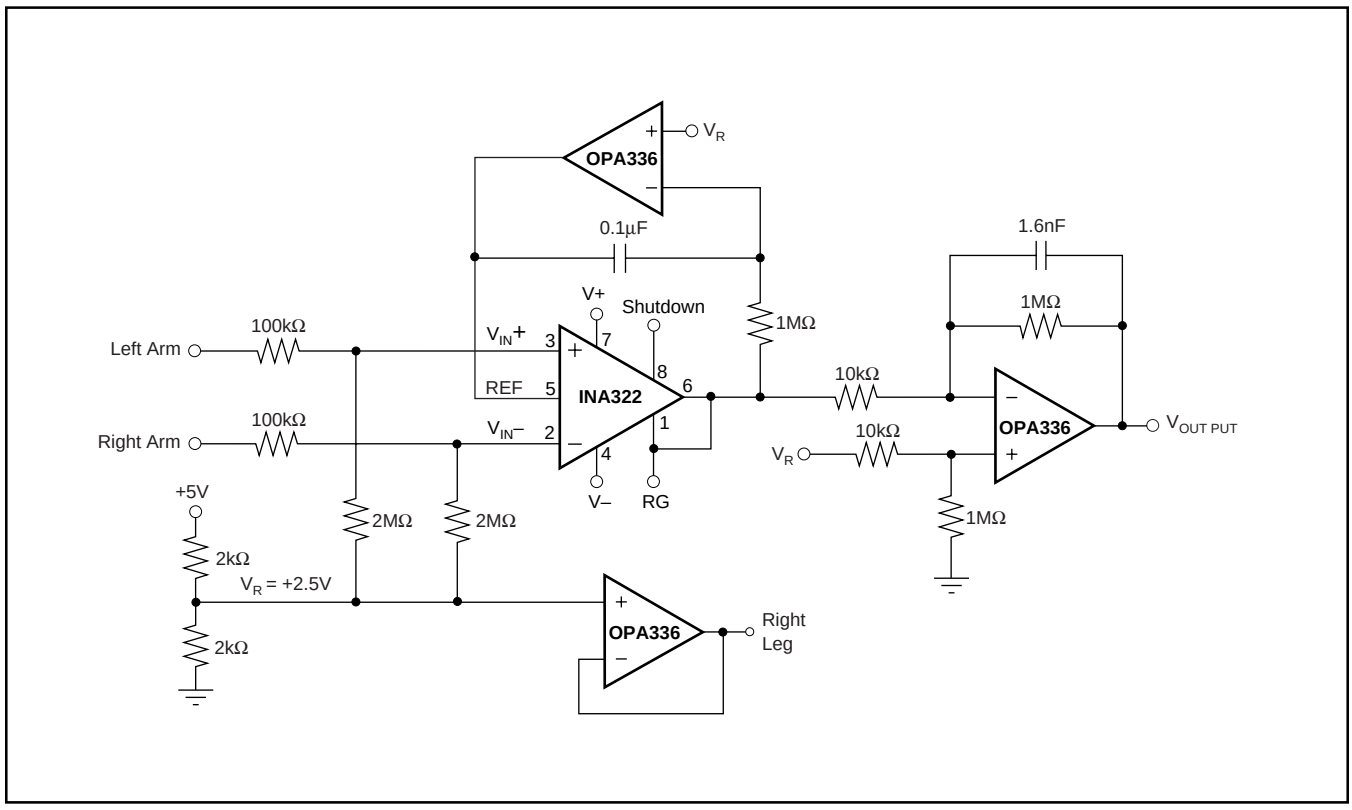



FIGURE 9. Simplified ECG Circuit for Medical Applications.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| INA2322EA/250 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | INA 2322EA | Samples |
| INA2322EA/250G4 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | INA 2322EA | Samples |
| INA322EA/250 | ACTIVE | VSSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -55 to 125 | C22 | Samples |
| INA322EA/250G4 | ACTIVE | VSSOP | DGK | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -55 to 125 | C22 | Samples |
| INA322EA/2K5 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -55 to 125 | C22 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

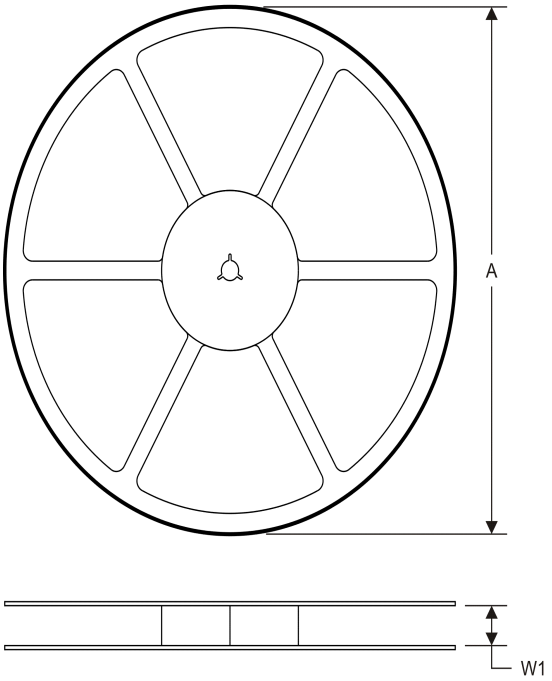
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

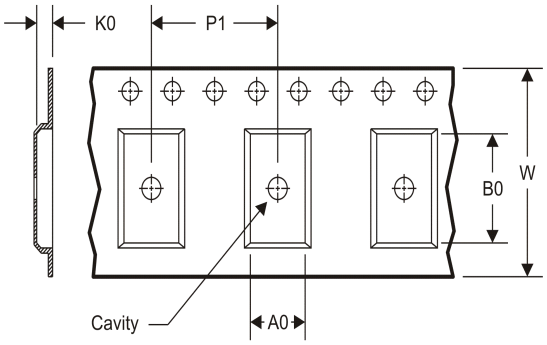
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



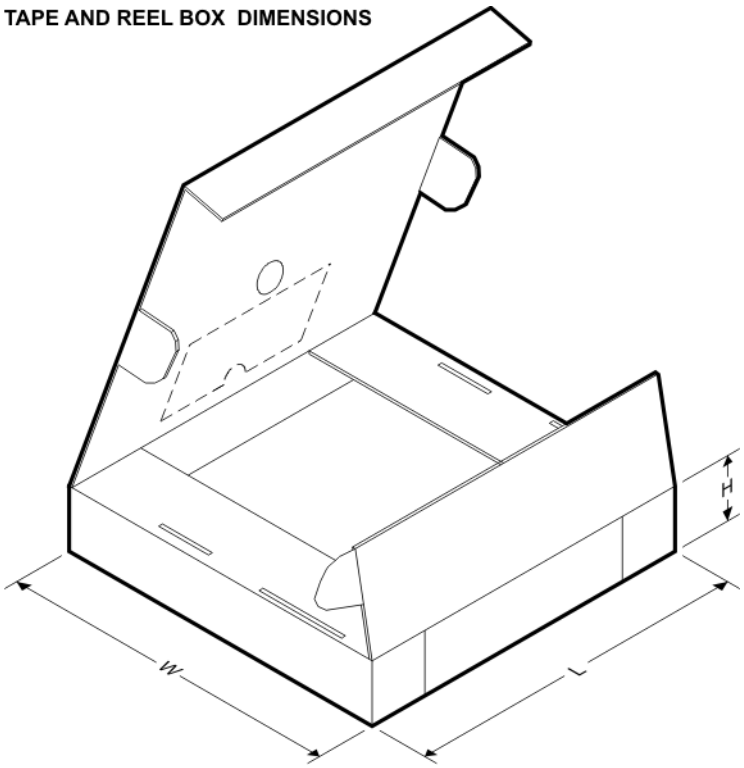

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INA2322EA/250 | TSSOP | PW | 14 | 250 | 180.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| INA322EA/250 | VSSOP | DGK | 8 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| INA322EA/2K5 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

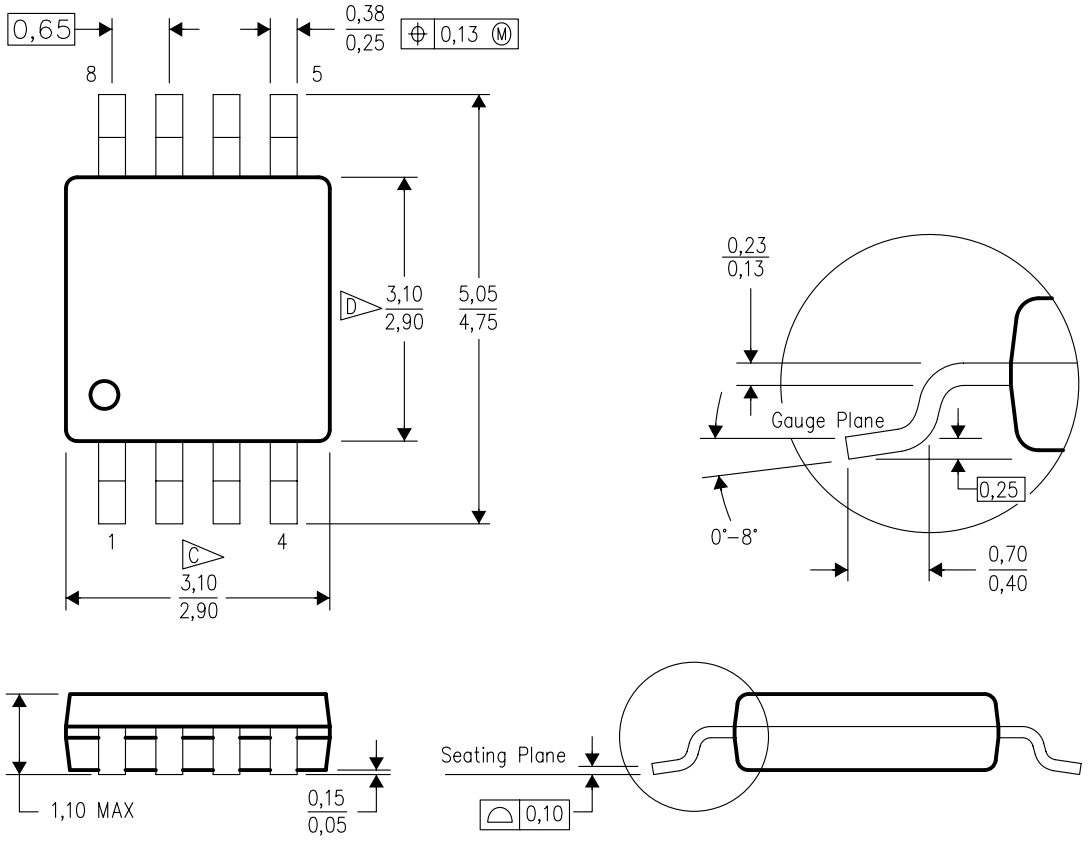
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| INA2322EA/250 | TSSOP | PW | 14 | 250 | 210.0 | 185.0 | 35.0 |
| INA322EA/250 | VSSOP | DGK | 8 | 250 | 210.0 | 185.0 | 35.0 |
| INA322EA/2K5 | VSSOP | DGK | 8 | 2500 | 367.0 | 367.0 | 35.0 |

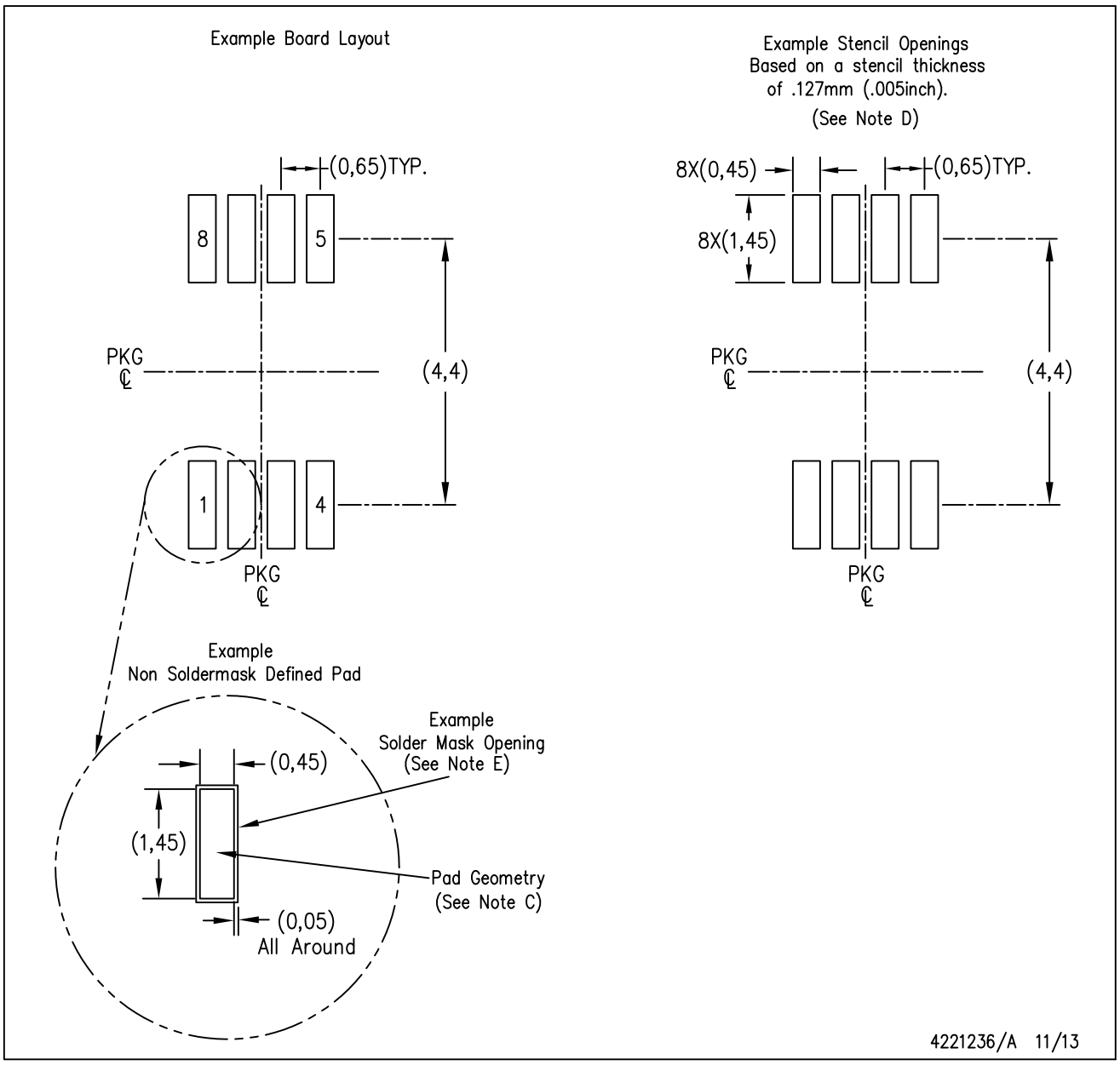
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

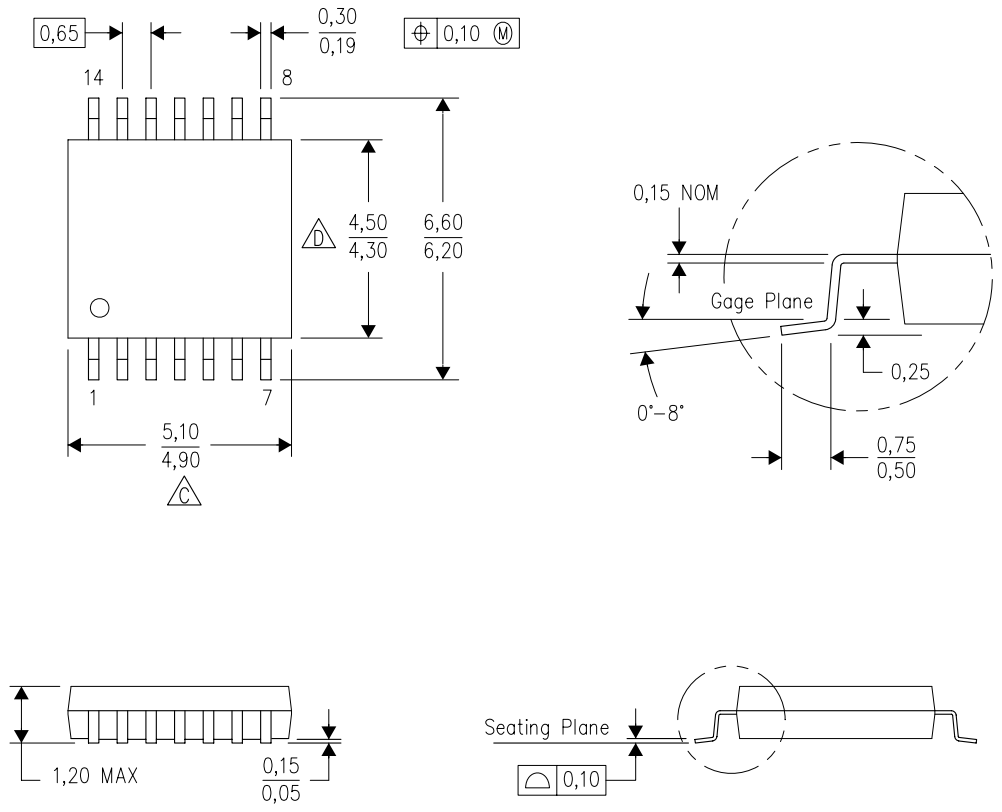
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
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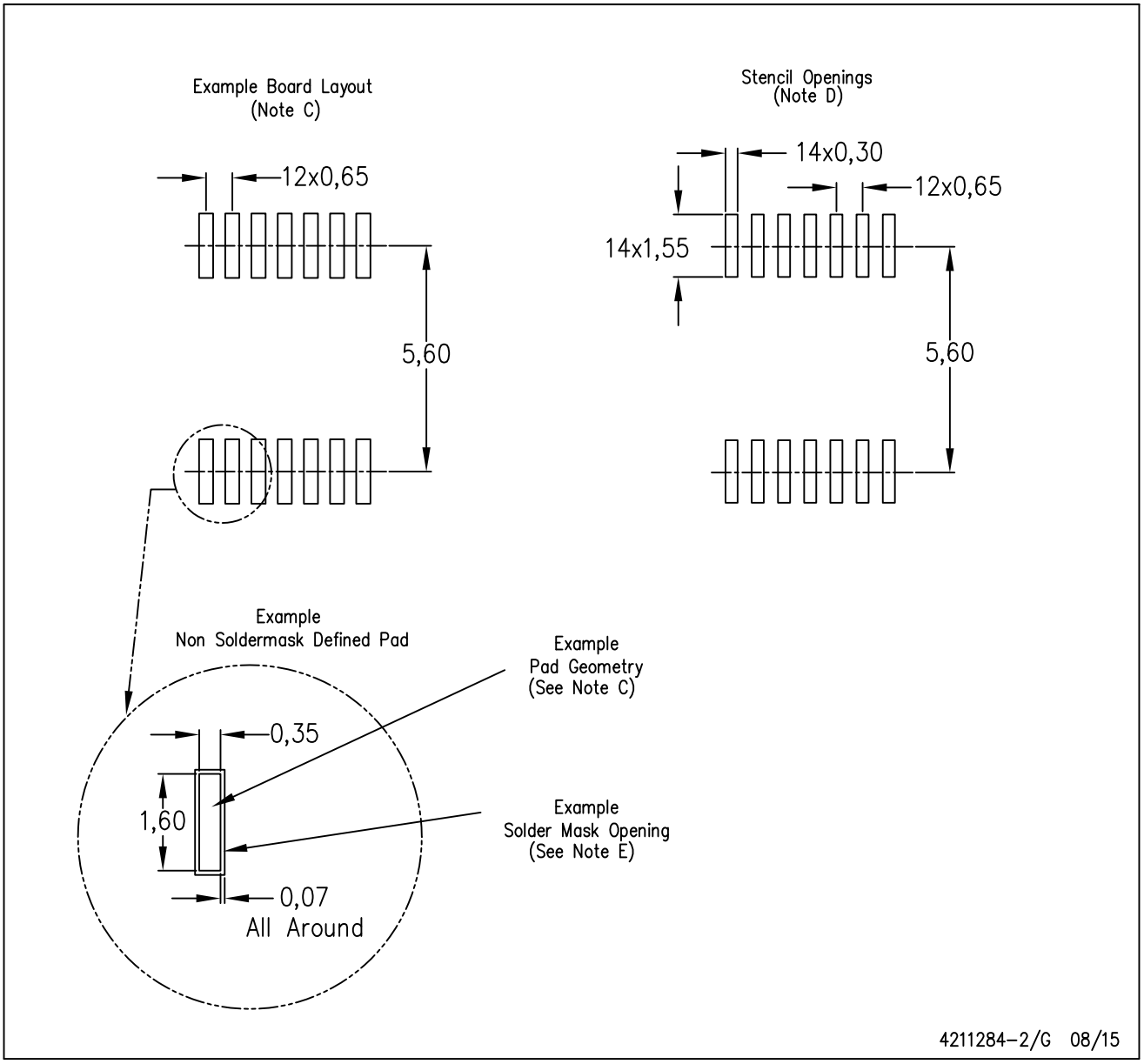
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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