DRV8307 Brushless DC Motor Controller

1 Features

- Three-Phase Brushless DC Motor Controller
  - PWM Input for Speed Control
- Operating Supply Voltage 8.5 to 32 V
- 30-mA Gate-Drive Current to 6 N-Channel MOSFETs
- Integrated Current Sense Amplifier
- 5-V Regulator for Hall Sensors
- Low-Power Standby Mode
- Locked Rotor Detection and Restart
- Integrated Overcurrent and Overtemperature Protection
- 6- × 6-mm VQFN Package, 0.5-mm Pitch

2 Applications

- Industrial Pumps and Fans
- White Goods
- Robotic Appliances

3 Description

The DRV8307 is a three half-bridge pre-driver that drives six N-type MOSFETs 30 mA with a single power supply. Aimed at sensored three-phase brushless DC motors, the DRV8307 is driven by a single PWM input and supports integrated commutation logic with three Hall sensor inputs. A separate 5-V regulator is also included to be used to power Hall-effect sensors and other external components.

The DRV8307 includes a current sense input for current limiting and protection. The current limit can be set by adjusting the value of the R_{ISENSE} sense resistor.

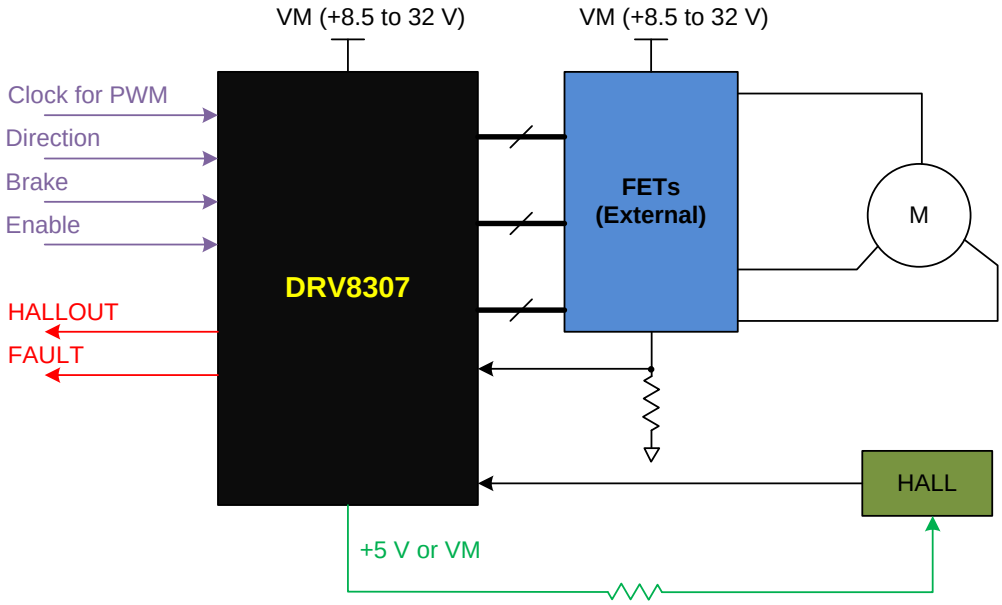
Motor operation (start and stop) is controlled through the ENABLEn terminal. If the ENABLEn terminal is set high and motor rotation has stopped, the device enters into a low-power standby state, thereby conserving overall system power during periods of inactivity.

Protection features are also included in the DRV8307 device such as locked rotor detection, as well as overcurrent and overtemperature protection and undervoltage lockout to bolster overall system robustness and reliability.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
DRV8307RHA	VQFN (40)	6 mm × 6 mm

4 Simplified Schematic



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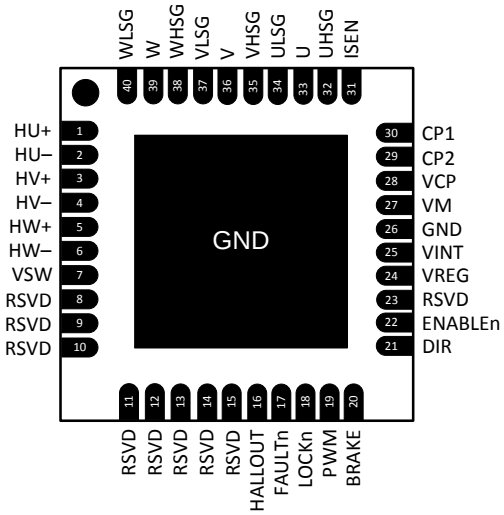
5 Revision History

Date	Revision	Notes
April 2014	*	Initial Release

6 Terminal Configurations and Functions

40-TERMINAL VQFN PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL		I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NUMBER			
POWER AND GROUND				
CP1	30	I/O	Charge pump flying capacitor	Connect a 0.1-µF 35-V capacitor between CP1 and CP2
CP2	29	I/O		
GND	26, PPAD	I	Ground reference. Terminal 26 and the Power Pad are internally connected.	Connect to board GND
VCP	28	I/O	Charge pump storage capacitor	Connect a 1-µF 35-V ceramic capacitor to VM
VINT	25	I/O	Internal 1.8-V core voltage regulator bypass	Bypass to GND with a 1-µF 6.3-V ceramic capacitor
VM	27	I	Motor supply voltage	Connect to motor supply voltage. Bypass to GND with a 0.1-µF ceramic capacitor, plus a large electrolytic capacitor (47 µF or larger is recommended), with a voltage rating of 1.5× to 2.5× VM.
VREG	24	O	5-V regulator output. Active when ENABLEn is active.	Bypass to GND with a 0.1-µF 10-V ceramic capacitor. Can provide 5-V power to Hall sensors.
VSW	7	O	Switched VM power output. When ENABLEn is active, VM is applied to this terminal.	Can be used for powering Hall elements, along with added series resistance.
CONTROL				
BRAKE	20	I	Causes motor to brake. Polarity is programmable. Internal pulldown resistor.	
PWM	19	I	The clock input, used in clock frequency mode and clock PWM mode. Internal pulldown resistor.	
DIR	21	I	Sets motor rotation direction. Internal pulldown resistor.	
ENABLEn	22	I	Enables and disables the motor – active low. Internal pulldown resistor.	
FAULTn	17	OD	Fault indicator – active low when overcurrent, overtemperature, or rotor stall detected. Open-drain output.	
HALLOUT	16	OD	Outputs a TACH signal generated from the Hall U sensor. Open-drain output.	

(1) I = input, O = output, OD = open-drain output, I/O = input/output

Terminal Functions (continued)

TERMINAL		I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NUMBER			
LOCKn	18	OD	Outputs a signal that indicates the speed loop is locked. Open-drain output.	
RSVD	23		Reserved	Can be floating or connected to ground.
RSVD	11			
RSVD	12			
RSVD	14			
RSVD	15			
RSVD	13			
POWER STAGE INTERFACE				
ISEN	31	I	Low-side current sense resistor	Connect to low-side current sense resistor
U	33	I	Measures motor phase voltages for V_{FETOCP}	Connect to motor windings
V	36	I		
W	39	I		
UHSG	32	O	High-side FET gate outputs	Connect to high-side ½ H-bridge N-channel FET gate
VHSG	35	O		
WHSG	38	O		
ULSG	34	O	Low-side FET gate outputs	Connect to low-side ½ H-bridge N-channel FET gate
VLSG	37	O		
WLSG	40	O		
RSVD	8		Reserved	Do not connect. Leave floating.
RSVD	9			
RSVD	10			
HU+	1	I	Hall sensor U positive input	Connect to Hall sensors. Noise filter capacitors may be desirable, connected between the + and – Hall inputs.
HU–	2	I	Hall sensor U negative input	
HV+	3	I	Hall sensor V positive input	
HV–	4	I	Hall sensor V negative input	
HW+	5	I	Hall sensor W positive input	
HW–	6	I	Hall sensor W negative input	

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)(2)(3)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	35	V
Charge pump and high-side gate drivers (VCP, UHSG, VHSG, WHSG)	–0.3	50	V
Output terminal, low side gate drivers, charge pump flying cap and switched VM power supply voltage (U, V, W, ULSG, VLSG, WLSG, CP1, CP2 VSW)	–0.6	40	V
Internal core voltage regulator (VINT)	–0.3	2.0	V
Linear voltage regulator output (VREG)	–0.3	5.5	V
Sense current terminal (ISEN)	–0.3	2.0	V
Digital terminal voltage (FAULTn, LOCKn, PWM, BRAKE, DIR, ENABLEn, HALLOUT)	–0.5	5.75	V
Hall sensor input terminal voltage (HU+, HU–, HV+, HV–, HW+, HW–)	0	VREG	V
Continuous total power dissipation	See Thermal Information		
Operating junction temperature range, T_J	–40	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed

7.2 Handling Ratings

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{stg}	Storage temperature range	–60	150	°C

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range, ENABLEn = 0, motor operating (1)	8.5		32	V
V_{MDIS}	Motor power supply voltage range, ENABLEn = 1, motor not operating	4.5		35	
I_{VREG}	VREG output current(2)	0		30	mA
I_{VSW}	VSW output current(2)	0		30	
f_{HALL}	Hall sensor input frequency(3)	0		30	kHz
f_{PWM}	Frequency on PWM	16		50 (4)	kHz

(1) Note that at VM < 12 V, gate drive output voltage tracks VM voltage
(2) Power dissipation and thermal limits must be observed
(3) f_{HALL} of 50 Hz to 6.7 kHz is best
(4) Operational with frequencies above 50 kHz, but resolution is degraded

7.4 Thermal Information

THERMAL METRIC[1]		DRV8307 RHA (40 TERMINALS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	33.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[3]	23.0	
$R_{\theta JB}$	Junction-to-board thermal resistance[4]	8.8	
ψ_{JT}	Junction-to-top characterization parameter[5]	0.3	
ψ_{JB}	Junction-to-board characterization parameter[6]	8.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance[7]	2.3	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VM SUPPLY						
I_{VM}	VM active current	ENABLEn = 0, VREG and VSW open		12	18	mA
I_{STBY}	VM standby current	ENABLEn = 1			120	µA
V_{RESET}	VM logic reset voltage	VM falling			4.6	V
		VM rising	5.0			
VREG SUPPLY						
V_{VREG}	Output voltage	I_{OUT} = 1 to 30 mA	4.75	5	5.25	V
I_{VREG}	Output current				30	mA
VSW SUPPLY						
$R_{DS(ON)}$	VSW switch on-resistance	I_{OUT} = 1 to 30 mA		9	20	Ω
I_{VSW}	Output current				30	mA
INTERNAL CLOCK OSCILLATOR						
f_{CLK50}	Internal CLK50 clock frequency			50		MHz
LOGIC-LEVEL INPUTS AND OUTPUTS						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		1.5		5.5	V
I_{IL}	Low-level input current		–50		50	µA
I_{IH}	High-level input current	V_{IN} = 3.3 V, DIR, BRAKE, PWM	20		100	µA
		V_{IN} = 3.3 V, ENABLEn	6		9	
V_{HYS}	Input hysteresis voltage		0.1	0.3	0.5	V
R_{PD}	Input pulldown resistance	DIR, BRAKE, PWM	50	100	150	kΩ
		ENABLEn	350		550	
OPEN DRAIN OUTPUTS						
V_{OL}	Low-level output voltage	I_{OUT} = 2.0 mA			0.5	V
I_{OH}	Output leakage current	V_{OUT} = 3.3 V			1	µA
HALL SENSOR INPUTS						
V_{HYS}	Hall amplifier hysteresis voltage		15	20	25	mV
ΔV_{HYS}	Hall amplifier hysteresis difference	Between U, V, W	–5		5	mV
V_{ID}	Hall amplifier input differential		50			mV
V_{CM}	Hall amplifier input common mode voltage range		1.5		3.5	V
I_{IN}	Input leakage current	Hx+ = Hx–	–10		10	µA
t_{HDEG}	Hall deglitch time			20		µs
MOSFET DRIVERS						
V_{OUTH}	High-side gate drive output voltage	I_O = 100 µA, VM ≥ 12V		VM + 10		V
V_{OUTL}	Low-side gate drive output voltage	I_O = 100 µA		10		V
I_{OUT}	Peak gate drive current			30		mA
CYCLE-BY-CYCLE CURRENT LIMITER						
$V_{LIMITER}$	Voltage limit across R_{ISENSE} for the current limiter		0.225	0.25	0.275	V
t_{BLANK}	Time that $V_{LIMITER}$ is ignored, from the start of the PWM cycle			6		µs
PROTECTION CIRCUITS						
$V_{SENSEOCP}$	Voltage limit across R_{ISENSE} for overcurrent protection		1.7	1.8	1.9	V
$t_{SENSEOCP}$	Deglitch time for $V_{SENSEOCP}$ to trigger			5		µs

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FETOCP}	Voltage limit across each external FET's drain		850	1000	1200	mV
t_{FETOCP}	Deglitch time for V_{FETOCP} to trigger			5		µs
V_{UVLO}	VM undervoltage lockout	VM rising		8		V
		VM falling		7.8		
V_{OVLO}	VM overvoltage lockout	VM rising	32	34	36	V
t_{RETRY}	Fault retry time after RLOCK or OTS			5		s
T_{TSD}	Thermal shutdown die temperature		150	160		°C
t_{LOCK}	Locked rotor detect time			3		s
V_{CPFAIL}	VCP failure threshold			VM + 3.0		V

7.6 Typical Characteristics

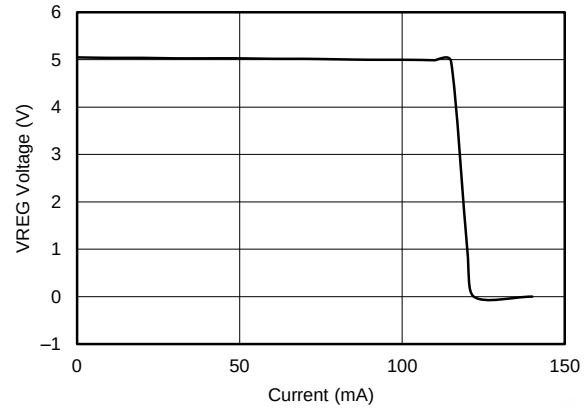
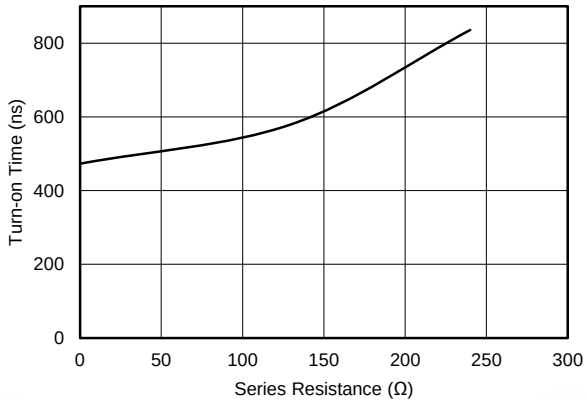


Figure 1. VREG Load Capability



With the CSD88537ND FETs, a series resistor was added to the high-side gate drive, and the V_{GS} rise time was measured.

Figure 2. FET Turn-On Time vs Series Resistance

8 Detailed Description

8.1 Overview

The DRV8307 device controls 3-phase brushless DC motors using a speed and direction input interface and Hall signals from the motor. The device drives N-channel MOSFETs with 10-V V_{GS} and a gate drive current of 30 mA.

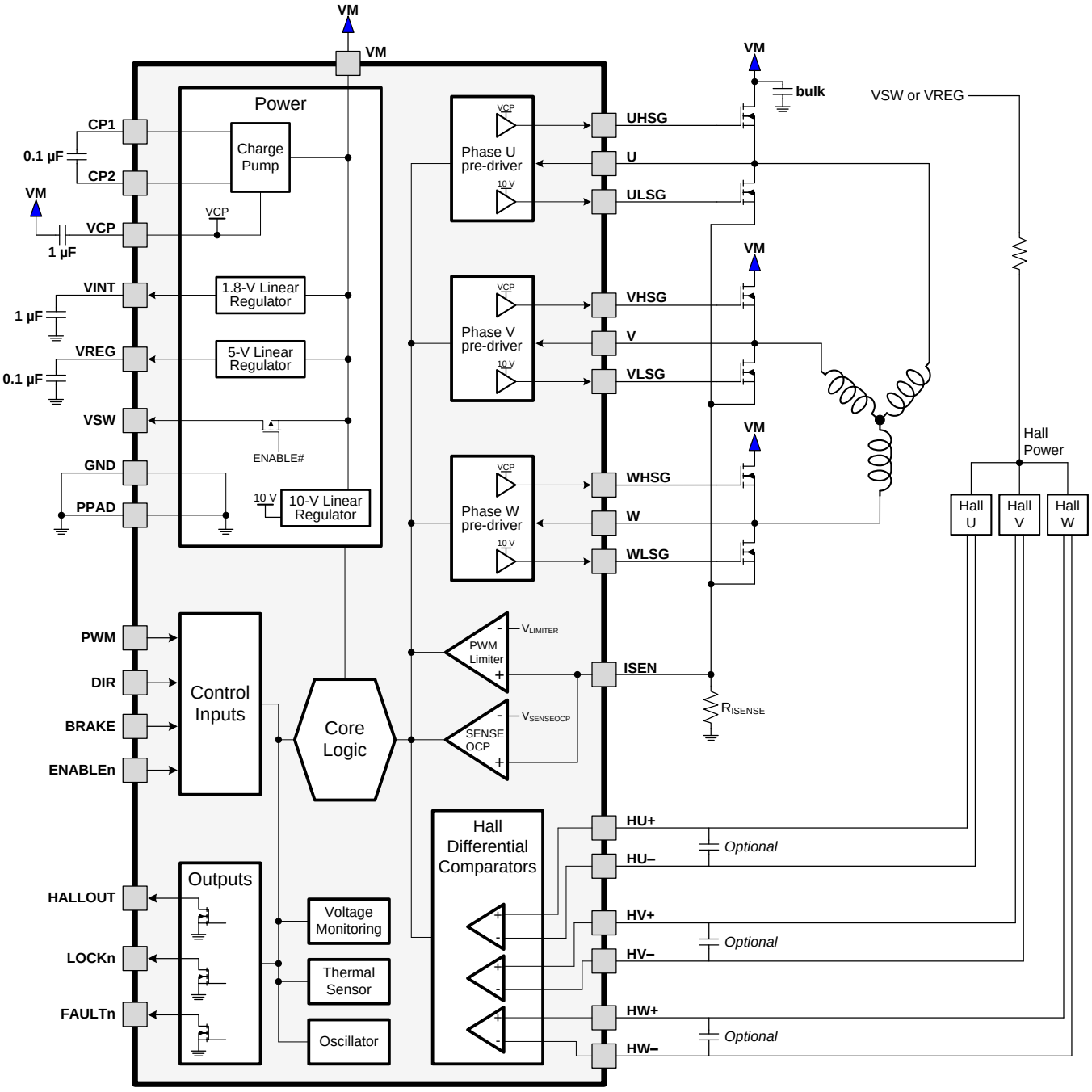
The speed of the motor is controlled by varying the duty cycle of the input clock (pulse-width modulation). Motor speed is indicated on the HALLOUT terminal, which follows the HALL U transitions.

When the DRV8307 device begins spinning a motor, it initially uses all three Hall sensor phases to commutate. After a constant speed is reached, the LOCKn terminal is pulled low and only one Hall sensor becomes used; this feature reduces jitter by eliminating the error caused by non-ideal Hall device placement and matching.

Numerous protection circuits prevent system components from being damaged during adverse conditions. Monitored aspects include motor voltage and current, gate drive voltage and current, device temperature, and rotor lockup. When a fault occurs, the DRV8307 device stops driving and pulls FAULTn low, in order to prevent FET damage and motor overheating.

The DRV8307 device is packaged in a compact 6 × 6-mm, 40-terminal VQFN with a 0.5-mm terminal pitch, and operates through an industrial ambient temperature range of –40°C to 85°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Hall Comparators

Three comparators are provided to process the raw signals from Hall effect transducers to commutate the motor. The Hall amplifiers sense zero crossings of the differential inputs and pass the information to digital logic.

The Hall amplifiers have hysteresis, and their detect threshold is centered at 0. Note, hysteresis is defined as shown in Figure 3:

Feature Description (continued)

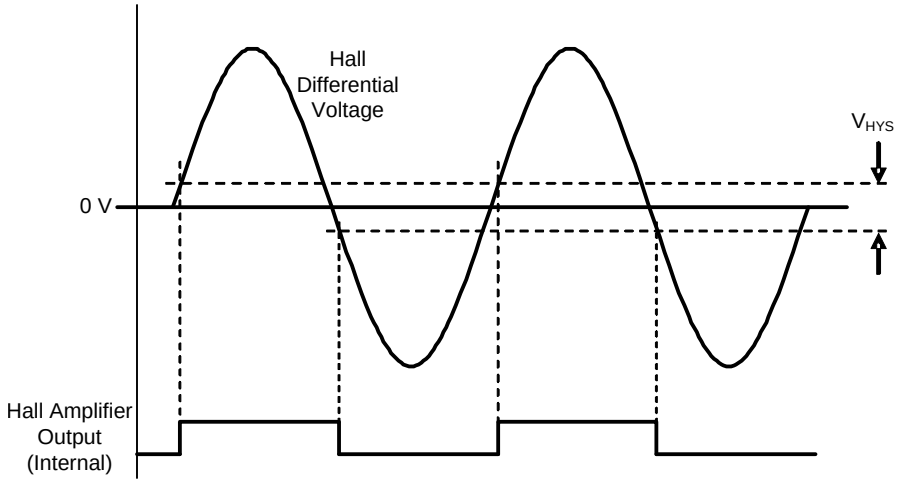


Figure 3. Hall Amplifier Hysteresis

In addition to hysteresis, the Hall inputs are deglitched with a circuit that ignores any extra Hall transitions for a period of 20 µs after sensing a valid transition. This prevents PWM noise from being coupled into the Hall inputs, which can result in erroneous commutation.

If excessive noise is still coupled into the Hall comparator inputs, it may be necessary to add capacitors between the + and – inputs of the Hall comparators, and (or) between the input or inputs and ground.

The ESD protection circuitry on the Hall inputs implements a diode to VREG. Because of this diode, the voltage on the Hall inputs should not exceed the VREG voltage.

Since VREG is disabled in standby mode (ENABLEn inactive), the Hall inputs should not be driven by external voltages in standby mode. The DRV8307 device specifies if the Hall sensors are powered from VREG or VSW; however, if the Hall sensors are powered externally, they should be disabled when the DRV8307 is put into standby mode. In addition, the Hall sensors should be powered-up before enabling the motor, or an invalid Hall state may cause a delay in motor operation.

8.3.2 HALLOUT Output

The HALLOUT terminal indicates the speed of the motor. It follows the transitions observed from the HALL U hall sensor. Figure 4 shows the HALLOUT signal.

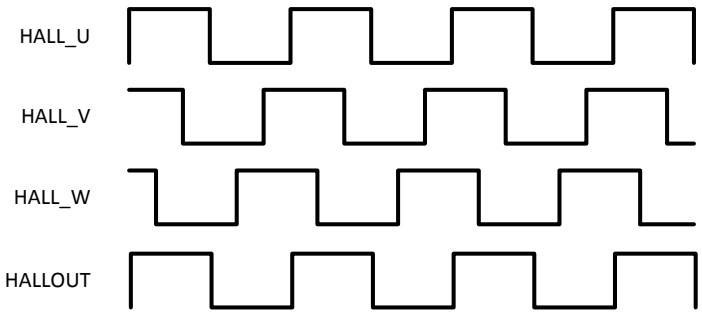


Figure 4. HALLOUT Relationship to Hall Transitions

8.3.3 Enable, Reset, and Clock Generation

The ENABLEn terminal is used to start and stop motor operation. The ENABLEn terminal is active low.

When ENABLEn is active, operation of the motor is enabled. When ENABLEn is made inactive, the motor coasts. After motor rotation has stopped (when no transitions occur on the HALLOUT terminal for a period of 1 s), the DRV8307 device enters a low-power standby state.

Feature Description (continued)

When in the standby state:

- The motor driver circuitry is disabled (all gate drive outputs are driven low, so the FET outputs are high-impedance).
- The gate drive regulator and charge pump are disabled.
- The VREG regulator and VSW power switch are disabled.
- All analog circuitry is placed into a low power state.
- The digital circuitry in the device still operates.

All internal logic is reset in two different ways:

- Upon device power-up
- When VM drops below V_{RESET}

An internal clock generator provides all timing for the DRV8307 device. The master oscillator runs at 100 MHz. This clock is divided to a nominal 50-MHz frequency that clocks the remainder of the digital logic.

8.3.4 Commutation

For 3-phase brushless DC motors, rotor position feedback is provided from Hall effect transducers mounted on the motor. These transducers provide three overlapping signals, each 60° apart. The windings are energized in accordance with the signals from the Hall sensors to cause the motor to move.

In addition to the Hall sensor inputs, commutation is affected by a direction control, which alters the direction of motion by reversing the commutation sequence. Control of commutation direction is by the DIR input terminal.

If the commanded direction changes while the motor is moving, the device allows the motor to coast until the motor stops. The stopped condition is determined by measuring the period of the HALL_U signal; when the period exceeds 160 ms, typical operation resumes and the motor starts spinning in the commanded direction. This prevents excessive current flow in the output stage if the motor is reversed while running at speed.

In standard 120° commutation, mis-positioning the Hall sensors can cause motor noise, vibration, and torque ripple. 120° commutation using a single Hall sensor (single-Hall commutation) can improve motor torque ripple and vibration because it relies on only one Hall edge for timing.

8.3.4.1 120° 3-Hall Commutation

In standard 120° commutation, the motor phases are energized using simple combination logic based on all three Hall sensor inputs.

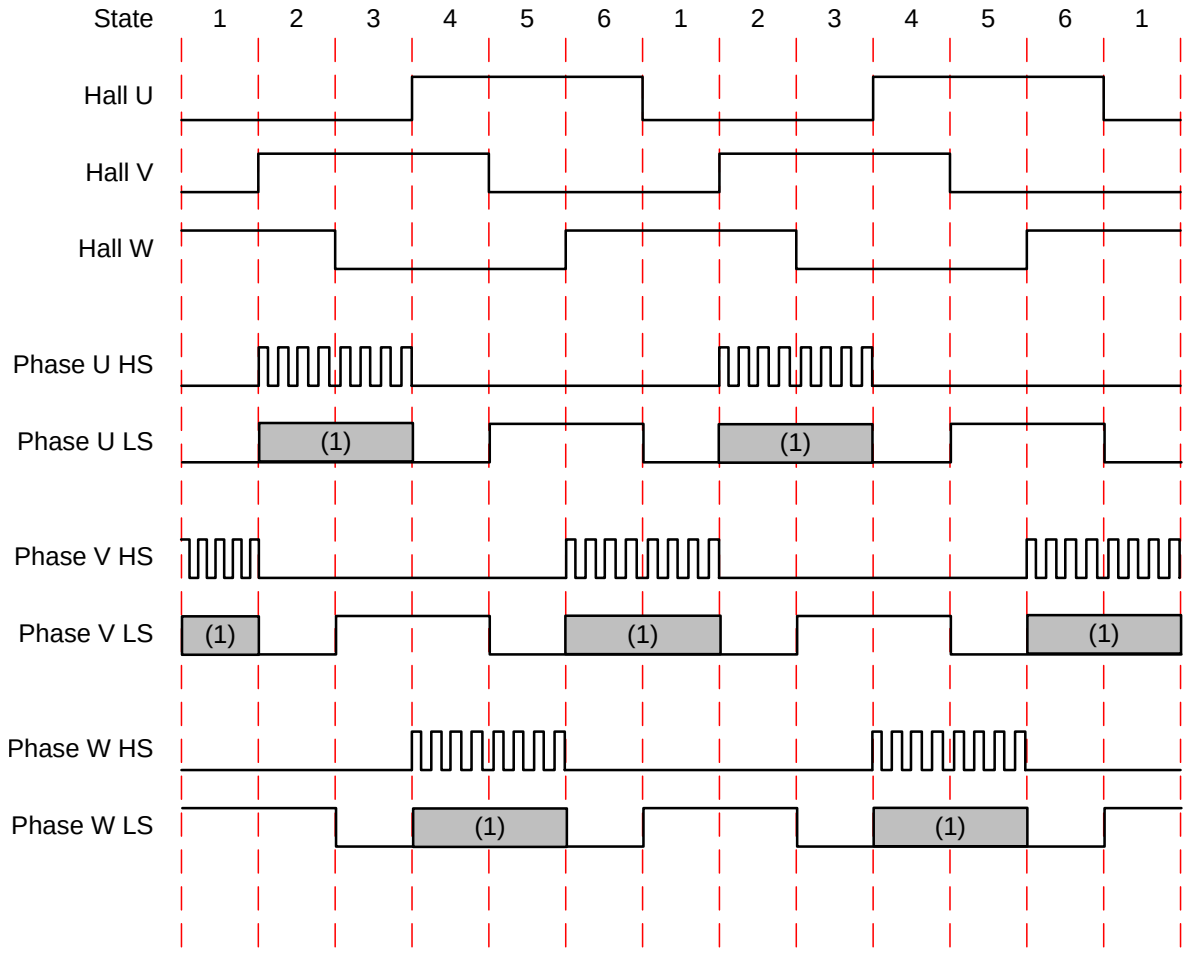
Standard 120° commutation is in accordance with Table 1, Figure 5, and Figure 6:

Feature Description (continued)

Table 1. Standard 120° Commutation(1)

STATE	HALL INPUTS						PRE-DRIVE OUTPUTS					
	DIR = 1			DIR = 0			Phase U		Phase V		Phase W	
	U_H	V_H	W_H	U_H	V_H	W_H	U_HSGATE	U_LSGATE	V_HSGATE	V_LSGATE	W_HSGATE	W_LSGATE
1	L	L	H	H	H	L	L	L	PWM	L / !PWM(2)	L	H
2	L	H	H	H	L	L	PWM	L / !PWM(2)	L	L	L	H
3	L	H	L	H	L	H	PWM	L / !PWM(2)	L	H	L	L
4	H	H	L	L	L	H	L	L	L	H	PWM	L / !PWM(2)
5	H	L	L	L	H	H	L	H	L	L	PWM	L / !PWM(2)
6	H	L	H	L	H	L	L	H	PWM	L / !PWM(2)	L	L
1X	H	H	H	L	L	L	L	L	L	L	L	L
2X	L	L	L	H	H	H	L	L	L	L	L	L

(1) Hall sensor is H if the positive input terminal voltage is higher than the negative input terminal voltage. States 1X and 2X are illegal input combinations.
(2) During states where the phase is driven with a PWM signal, using asynchronous rectification, the LS gate is held off (L); using synchronous rectification, the LS gate is driven with the inverse of the HS gate.



(1) !PWM for Sync Rectification

Figure 5. Standard 120° Commutation (DIR = 1)

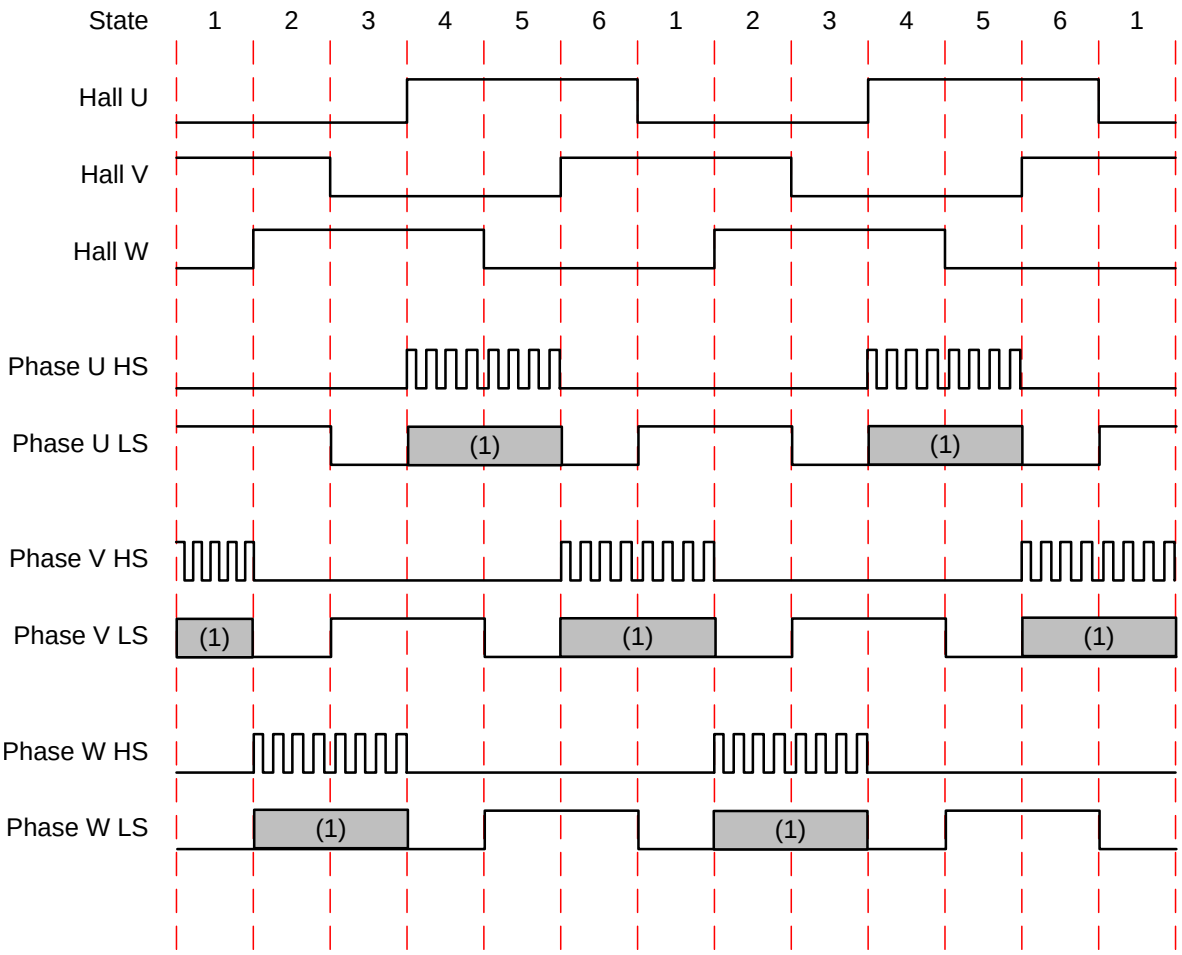


Figure 6. Standard 120° Commutation (DIR = 0)

8.3.4.2 120° Single-Hall Commutation

To generate commutation timing for single-Hall commutation, a digital timer is used to create a clock that runs at 960× the Hall sensor frequency. Only one Hall sensor input, HALL_U, is used for commutation; this eliminates any torque ripple caused by mechanical or electrical offsets of individual Hall sensors.

Single-Hall commutation is only enabled when the motor is operating at a nearly constant speed or speed-locked condition. To control this function, logic is used to determine when the speed is constant. This logic generates the LOCK signal. The LOCK signal is also output on the LOCKn terminal.

Until LOCK goes active (for example, at start-up, stop, or application of a sudden load that causes motor speed to drop very quickly), standard 120° commutation is used requiring all three Hall sensors.

Timing of 120° single-Hall commutation is essentially the same as standard 120° commutation shown previously. However, there are small time differences in when the transitions occur.

8.3.5 Braking

Motor braking can be initiated by the BRAKE terminal.

Table 2. Brake Behavior

BRAKE Terminal	Resulting Function
0	Not brake
1	Brake

When the motor is braking, all low-side drivers are held in an on state, causing all low-side FETs to turn on.

8.3.6 Output Pre-Drivers

The output drivers for each phase consist of N-channel and P-channel MOSFET devices arranged as a CMOS buffer. They are designed to directly drive the gate of external N-channel power MOSFETs. The outputs provide synchronous rectification operation. In synchronous rectification, the low-side FET is turned on when the high side is turned off.

The high-side gate drive output UHSG is driven to VCP whenever the duty cycle output U_PD from the PWM generator is high, the enable signal U_HS from the commutation logic is active, and the current limit ($V_{LIMITER}$) is not active. If the high-side FET is on and a current limit event occurs, the high-side FET is immediately turned off until the next PWM cycle.

The low-side gate drive ULSG is driven to VM whenever the internal signal U_LS is high, or whenever synchronous rectification is active and UHSG is low.

Phases V and W operate in an identical fashion.

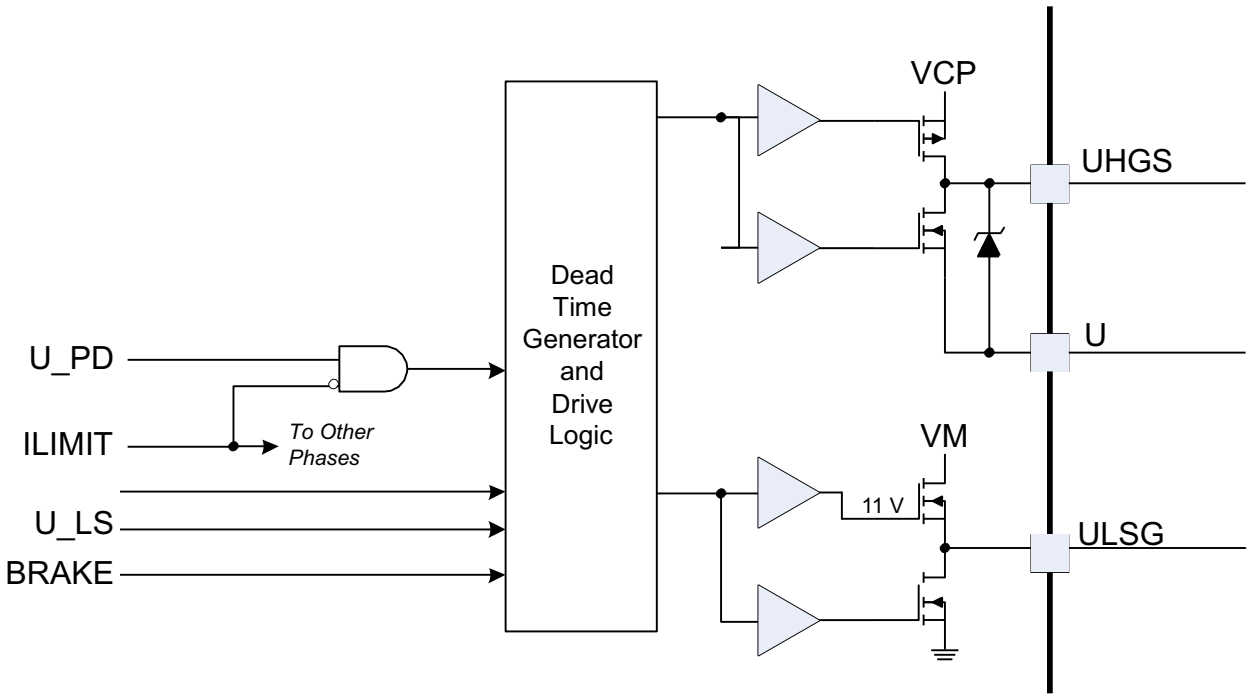


Figure 7. Pre-Driver Block Diagram

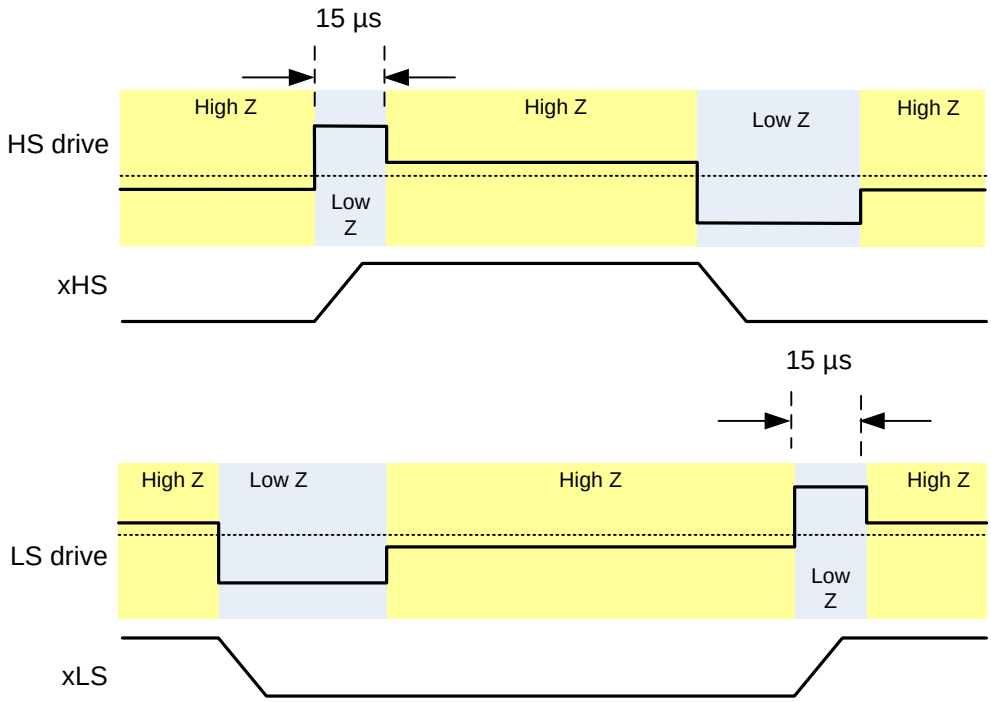


Figure 8. Gate Control Behavior

The peak drive current of the pre-drivers is fixed at 30 mA.

When changing the state of the output, the peak current is applied for a short period of time (15 µs) to charge the gate capacitance. After this time, a weak current source is used to keep the gate at the desired state.

During high-side turn-on, the low-side gate is held low with a low impedance. This prevents the gate-source capacitance of the low-side FET from inducing turn-on. Similarly, during low-side turn-on, the high-side gate is held off with a low impedance.

The pre-driver circuits include enforcement of a dead time in analog circuitry, which prevents the high-side and low-side FETs from conducting at the same time.

8.3.7 Current Limit

The current limit circuit activates if the voltage detected across the low-side sense resistor exceeds $V_{LIMITER}$. Note that the current limit circuit is ignored immediately after the PWM signal goes active for a short blanking time, to prevent false trips of the current limit circuit.

If current limit activates, the high-side FET is disabled until the beginning of the next PWM cycle. If synchronous rectification is enabled when the current limit activates, the low-side FET is activated while the high-side FET is disabled.

8.3.8 Charge Pump

Since the output stages use N-channel FETs, a gate drive voltage higher than the VM power supply is needed to fully enhance the high-side FETs. The DRV8307 device integrates a charge pump circuit that generates a voltage approximately 10 V more than the VM supply for this purpose.

The charge pump requires two external capacitors for operation. For details on these capacitors (value, connection, and so forth), refer to Figure 9.

The charge pump is shut down when in standby mode (ENABLEn inactive).

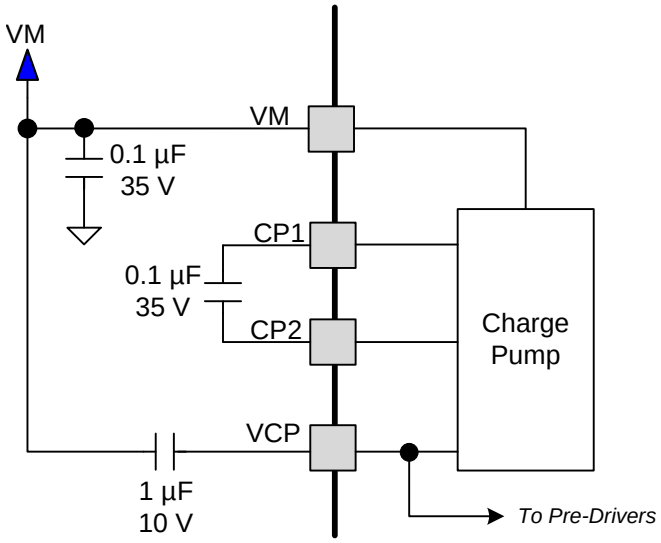


Figure 9. Charge Pump Block Diagram

8.3.9 5-V Linear Regulator

A 5-V linear regulator (VREG) is provided to power internal logic and external circuitry, such as the Hall effect sensors.

A capacitor must be connected from the VREG output to ground, even if the output is not used for external circuitry. The recommended capacitor value is a 0.1-µF, 10-V ceramic capacitor.

The VREG output is designed to provide up to 30-mA output current, but power dissipation and thermal conditions must be considered. As an example, with 24 V in and 20 mA out, power dissipated in the linear regulator is 19 V × 20 mA = 380 mW.

The VREG regulator is shutdown in standby mode (when ENABLEn is inactive).

8.3.10 Power Switch

A low-current switch is provided in the DRV8307 device that can be used to power the Hall sensors or other external circuitry through the VSW terminal. When ENABLEn is active the switch is turned on, connecting the VSW terminal to VM. When ENABLEn is inactive the switch is turned off (standby mode).

8.3.11 Protection Circuits

A number of protection circuits are included in the DRV8307 device. Faults are reported by asserting the FAULTn terminal (an active-low, open-drain output signal).

8.3.11.1 VM Undervoltage Lockout (UVLO)

If the VM power supply drops, there may not be enough voltage to fully turn on the output FETs. Operation in this condition causes excessive heating in the output FETs. To protect against this, the DRV8307 device contains an UVLO circuit.

In the event that the VM supply voltage drops below the UVLO threshold (V_{UVLO}), the FAULTn terminal is driven active and the motor driver is disabled. After VM returns to a voltage above the UVLO threshold, the FAULTn terminal is high impedance and operation of the motor driver automatically resumes.

8.3.11.2 VM Overvoltage (VMOV)

In some cases, energy from the mechanical system can be forced back into the VM power supply. This can result in the VM power supply being boosted by the energy in the mechanical system, causing breakdown of the output FETs, or damaging the DRV8307 device. To protect against this, the DRV8307 device has overvoltage protection.

An overvoltage event is recognized if the VM voltage exceeds the overvoltage threshold (VM_{OVLO}). Note that for the output FETs to be protected, they must be rated for a voltage greater than the selected overvoltage threshold.

In the event of an overvoltage, the FAULTn terminal is pulled low. The output stage is forced into asynchronous rectification. After VM returns to a voltage below the overvoltage threshold, the FAULTn terminal is high impedance. After a fixed 60-µs delay, synchronous rectification is re-enabled.

8.3.11.3 Motor Overcurrent Protection (OCP)

OCP is provided on each FET in addition to the current limit circuit. The OCP circuit is designed to protect the output FETs from atypical conditions such as a short circuit between the motor outputs and each other, power, or ground.

The OCP circuit is independent from the current limit circuitry. OCP works by monitoring the voltage drop across the external FETs when they are enabled. If the voltage across a driven FET exceeds V_{FETOCP} for more than t_{FETOCP} an OCP event is recognized.

In addition to monitoring the voltage across the FETs, an OCP event is triggered if the voltage applied to the ISEN terminal exceeds the $V_{SENSEOCP}$ threshold voltage.

In the event of an OCP event, FAULTn is pulled low and the motor driver is disabled.

After a fixed delay of 5 ms, the FAULTn terminal is driven inactive and the motor driver is re-enabled.

8.3.11.4 Charge Pump Failure (CPFAIL)

If the voltage generated by the high-side charge pump is too low, the high-side output FETs are not fully turned on and excessive heating results. To protect against this, the DRV8307 device has a circuit that monitors the charge pump voltage.

If the charge pump voltage drops below V_{CPFAIL}, the FAULTn terminal is pulled low and the motor driver is disabled. After the charge pump voltage returns to a voltage above the V_{CPFAIL} threshold, the FAULTn terminal is high impedance and operation of the motor driver automatically resumes.

8.3.11.5 Charge Pump Short (CPSC)

To protect against excessive power dissipation inside the DRV8307 device, a circuit monitors the charge pump and disables it in the event of a short circuit on the PCB.

If a short circuit is detected on the charge pump, the FAULTn terminal is pulled low and the motor driver is disabled. After a fixed period of 5 s, the FAULTn terminal is high impedance and operation of the motor driver automatically resumes. If the short circuit condition is still present, the cycle repeats.

8.3.11.6 Rotor Lockup (RLOCK)

Circuitry in the DRV8307 device detects a locked or stalled rotor. This RLOCK can occur in the event of a mechanical jam or excessive torque load that causes the motor to stop rotating while enabled. The rotor lock condition is set if there are no transitions detected on the HALLOUT signal for 3 s. RLOCK can also occur if the three Hall signals are an invalid state (all High or all Low), which can be caused by a bad wire connection. If the BRAKE terminal goes high for longer than 3 s while the PWM clock is on DRV8307 will detect RLOCK.

If a locked rotor condition is recognized, the FAULTn terminal is pulled low and the motor driver is disabled. The part re-enables itself after a fixed delay of 5 s.

8.3.11.7 Overtemperature (OTS)

To protect against any number of faults that could result in excessive power dissipation inside the device, the DRV8307 device includes overtemperature protection.

Overtemperature protection activates if the temperature of the die exceeds the OTS threshold temperature (T_{TSD}). If this occurs, the FAULTn terminal is pulled low and the device is disabled. The part re-enables itself after a fixed delay of 5 s.

8.4 Device Functional Modes

8.4.1 Clock PWM Mode

In PWM input mode, the PWM input signal is timed using a 50-MHz clock to generate a 12-bit number that corresponds to the duty cycle of the incoming PWM signal. The input PWM frequency should be between 16 and 50 kHz; higher PWM frequencies work, but resolution is degraded. Note that the gate driver's output PWM frequency is independent of the speed control PWM input frequency; the output PWM frequency is 25 kHz.

The outputs of the PWM generators are the signals U_PD, V_PD, and W_PD. These contain the duty cycle information for each phase.

Figure 10 shows modulation and PWM generation.

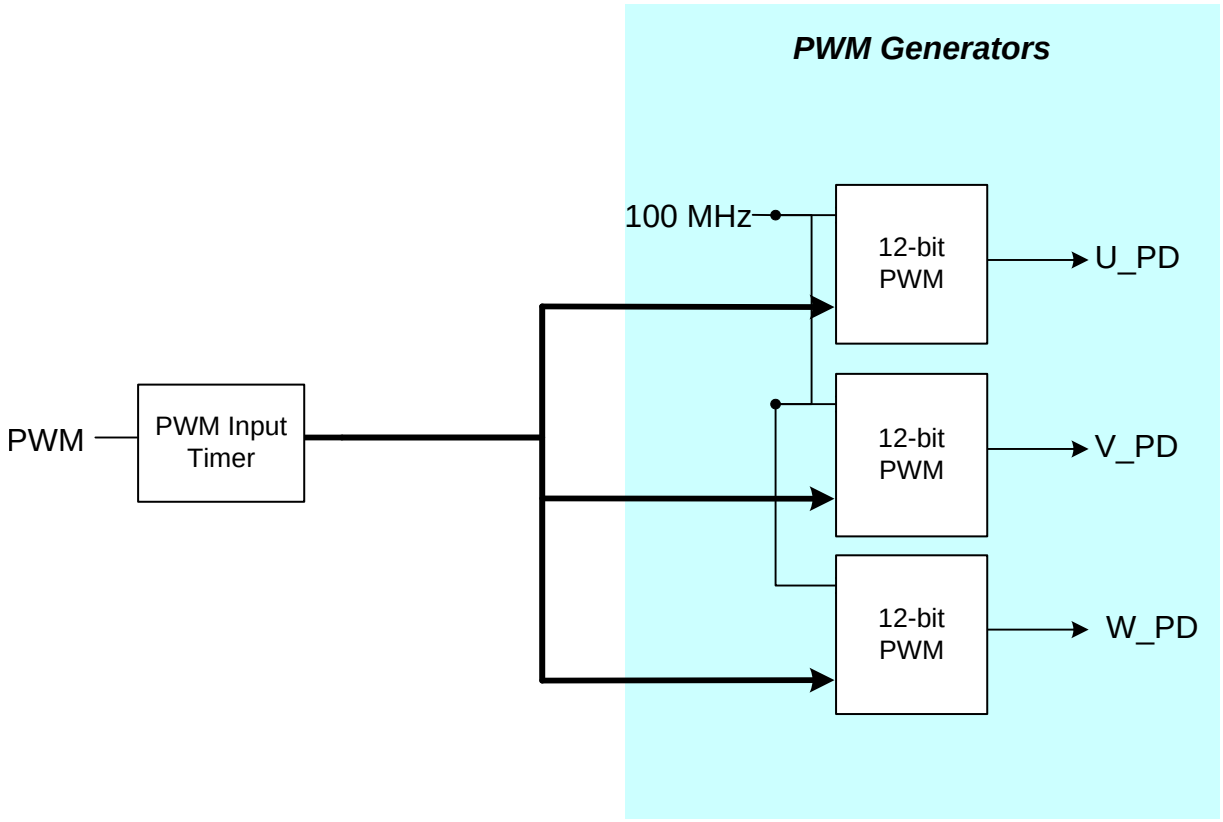


Figure 10. Modulation and PWM Generation

9 Application and Implementation

9.1 Application Information

9.1.1 Hall Sensor Configurations and Connections

The Hall sensor inputs on the DRV8307 device are capable of interfacing with a variety of Hall sensors. Typically, a Hall element is used, which outputs a differential signal on the order of 100 mV. To use this type of sensor, the VREG regulator can be used to power the Hall sensor. Figure 11 shows the connections.

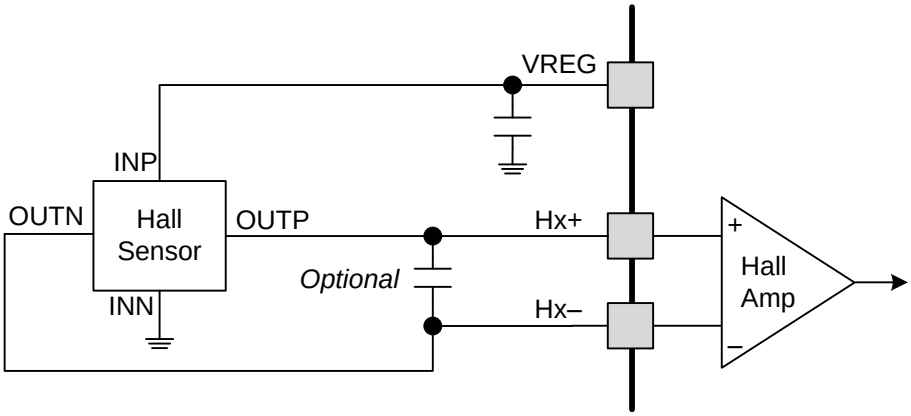


Figure 11. Differential Hall Sensor Connections

Since the amplitude of the Hall sensor output signal is very low, often capacitors are placed across the Hall inputs to help reject noise coupled from the motor PWM. Typically capacitors from 1 to 10 nF are used.

Some motors use digital Hall sensors with open-drain outputs. These sensors can also be used with the DRV8307 device, with the addition of a few resistors (see Figure 12).

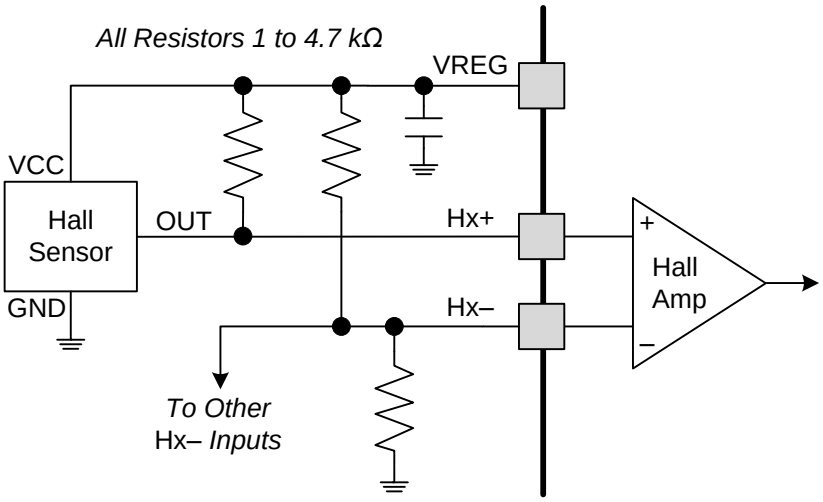


Figure 12. Single-Ended Hall Sensor Connections

The negative (Hx–) inputs are biased to 2.5 V by a pair of resistors between VREG and ground. For open-collector Hall sensors, an additional pullup resistor to VREG is needed on the positive (Hx+) input.

9.1.2 ENABLEn Considerations

Because the ENABLEn function doubles as a sleep (low-power shutdown) function, there are some important considerations when asserting and deasserting ENABLEn.

Application Information (continued)

While the motor driver is enabled, the deassertion of ENABLEn initiates a stop-and-power-down sequence. This sequence starts by disabling the motor (coasting) and waiting for rotation to stop. After rotation is stopped for 1 s (as determined by the absence of transitions on HALLOUT), the internal circuitry is powered-down, the V5 regulator and power switch are disabled, and internal clocks are stopped.

After this stop-and-power-down sequence has been initiated (by deasserting the ENABLEn terminal for at least 1.2 µs), the sequence continues to completion, regardless of the state of ENABLEn. If ENABLEn is immediately returned to the active state, the motor slows and stops for 1 s, then starts again.

9.2 Typical Application

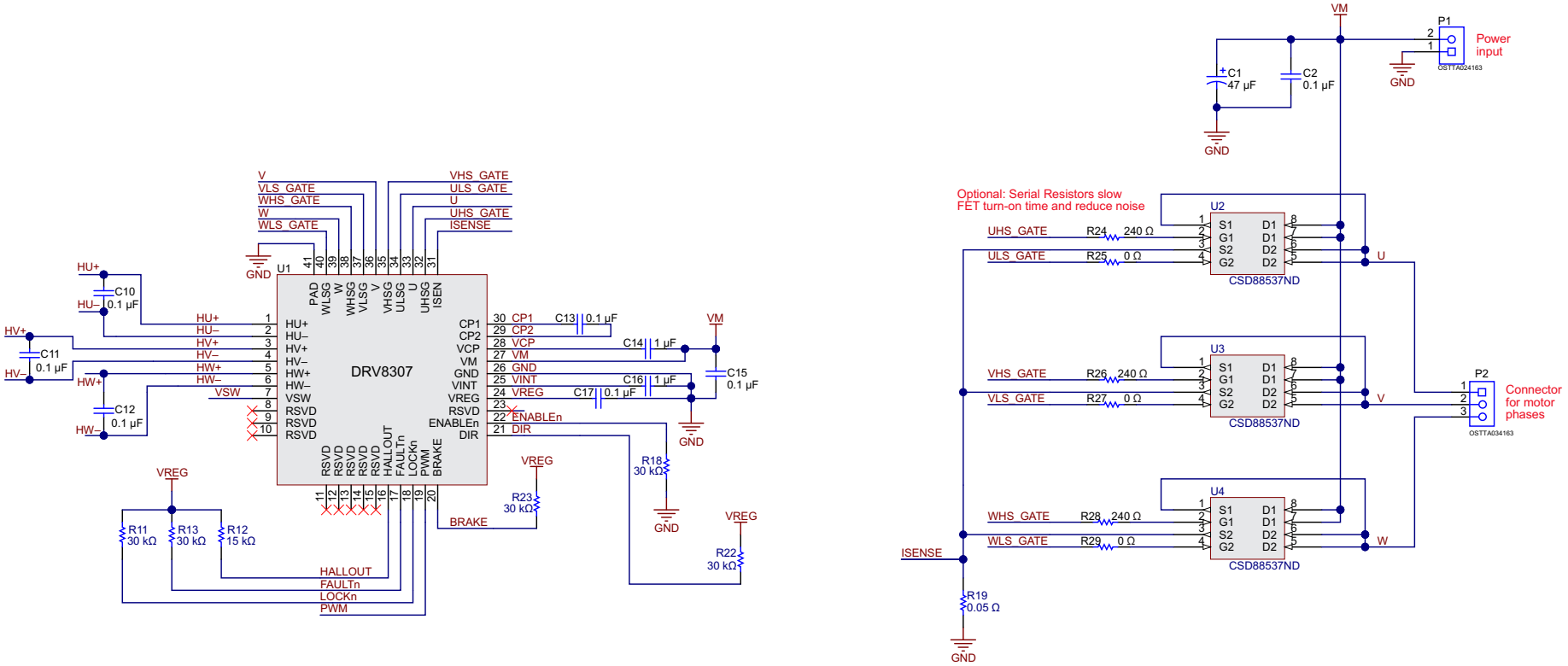


Figure 13. Schematic

9.2.1 Design Requirements

Design Parameter	Value
Supply voltage	8.5 to 32 V
PWM frequency	16 to 50 kHz
PWM duty cycle	0% to 100%
Current limiter	$V_{LIMITER}$ / R_{ISENSE}
External FETs	N-channel MOSFETs
Bulk supply capacitance	2 to 4 µF per watt

9.2.2 Detailed Design Procedure

When designing a system with the DRV8307, determine an operating motor voltage between 8.5 to 32 V. Higher voltages directly scale motor speed, with the same PWM input.

The frequency of the input clock (PWM) must be between 16 and 50 kHz. Note that this frequency does not affect the pre-driver output frequency, which is fixed at 25 kHz (typical).

The PWM duty cycle controls motor speed and can be set either to a fixed value or varied while the motor is spinning. If it is changed while spinning, use gradual steps (for example, 1% increments), because a large change in the commanded duty cycle can cause a large step in commutation, which can lock up the motor. This behavior is typical with other industry devices.

The DRV8307 device constantly monitors motor current and reduces FET drive when necessary, to keep current within $V_{LIMITER}$ / R_{ISENSE}. This feature reduces the requirements of power supply current capacity and bulk capacitance to maintain a stable voltage, especially during motor startup. The designer should target a peak current limit and size R_{ISENSE} appropriately. $V_{LIMITER}$ is fixed at 0.25 V (typical).

$$R_{ISENSE} = 0.25\ V / I_{PEAK} \quad (1)$$

For example, if 4-A peak is desired, then a 0.06-Ω resistor should be chosen as in Equation 2.

$$0.06\ \Omega = 0.25\ V / 4\ A \quad (2)$$

When selecting the power FETs, use six N-channel MOSFETs. They must support V_{GS} > 10 V (since the DRV8307 device drives 10 V V_{GS}). They must also support V_{DS} > VM, and TI recommends to have 1.5× to 2× margin, to prevent FET damage during transient voltage spikes that can occur when motors change speeds.

It is important to use large bulk capacitance on VM, and the required size depends on the power of the motor. Of course, power = voltage × current. A general recommendation is to use 2 to 4 µF per watt. If a motor system uses 24 V and 3 A, a reasonable choice is 144 to 288 µF.

9.2.3 Application Performance Plot

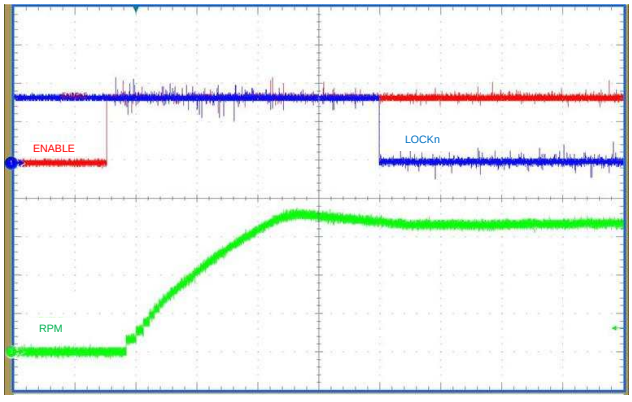


Figure 14. Typical Spinup Profile

10 Power Supply Recommendations

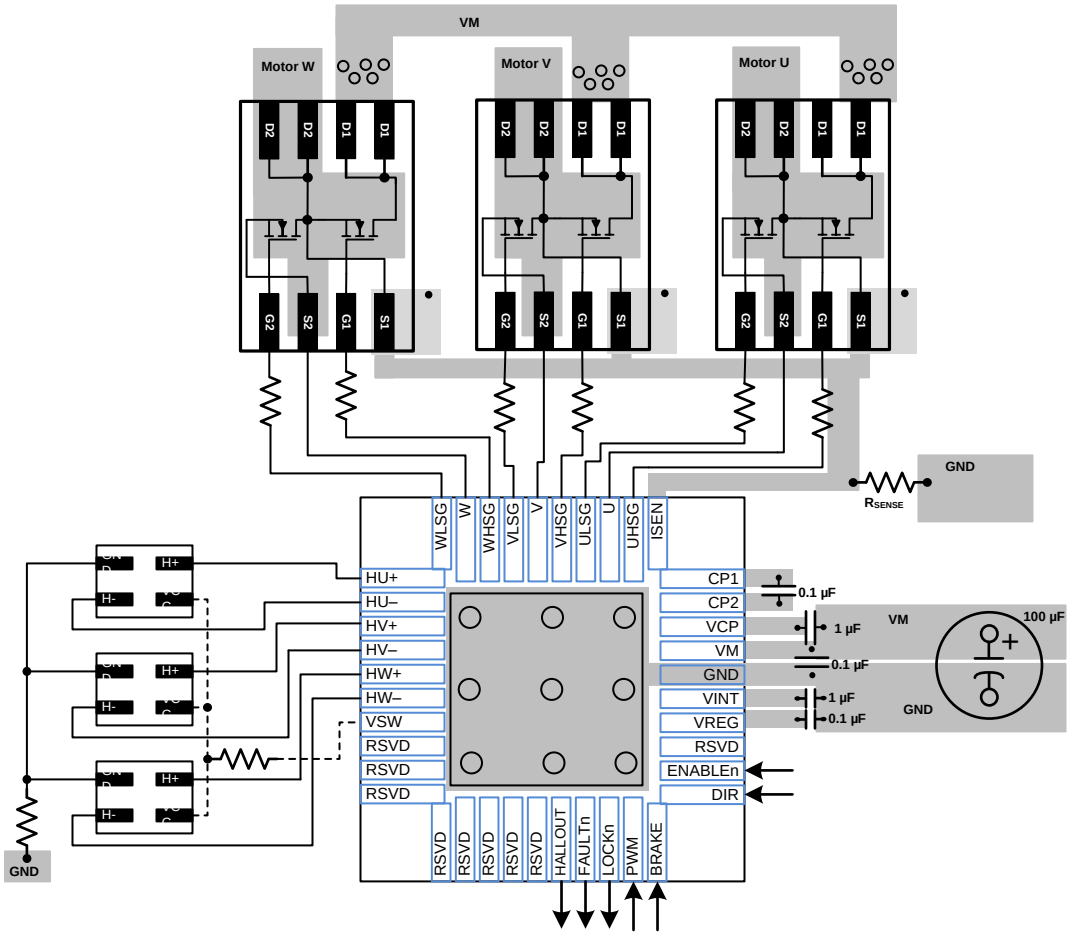
The DRV8307 device is designed to operate from an input voltage supply range between 8.5 and 32 V. This supply should be well regulated. TI recommends using a minimum bulk capacitance of 47 µF to minimize transients on the supply.

11 Layout

11.1 Layout Guidelines

For VM, place 0.1-µF bypass capacitor close to the device. Take care to minimize the loop formed by the bypass capacitor connection from VM to GND.

11.2 Layout Example



12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8307RHAR	ACTIVE	VQFN	RHA	40	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8307	Samples
DRV8307RHAT	ACTIVE	VQFN	RHA	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8307	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

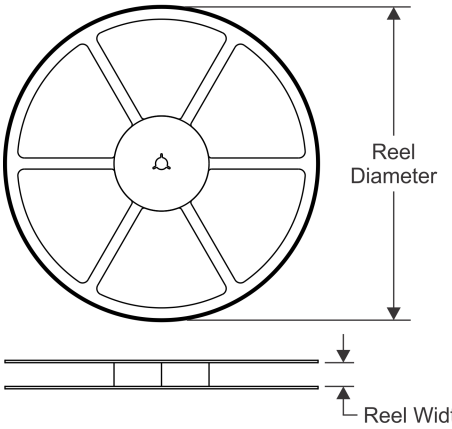
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

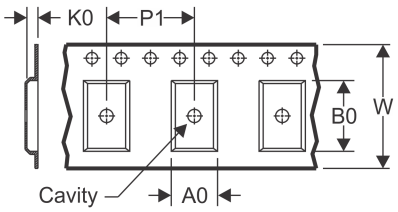
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

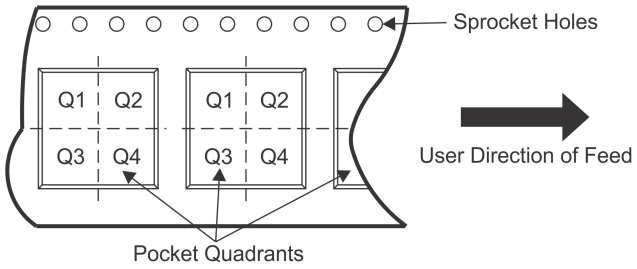


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

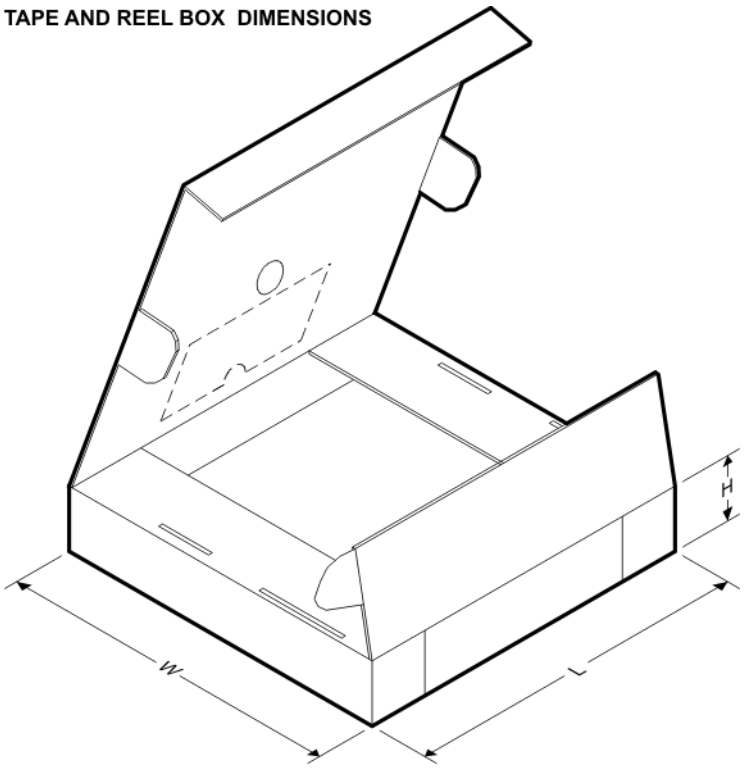
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8307RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8307RHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

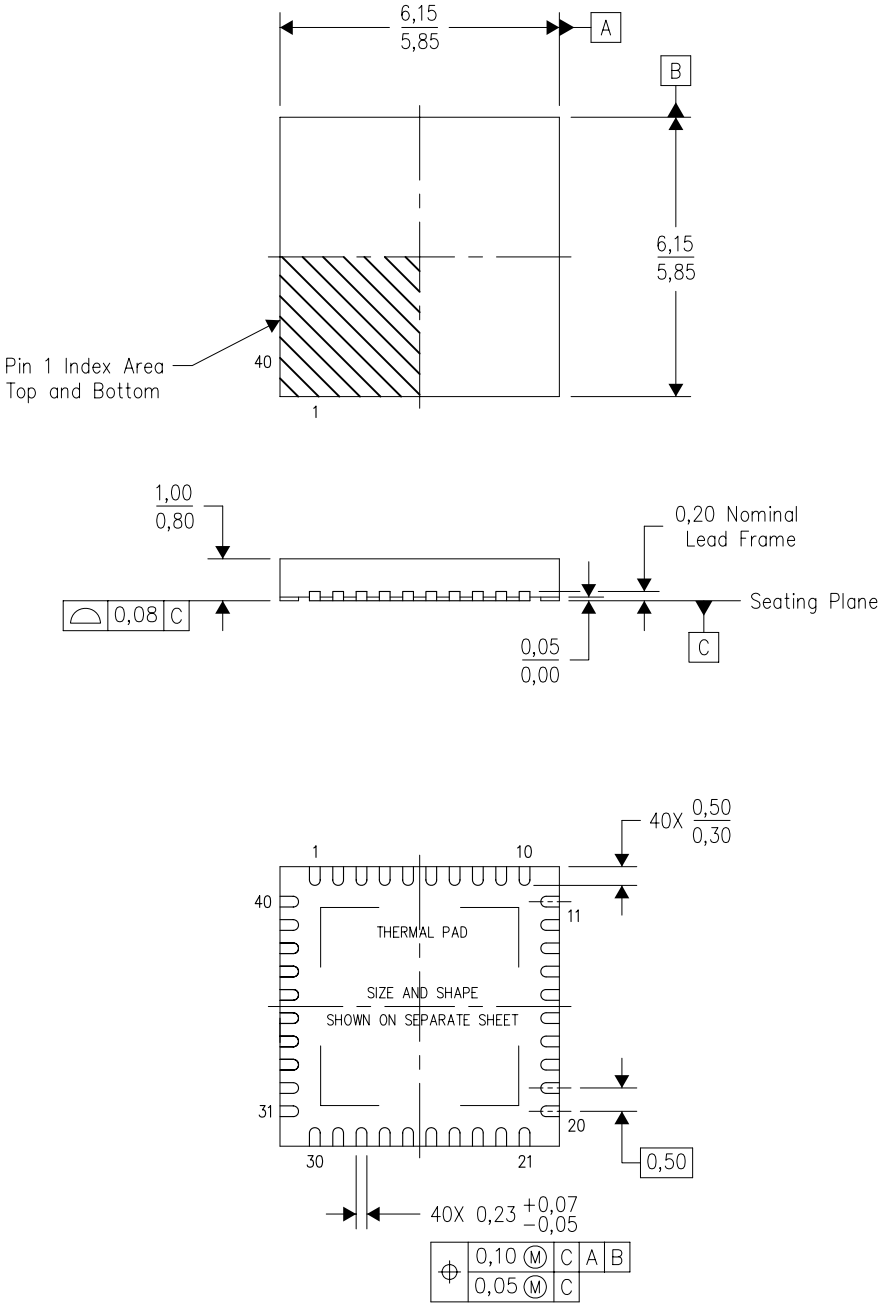
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8307RHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DRV8307RHAT	VQFN	RHA	40	250	210.0	185.0	35.0

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

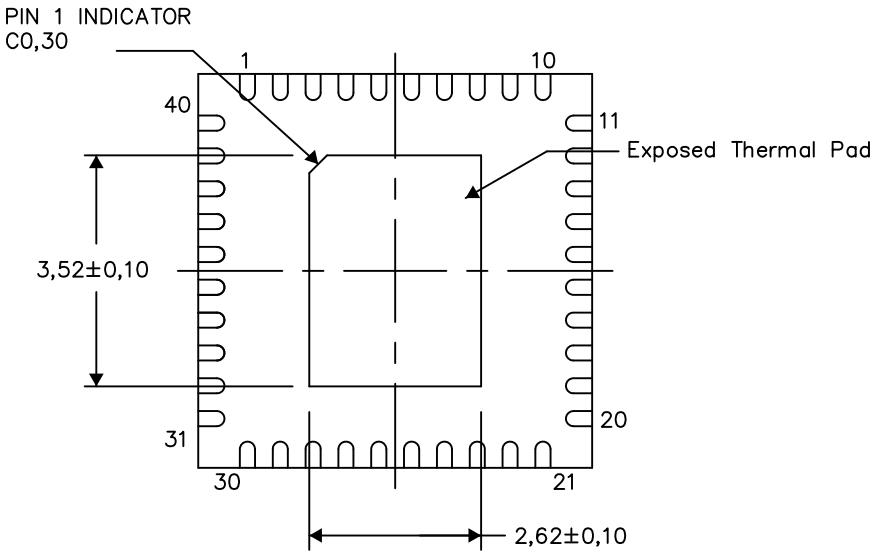
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



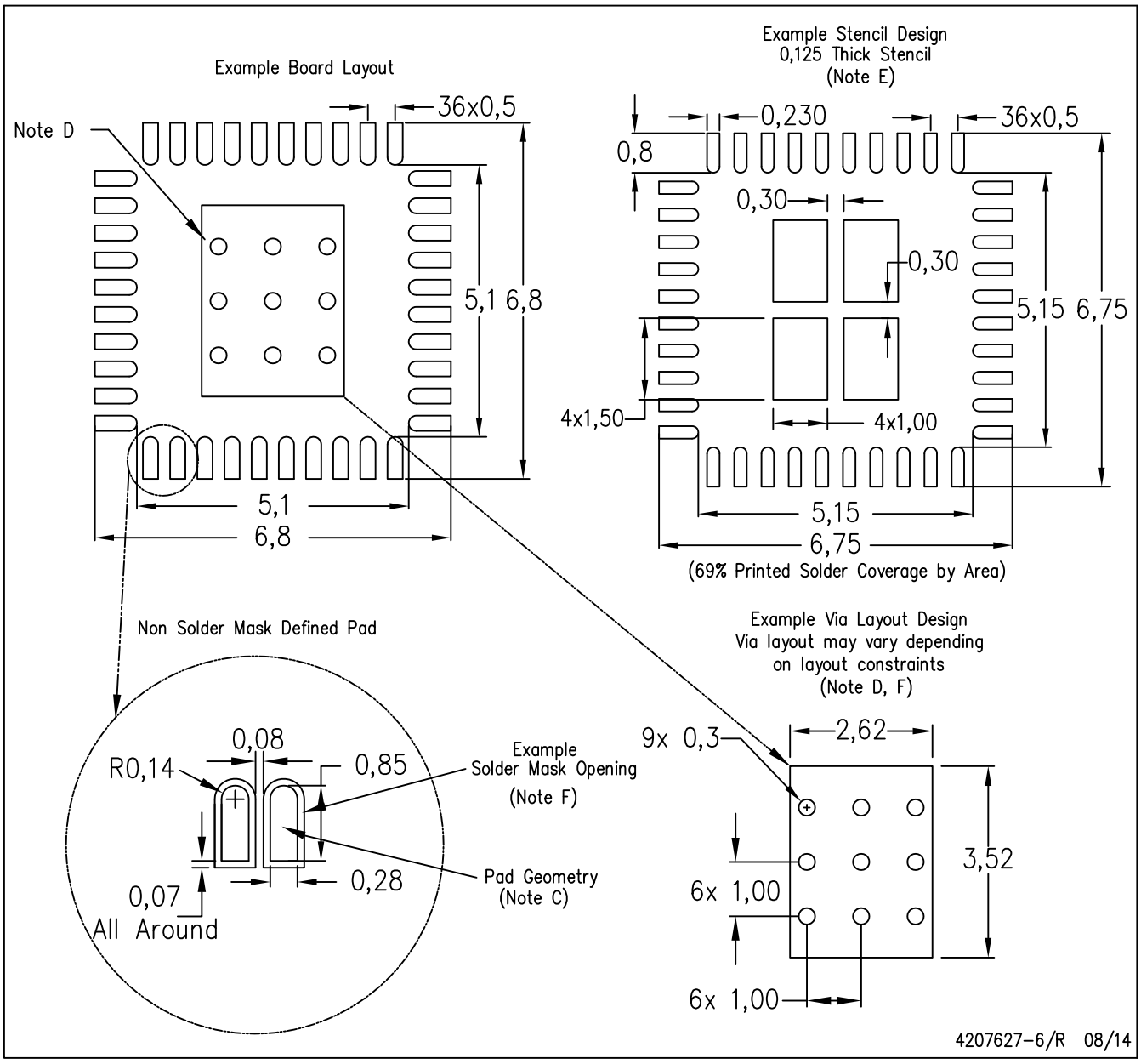
Bottom View

Exposed Thermal Pad Dimensions

4206355–9/X 08/14

NOTES: A. All linear dimensions are in millimeters

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
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Logic	logic.ti.com	Security	www.ti.com/security
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