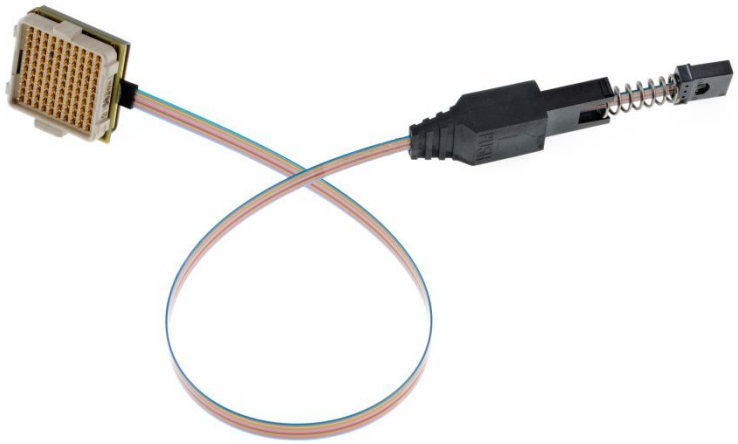
D-Light DLT-xx-251-lw-Pyz-Lvv
2 to 12 channels 4.25 Gbps optoelectronic transmitter

Features

- Up to 4.25 Gbps per channel
- 2 to 12 independent transmitters in a single package
- Each channel complies with IEEE Std. 802.3z Gigabit Ethernet 1000 Base-Sx PMD requirements as 2 GEth
- Also suitable for Fibre Channel, Infiniband and VSR-1 requirements
- Qualified over the industrial temperature range [-40;+85°C]
- Standard electrical SMT interface
- Small package size (16x16x3mm)
- Pigtailed optical connectics
- Low power consumption
- Single 3.3 V power supply



Applications

- Sensors interconnects
- Radar datacommunication
- Numerical video transmission
- Board-to-board communications
- Severe environment interconnects
- Space application

Product Description

D-Light DLT-xx-251-lw-Pyz parallel optoelectronic modules transmit high data rate signals on either 2, 4, 8 or 12 independent channels. They are optimized for short distance high data rate optical communications on multimode ribbon fiber and fully comply with ARINC804 Standard. They are protocol independent and can be applied to Gigabit Ethernet (both 1GBE and 10 GBE), Fibre Channel, Infiniband or any specific communication application in over [-40;+85°C].

DLT-xx-251-lw-Pyz modules integrate state-of-the art 850-nm GaAs VCSEL arrays and are optimized for low power consumption (<125 mW for each transmitter channel).

DLT-xx-251-lw- are available in various package such as surface mount or pluggable ones and various multimode fiber ribbon pigtail termination are offered around the standardized MT ferrule.

Ordering Information

Several versions of D-Light optoelectronic transmitters are currently available. DLT-xx-251-lw-Pyz optical interface consists of a multimode ribbon fiber pigtail terminated by any MT-ferule compatible connectors (other configuration available upon request).

DLT-xx-251-lw-Pyz-Lvv

- vv : Pigtail Length → Length in cm (see page 22 for details)
- z : Fibres diameter
  - 1 ↔ 50/125µm bare fiber
  - 2 ↔ 62.5/125µm bare fiber
- y : Connector type
  - O ↔ MPO/MPX connector
  - T ↔ MTP connector
  - N ↔ MT ferule only
  - M ↔ MT ferule plus spring
- w : Packaging option
  - L ↔ 48-Pin LCC package
  - GM↔ 100-Pin Meg-Array socketed package
- xx : number of channel
  - 02 ↔ 2 channels
  - 04 ↔ 4 channels
  - 08 ↔ 8 channels
  - 12 ↔ 12 channels

DATASHEET

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Absolute Maximum Ratings

Stress beyond these values may cause permanent damage to the device.

Parameter	Symbol	Min	Max	Unit	Notes
Storage temperature	T_{st}	-55	+125	°C	-
Soldering temperature	T_{sol}	-	230	°C	-
Soldering time	t_{sol}	-	60	s	-
Supply voltage	V_{CC}	-0.3	+4.0	V	-
Signal pins voltage range	V_{pin}	V_{EE}-0.3	V_{CC}+0.3	V	-
Differential input voltage	ΔV_{in}	-	1.2	V	-
Junction temperature	T_j	-	130	°C	-
ESD resistance voltage	ESD	-	1	KV	1

Notes:

1. Human Body Model (HBM) according to JESD22-A114-B.

Module specifications – General

VCC=3.3V, VEE=GND=0V

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply voltage		V_{CC}	3.0	3.3	3.6	V	-
Supply voltage noise		N_{VCC}	-	-	100	mV	1
Supply current		I_{CC}	-	xx·20	400	mA	2
Power supply noise rejection		PSR	-	-	15	dB	-
Power consumption	12 channels	P_{tot}	-	650	1300	mW	3
	Per channel	P_{ch}	-	115	145	mW	3
Tx enable/disable voltage	Disabled	V_{dis}	0	-	0.8	V	4
	Enabled	V_{en}	V_{CC}-1.3	-	V_{CC}	V	4
Data rate per channel		B	-	2.5	4.25	Gbps	5
Qualified temperature		T_{op}	-40	-	+90	°C	6

Notes:

1. For noise frequencies < 10MHz
2. xx represents the number of channel, the maximum supply current is for 12 channels.
3. Power consumption per or for 12 channels operating at full speed overall the temperature range (3.6v).
4. The module is normally disabled (i.e. when the Tx Enable control input is not connected). When the Tx Enable control input voltage is higher than V_{cc}-1.3, the module is powered up.
5. Operation at 4.25Gbps Transmitter impact the channel crosstalk penalty from 2 dB max to 3dB max and the extinction ratio to min value of 7dB.
6. Module operates over [-55;+100°C] with limited degraded performances.

Module specifications – High Speed Electrical

VCC=3.3V, VEE=GND=0V, Temp = [-40;+90°C]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Number of channels	N_{ch}	2	-	12	-	-
Input voltage range	V_{INx}	V_{EE}+0.8	-	V_{CC}+0.2	V	-
Differential input voltage	V_{INpp}	200	-	1900	mV	1
Single-ended input voltage	$\lvert V_{xP}-V_{xN}\rvert$	100	-	950	mV	1
Input common mode range	V_{xCM}	1.125	1.2	1.375	V	-
Input impedance	Z_{in}	80	100	120	Ω	-
Input Rise/Fall Time	t_{inR},t_{inF}	50	-	150	ps	2
Input capacitance (each input)	C_{in}	-	0.5	-	pF	-
Channel crosstalk penalty	X_{Popt}	-	1	2	dB	3

Notes:

1. 100mV for HS signals, 150mV required for ACJTAG functionality over complete range
2. Measured at 1.25Gbps and with 20% / 80% levels
3. For adjacent channels in worst case at full speed (one channel at receiver sensitivity & adjacent channel at receiver saturation).

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Module specifications – Digital Electrical

VCC=3.3V, VEE=GND=0V, Temp = [-40;+90°C]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Digital input voltage (CMOS)	High	V_{high}	2	-	V_{CC}	V	1
	Low	V_{low}	V_{EE}	-	V_{EE}+0.8	V	1
Digital output voltage (CMOS)	High	V_{high}	2.4	-	V_{CC}	V	1
	Low	V_{low}	V_{EE}	-	V_{EE}+0.4	V	1
Digital input voltage (Serial)	High	V_{high}	2	-	V_{CC}	V	-
	Low	V_{low}	V_{EE}	-	V_{EE}+0.8	V	-
Serial Interface input capacitance		C_I	-	-	10	pF	-
Serial Interface Rise Time		t_r	-	-	1	µs	-

Notes:

1. Compatible with JESD8-B CMOS digital level specifications.

Module specifications - Optical

VCC=3.3V, VEE=GND=0V, Temp = [-40;+90°C]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Center wavelength	λ_C	830	850	860	nm	-
Spectral width – rms	$\Delta\lambda$	-	-	1	nm	-
Core diameter of the Tx optical fiber pigtail	D_C	50	-	62.5	µm	1
Optical output power per channel	P_{out}	-4	-3	-0.67	dBm	2,3,4
Optical output power variation over the specified temperature range	ΔP_{out}	-	1	1.5	dB	4
Channel-to-channel power dispersion	DP_{out}	-	1.5	2	dB	4
Optical modulation amplitude	OMA	600	-	-	µW	4
Optical extinction ratio	E_R	7.5	9	-	dB	4
Relative Intensity Noise	RIN	-	-	-117	dB/Hz	-
Total jitter	T_J	-	-	150	ps	-
Deterministic Jitter (K28.5) @ 2.5Gbps	D_J	-	15	55	ps	-
Rise/Fall time	τ_R, τ_F	-	-	150	ps	5

Notes:

1. See Part Number construction to select fiber diameter or contact.
2. DLT-xx-251-Iw-Pyz transceivers are Class I laser products according to IEC 60825-1 standard.
3. Output optical power can be adjusted by the user through a 2-Wire serial interface.
4. Over the specified temperature range.
5. Measured at 20% / 80% levels.

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Functional block diagram

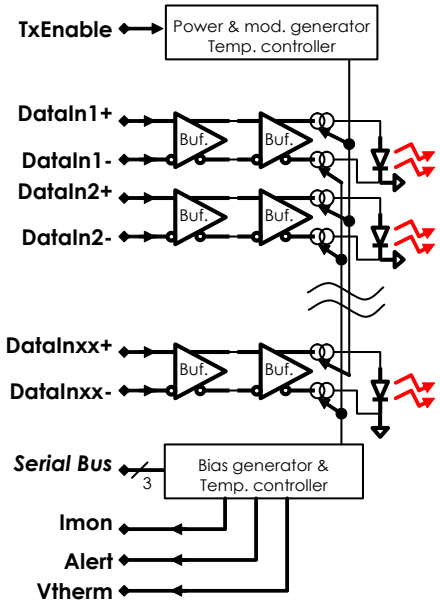

Figure 1 - DLT-xx-251-Iw-Pyz block schematics

Detailed description

General

DLT-xx-251-Iw-Pyz modules are optimized for harsh environment high speed serial links. The module is 3.3 Volts single supplied for low power consumption. The module dimensions are 16×16×3 mm in the QFN/LCC or socketed package format.

The high-speed path through the device consists of 2 to 12 replicated channels of differential-input buffer and output driver stages. The 12 channels are identical and matched such as to minimize crosstalk and inter-channel skew. The input stage is a versatile LVDS/CML compliant buffer that can be DC-coupled. The driver control circuit provides control of currents into the VCSEL and supervision of VSCEL status amongst other features. Each channel operates at up to 4.25 Gbps. The typical power consumption is 110 mW per channel.

DLT-xx-251-Iw-Pyz modules are based on high speed 850nm GaAs Vertical Cavity Surface Emitting Lasers (VCSEL) arrays and on high performance BiCMOS laser driver arrays. Each transmitter is divided in three parts: the high speed circuit compatible with data rate running from DC to 4.25 Gbps; the biasing and control circuit to control and monitor each laser according to the application; and the optical sub assembly, integrating all the opto-electronic and optical elements. Several features allow a large range of applications.

- Average and modulation currents (the same for all channels) are both temperature controlled and monitored.
- A 2-wire serial interface is implemented to control and monitor the different parameters of the transmitter.
- A AC-JTAG and boundary scan compliant interface.
- A versatile input stage allows 100 Ω differential or 50 Ω to ground termination resistors to comply with PCML or LVDS signaling levels.
- LVCMOS input compatible TxEnable commands permit low power consumption.
- Analog inputs/outputs monitor each channel state and performance.

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The module could be operated in **digital** or a **temperature compensation mode (TC)**. In the **temperature compensation mode**, the module is operated in a standalone mode and automatically compensates the temperature effects on the lasers in order to maintain module performances over the whole temperature mode. In the **digital mode**, the internal registers of the driver can be accessed and device specific values such modulation current and average current settings modified.

The DLT-xx-251-Iw-Pyz has a number of management interface options. They are the status and control pins, the JTAG memory map user register and the serial interface (Temperature compensation and Digital modes).

The definition of the status and control pins changes slightly depending on whether TC or digital mode is selected. In the temperature compensation mode, the on-chip state control logic autonomously handles the control signals and the alerts. In addition, status information can be read from the serial interface or from the user registers defined in the JTAG memory map. In the digital mode the serial interface has full control over the device including the current settings. The serial interface provides hitless read access to the internal registers. Many industry standard microcontrollers are compatible with this serial interface and can operate at 100 kHz. The serial interface is I²C™ compatible (I²C is a trademark of Phillips Corp.). The temperature sensor and monitor current outputs provide additional information to the system if necessary.

The status and control pins available include all-channel laser shutdown, VCSEL voltage alerts and voltage supply alerts. The VCSEL voltage supervisor raises an alert when the allowed operating range of the VCSEL is exceeded.

The device features AC-JTAG and boundary scan. AC-JTAG is compliant to IEEE 1149.6. This allows system users to check board level connections that are AC-coupled and supplements the DC-coupled connectivity check already available with JTAG. The JTAG port features EXTEST capability on all module interface pins, as well as ACEXTEST capability on the high-speed electrical inputs.

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Detailed description

The module is based on high speed 850nm GaAs Vertical Cavity Surface Emitting Lasers array (VCSEL) and high performance BiCMOS laser driver array. The transmitter is divided in three parts:

- The high speed circuit compatible with data rate running from DC to 4.25 Gbps,
- the biasing and control circuit to control and monitor the laser and transmitter according to the application,
- and the optical sub assembly, integrating all the opto-electronic and optical elements.

Power supply and biasing

The module is 3.3 Volts single power supply and includes internal decoupling components. Supply filtering is recommended, with roll-off frequency at 10 MHz or lower (see applications hints for details).

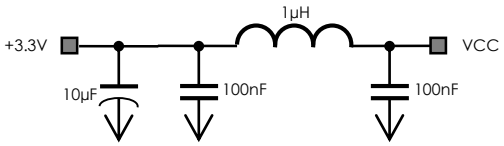

Figure 2 - Typical power supply filter

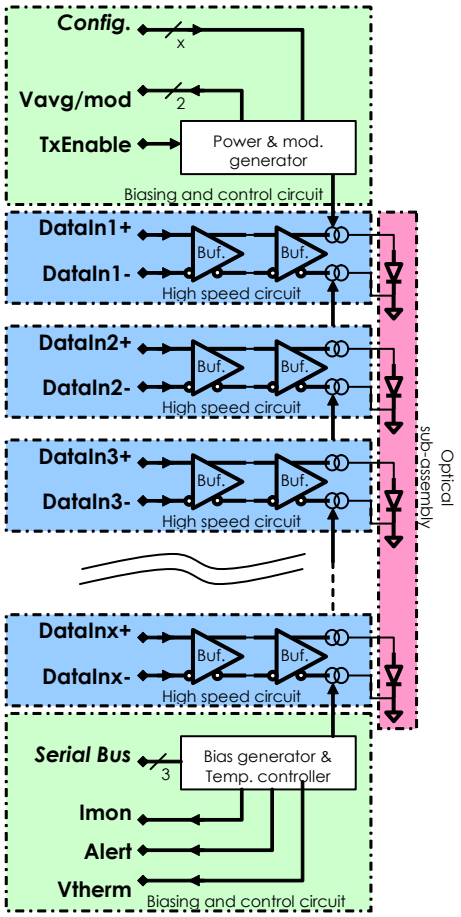

Figure 3 - Transmitter block diagram

Transmitter controls

The transmitter could be controlled or monitored by both, the serial interface (accessible in TC or Digital modes) and external I/O pins.

External IO pins:

The transmitter is provided with several input/output pins, which permit a complete monitoring of the component:

- Alert signal: provides for each laser a voltage supervisor output indicating whenever the VCSEL voltage drops below or exceeds in-fab predefined threshold voltages. The VCSEL voltage supervisor detects both a high voltage level V_{VH}, and a low voltage level V_{VL}. These two signals are processed differently:
  - **V_{VH}** is only active when transmitter is powered-up. The threshold voltage is typically 2.2V. This signal does not power down the data channel.
  - **V_{VL}** is only active when transmitter is powered-up. The threshold voltage is typically 1.3V. The V_{VL} signal provides diagnostic information.
  - V_{VH} and V_{VL} signals are OR'ed to from the ALERT output signal.

- TxEnable: the transmitter can be disabled by pulling down the TxEnable input pin. Average and modulation currents are therefore set to 0 mA and the VCSEL is shut-off.

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- IMON signal: The monitor current output is analog current output used during the manufacturing process. The current provided to this pin allows isolating the process dependency and an estimate of the modulation and average current settings can be computed. The factor of proportionality is given by the following equation:

$$I_{MON} = \frac{I_{Unit}}{2}$$

- Driver Temperature dependent voltage: this output produces a voltage proportional to the chip temperature. At a temperature of 50 °C, approximately 1.305V is present at V_{THERM}. The thermal voltage slope is given in table 1 (typ: 7.8mV/°C).

- Bias and modulation Voltage supervisors: This two pins (V_{MOD} and V_{AVG}) can be used either as output pins to monitor Bias and Voltage or input pins for external voltage controlling of the bias and modulation currents. Refer to previous section "drive current control/programming" for equations.

- Modes of drive control: The driver array can be controlled either in a temperature compensation (default mode) or digital mode. The different modes are selectable using MODE input pins.

- Serial interface: 2-wire bidirectional interface used to program average and modulation currents. See the section below for detailed description.

Serial interface controls:
The module memory mapping is accessible through the two-wire serial interface. Refer to the dedicated section for details. The memory is divided in two main parts:

- One part accessible in TC and Digital mode: providing the module status, several controls and monitor register
- The JTAG and boundary part.

Data Input stage

The input stage is a versatile differential amplifier with large common-mode range compatible with various signaling levels such as CML, LVDS or ECL/PECL. This stage is internally biased and therefore suitable for AC-coupled operations and complies with standard IEEE 1596.3 "Reduced Range Link". The input stage can be DC-coupled to reduce the number of external components. In this case the input signals shall comply with the input stage common mode (refer to Module specification - High speed electrical table).

For Differential CML : Internal bias (Vref) allows AC connection of the two incoming 50 Ω impedance lines to Dx+ and Dx-.
For Differential ECL 10k/100k/PECL : Separate load resistors are needed to draw bias current off the emitter follower outputs. And for LVDS : Internal biasing provide 100 Ω differential input impedance.
Input stage is compliant with LVDS or CML standards. The module provide on chip biasing of the inputs. On-chip termination resistors R_A allows 100 Ω differential termination or 50 Ω to ground. The input stage handles up to 10mA of input current.

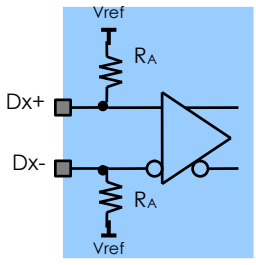

Figure 4 - Input stage

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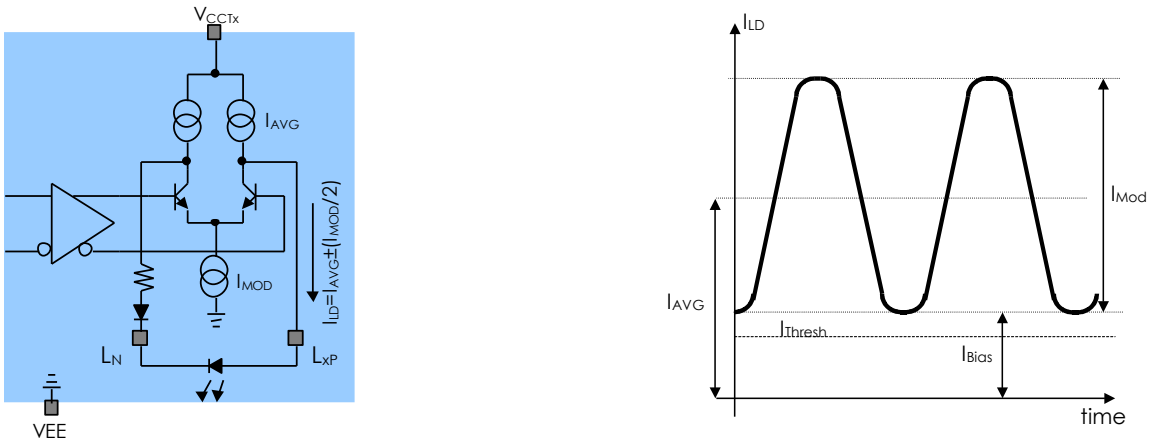
Driver stage

The current driver operates in inverted mode: it "steals" a current from the anode (p-side: Lp) of the laser. The complementary current is fed through an on-chip dummy diode to the common-n node, thus avoiding any net signal currents on the supply rails (Figure 4 - a & b).



(a) Output stage (b) Laser diode currents

Figure 5 - Output stage model

- In the logical High (True) state, the light is turned on : $I_H=I_{AVG}+I_{MOD}/2$
- In the logical Low (False) state, the light is turned off : $I_L=I_{AVG}-I_{MOD}/2$

The driver output stage is modeled by a current source and a capacitance C_{LP}. The VCSEL and its assembly are modeled by a bond-wire inductance L_L a series resistance r_s and an extrinsic capacitance C_{Ext}. See application notes for more information on the equivalent circuit.

Drive Current Control/Programming

DLT-xx-251-Iw-Pyz-Lvv devices could be operated in two modes:

- In the **temperature compensation mode**, the module is operated in a standalone mode and automatically compensates the temperature effects on the lasers in order to maintain module performances over the whole temperature mode.
- In the **digital mode**, the internal registers of the driver can be accessed and device specific values such modulation current and average current settings modified.

Theses modes are selectable through the **Mode** pin according the following table:

Mode pin voltage	Operating Mode	Description
GND	Digital mode	In the **Digital mode**, the automatic temperature compensation mode is disabled. The average and modulation current settings are defined through the serial interface by the state of the laser driver average and modulation registers (see memory organisation for details). Note that driver memory is a volatile memory space.
VCC	Temperature compensation mode (normal usage)	In the **Temperature compensation mode**, the module performances are automatically controlled to maintain average optical power and extinction ratio constant over temperature variation. In this mode the memory space allocable is in Table 0h and 1h. Modulation and bias currents are accessible through the serial interface. This mode is the normal mode of operations.

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In the **temperature compensation mode**, average and modulation current levels are globally set for all channels. They are internally set by programming R_{AVG} and R_{MOD} *(Figure 5)*. In normal operating conditions the V_{AVG} and V_{MOD} voltages are controlled/programmed using two digital potentiometers which can be addressed by means of a 2-wire serial interface (See the following section for further details on the 2-wire serial interface modes and operations).

Non-volatile Look-Up Table (LUT) with in-fabric programmed parameters are used to save and monitor the VCSEL current and voltage behavior over the functional temperature range. This specific design allows the optical power of the module to remain within 1.5dB optical power variation over the functional temperature range.

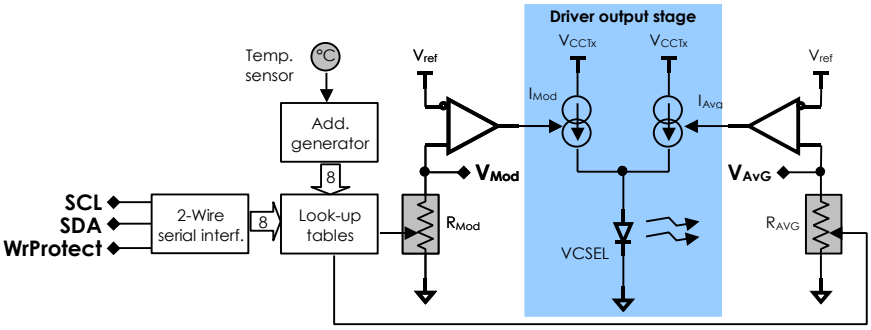

Figure 6 - Average and modulation current control circuit

The V_{MOD} and V_{AVG} voltages can be modified by the user to adapt the output optical power according to the applications requirements.

Laser currents are defined by the following equations:

$$I_{AVG} = N_{AVG} \cdot \frac{2 \cdot V_{REF}}{R_{AVG}} \quad \text{and} \quad I_{MOD} = N_{MOD} \cdot \frac{2 \cdot V_{REF\ mod}}{R_{MOD}}$$

R_{AVG} and R_{MOD} are the digital potentiometers equivalent value: $\boldsymbol{R_x=39.21x(Value_x)d}$, where $Value_x$ is the register value in decimal for average current or modulation. See table 1 for parameters values.

Parameter	Symbol	Min.	Typ.	Max.
Unit current	I_{unit}	-25%	1.10mA	+25%
Uniformity range		-	-	10%
Current control Reference Voltage	V_{REF}	-	1.188V	-
N_{AVG} Factor	N_{AVG}	-	8	-
N_{MOD} Factor	N_{MOD}	-	8	-
Thermal voltage slope	δV_{THERM}	-	7.8 mV/°C	-
Thermal voltage @ 50°C	V_{THERM}(50°C)	-	1.305V	-

Table 1 – Transceiver Internal gain and parameters for average and modulation programming

An **over temperature compensation mode (CCM pin)** has been implemented to boost the modulation current at high temperature. This mode could be used to increase optical performances at temperature higher than 80°C. Note that increasing the current in the laser could affect the module lifetime.

In the **Digital mode**, average and modulation current levels are programmed by the user through the serial interface mode. Refer to the memory mapping section for details. The internal unit current I_{UNIT} is generated with an on chip resistance R_{INT}. Fabrication tolerances and drift numbers are specified in the previous table. The serial interface allows each of the average and modulation currents of each of the 12 channels to be set individually. The following equations show the weighting of the different bits on the total current. A 6-bit linear DAC is converts the register setting into VCSEL average and modulation current as shown below: the average current has a multiplication factor of N_{AVG}; the modulation current of N_{MOD}.

The monitor current (Imon) provides an accurate process independent estimate of the average and modulation current.

In the digital mode, each channel could be programmed independently to a specific polarization point according to the following equations:

$$I_{AVG}^{X} = N_{AVG} \cdot I_{UNIT} \frac{(REG_{AVG})_d}{48} \quad \text{and} \quad I_{MOD}^{X} = N_{MOD} \cdot I_{UNIT} \frac{(REG_{MOD})_d}{48}$$

Where I^x is the current (modulation or average) the channel number X and $(REG_{AVG})_d$ or $(REG_{MOD})_d$ the decimal value of the average/modulation current register for channel X.

During link operation, the drive current settings may only be adjusted in single steps. Small steps will prevent jolts on the power supply and the link will remain error free. If the jolt is very large, a Power on Reset may occur. Note that in the digital mode data are not retained after a power Off/On cycle.

Power supply noise rejection

Even though bypass capacitors are integrated inside the module, additional filtering can reduce the noise penalty above 10 MHz. For a supply noise V_{PSN} = 100 mV_{PP} a 0.5 dB sensitivity penalty can be reached over the whole frequency range by using a first order low-pass filter with f_c=10 MHz on the power supply (See application note for additional information).

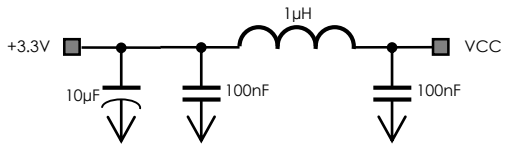

Figure 7 - Typical power supply filter

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Memory Mapping

The module memory is mapped in three separate memory area: The controller memory, the Driver memory and the JTAG memory. The two first memories are accessible through a common 2-wire serial interface with two independent clocks. The following figure details the module memory organization.

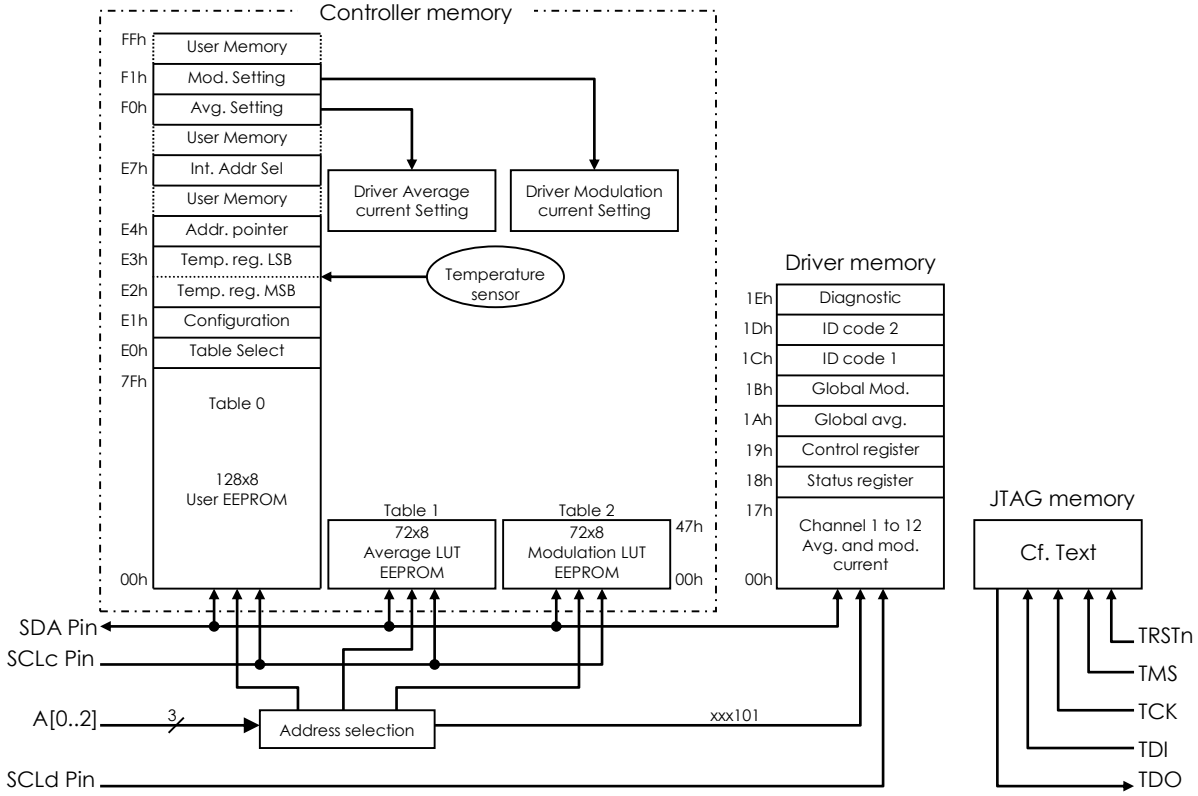

Figure 8 - DLT-xx-251-Ix memory organization

Temperature conversion

The direct-to-digital temperature sensor measures temperature through the use of an on-chip temperature measurement technique with and operating range from -40°C to + 95°C. Temperature conversions are initiated upon-power-up, and the most recent result is stored in address location (E2)h and (E3)h, which are updated every 10ms. Temperature conversion will not occur during an active read or write to main memory. The value of each current source is determined by the temperature-addressed look-up table (LUT) that assigns a unique value to each current source for every 2°C increment with a 1°C hysteresis at a temperature transition over the operating temp. range.

To calculate the value of the temperature, treat the two's complement value binary number as an unsigned binary number, then convert to decimal and divide by 256. If the result is greater than or equal to 128, then subtract 256 from the result.

Temperature bit weights

S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}

Temperature:
High byte: -128°C to +127°C signed;
Low byte: 1/256°C.

Temperature conversion examples

MSB (BIN)	LSB (BIN)	Temperature (°C)
01000000	00000000	64
01000000	00001111	64.059
01011111	00000000	95
11110110	00000000	-10

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Controller memory and register description (main memory area)

The main module memory is the controller memory area.

Controller memory - Table 0

Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
00 to 7F	EEPROM	R/W	00	User Memory	This block is for general purpose user memory. To access this memory space, the Table Select Byte (E0)h must be set to (00)h.
E0	EEPROM	R/W	00	Table select Byte	Writing this byte determines if one of the two 72x8 EEPROM LUTs of the user EEPROM memory is selected for reading or writing. Write (00)h to access the user memory, (01)h for the average LUT and (02)h for modulation LUT.
E1	EEPROM	R/W	03	Configuration byte	The three last bit of the configuration byte are used to control the configuration of the device. 7 … 0 00000 | TAU | TEN | AEN **TAU (bit 2):** Temperature address Update becomes a 1 after a temperature and address update has occurred as a result of a temperature conversion. The user can write this bit to 0 and check for a transition from 0 to 1 in order to verify a conversion has occurred. **TEN (bit1):** Temperature Update Enable. When set to 0 the temperature conversion feature is disabled. The user sets the average and modulation current in "manual mode" by writing to addresses (F0)h and (F1)h respectively. **AEN (bit 0):** Address Update Enable. When this bit is set to 0, the user can operate in a test mode. Address updates made from the temperature sensor will cease. The user can load a memory location into (E4)h and verify that the values in locations (F0)h and (F1)h are the expected ones.
E2	EEPROM	R/W	-	Temperature MSB	This byte contains the MSB of the 13 bit 2s complement temperature output from the temperature sensor.
E3	EEPROM	R/W	-	Temperature LSB	This byte contains the LSB of the 13 bit 2s complement temperature output from the temperature sensor.
E4	EEPROM	R	-	Address pointer	Derivated from the temperature sensor, this register contain the pointing address to the LUT.
E5 to E6	SRAM	R/W	-	User memory	General purpose user memory
E7	EEPROM	R/W	-	Address select	Internal or external device address select register. This byte allows the

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					user to use the external address pins or an internal register location to determine the main memory device address. 7 … 0 XXXX | A0 | A1 | A0 | ENBn When ENB=0 and external A2, A1 and A0 grounded, the device will respond to the internal address bits (A2,A1, A0) in this register. When ENB=1, the device will respond to the address set by the external A2, A1 and A0 pins.
E8 to EF	SRAM	R/W	-	User memory	General purpose user memory
F0	SRAM	R/W	-	Average current	Average current setting for the current temperature.
F1	SRAM	R/W	-	Modulation current	Modulation current setting for the current temperature.
F2 to FF	SRAM	R/W	-	User memory	General purpose user memory

Table (1)h and (2)h corresponds respectively to the LUT tables for setting the average and the modulation currents accordingly of the change in temperature. Address offset (00)h corresponds to -40°C and (44)h correspond to +95°C. Memory location (44-47)h, which cover the temperature range (+96° to 102°C), are outside of the specified operating temperature range [-40;+95°C]. However, the values stored in these locations will act as valid current settings if the temperature exceeds +95°C.

Driver memory and register description (main memory area)

The driver memory is accessible only in R/W only for the digital mode. To access the driver memory, connect the serial clock signal to SCLd pin. The driver memory responds only to address (xxxxx101)b.

Driver memory

Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
00	SRAM	R/W	00	Channel #1 Average Current Register	This register controls the channel 1 average current in the digital mode. 7 … 0 Res | V_{VL} | A5 | A4 | A3 | A2 | A1 | A0 Res. : Reserved V_{VL} is a read only bit. This bit is high indicates that a VCSEL voltage underflow as occurred for channel #1.
01	SRAM	R/W	00	Channel #1 Modulation Current Register	This register controls the channel 1 modulation current in the digital mode. 7 … 0 Res | V_{VH} | M5 | M4 | M3 | M2 | M1 | M0 Res. : Reserved V_{VH} Is a Read Only bit. This bit is high indicates that a VCSEL voltage overflow as occurred for channel #1.
02	SRAM	R/W	00	Channel #2 Average Current Register	This register controls the channel 2 average current in the digital mode. Cf. channel #1 description.
03	SRAM	R/W	00	Channel #2 Modulation Current Register	This register controls the channel 2 modulation current in the digital mode. Cf. channel #1 description.

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04	SRAM	R/W	00	Channel #3 Average Current Register	This register controls the channel 3 average current in the digital mode. Cf. channel #1 description.
05	SRAM	R/W	00	Channel #3 Modulation Current Register	This register controls the channel 3 modulation current in the digital mode. Cf. channel #1 description.
06	SRAM	R/W	00	Channel #4 Average Current Register	This register controls the channel 4 average current in the digital mode. Cf. channel #1 description.
07	SRAM	R/W	00	Channel #4 Modulation Current Register	This register controls the channel 4 modulation current in the digital mode. Cf. channel #1 description.
08	SRAM	R/W	00	Channel #5 Average Current Register	This register controls the channel 5 average current in the digital mode. Cf. channel #1 description.
09	SRAM	R/W	00	Channel #5 Modulation Current Register	This register controls the channel 5 modulation current in the digital mode. Cf. channel #1 description.
0A	SRAM	R/W	00	Channel #6 Average Current Register	This register controls the channel 6 average current in the digital mode. Cf. channel #1 description.
0B	SRAM	R/W	00	Channel #6 Modulation Current Register	This register controls the channel 6 modulation current in the digital mode. Cf. channel #1 description.
0C	SRAM	R/W	00	Channel #7 Average Current Register	This register controls the channel 7 average current in the digital mode. Cf. channel #1 description.
0D	SRAM	R/W	00	Channel #7 Modulation Current Register	This register controls the channel 7 modulation current in the digital mode. Cf. channel #1 description.
0E	SRAM	R/W	00	Channel #8 Average Current Register	This register controls the channel 8 average current in the digital mode. Cf. channel #1 description.
0F	SRAM	R/W	00	Channel #8 Modulation Current Register	This register controls the channel 8 modulation current in the digital mode. Cf. channel #1 description.
10	SRAM	R/W	00	Channel #9 Average Current Register	This register controls the channel 9 average current in the digital mode. Cf. channel #1 description.
11	SRAM	R/W	00	Channel #9 Modulation Current Register	This register controls the channel 9 modulation current in the digital mode. Cf. channel #1 description.
12	SRAM	R/W	00	Channel #10 Average Current Register	This register controls the channel 10 average current in the digital mode. Cf. channel #1 description.
13	SRAM	R/W	00	Channel #10 Modulation Current Register	This register controls the channel 10 modulation current in the digital mode. Cf. channel #1 description.
14	SRAM	R/W	00	Channel #11 Average Current Register	This register controls the channel 11 average current in the digital mode. Cf. channel #1 description.
15	SRAM	R/W	00	Channel #11 Modulation Current Register	This register controls the channel 11 modulation current in the digital mode. Cf. channel #1 description.
16	SRAM	R/W	00	Channel #12 Average Current Register	This register controls the channel 12 average current in the digital mode. Cf. channel #1 description.
17	SRAM	R/W	00	Channel #12 Modulation Current Register	This register controls the channel 12 modulation current in the digital mode. Cf. channel #1 description.
18	**SRAM**	**R**	**-**	**Status Register**	**-**

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Bit 7	-	R	0	Reserved	Reserved
Bit 6	-	R	N/A	TxEnable	This bit indicates the status of the TxEnable PIN.
Bit 5	-	R	1	Reserved	Reserved
Bit 4	-	R	1	Reserved	Reserved
Bit 3	-	R	N/A	Supply High	This bit indicates that the supply supervisor has detected that the upper limit of the supply voltage has been exceeded (3.7V).
Bit 2	-	R	N/A	Supply Low	This bit indicates that the supply supervisor has detected that the supply voltage has dropped below the lower limit (2.8V).
Bit 1	-	R	N/A	nV_{VH}	The Not VVH global bit goes low to indicate that the voltage of one of the VCSEL has exceeded the upper threshold (2.3V).
Bit 0	-	R	N/A	nV_{VL}	The Not VVH global bit goes low to indicate that the voltage of one of the VCSEL has gone below the lower threshold (2.3V).

19	**SRAM**	**R/W**	**00**	**Control Register**	**-**
Bit 7	-	R/W	0	nInc	When cleared the Not Increment bit will cause the sub-address register to increment after read and write operations. When the bit is set, the sub address register will not increment after read or write operations.
Bit 6	-	R	0	Reserved	Reserved
Bit 5	-	R	0	Reserved	Reserved
Bit 4	-	R	0	Reserved	Reserved
Bit 3	-	R	0	Reserved	Reserved
Bit 2	-	R/W	0	Status Bit	Not used
Bit 1	-	R/W	0	Disable	This bit is used to disable all lasers drivers in the digital mode. This signal disables only the output stages.
Bit 0	-	R/W	0	Alert	This bit controls the nAlert pin (not alert). When this bit is set, nAlert pin is driven low. When this bit is cleared, nAlert pin reports any other alerts that may be active at the time.

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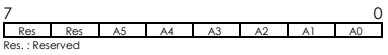
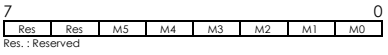
Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
1A	SRAM	W	N/A	Global Average Current Register	This register controls the global average current in the digital mode.  Res. : Reserved By setting this global instruction, the average current registers of all channels are set to the same value. Refer to Average Current Settings for the exact details of the operation. The values in the individual channel average registers are overwritten with this value. This byte is "write only". Software readback of channel of registers must be performed one channel at a time.
1B	SRAM	W	N/A	Global Modulation Current Register	This register controls the global modulation current in the digital mode.  Res. : Reserved By setting this global instruction, the modulation current registers of all channels are set to the same value. The values in the individual channel modulation registers are overwritten with this value. Refer to Modulation Current Settings for details. This byte is "write only". The values in the individual channel average registers are overwritten with this value. Software readback of channel of registers must be performed one channel at a time.
1C	EEPROM	R/W	5F	ID CODE 1 Register	This two registers contains the 11 bits ID code for the vendor. Default value is (015F)h. ID code 1 is the less significant bits.
1D	EEPROM	R/W	01	ID CODE 2 Register	
1E	SRAM	R	0x	Diagnostic Register	This register controls the global modulation current in the digital mode.  Res. : Reserved sX bits correspond to a short circuit condition for Average (sA) and Modulation (sM). fX bits corresponds to a open circuit condition for Average (fA) and Modulation (fM). This register provides extra diagnostics monitor to identify module failure.

Average and Modulation Current Settings in "Digital Mode"

The average and modulation currents could be independently set for each channel through the appropriate registers [00-17]h. The six bit register A5 to A0 for average and M5 to M0 for modulation are used to program the 6-bit linear digital to analog converter to set the VCSEL average and modulation current according the following equations:

$$I_{AVGx} = N_{AVG} \cdot I_{UNIT} \cdot \frac{(32 \cdot A5 + 16 \cdot A4 + 8 \cdot A3 + 4 \cdot A2 + 2 \cdot A1 + A0)}{48}$$

for average current of channel #x

$$I_{MODx} = N_{MOD} \cdot I_{UNIT} \cdot \frac{(32 \cdot M5 + 16 \cdot M4 + 8 \cdot M3 + 4 \cdot M2 + 2 \cdot M1 + M0)}{48}$$

for modulation current of channel #x

When the device is in Temperature Compensation mode, the Average and modulation current registers are read-only, resulting in a logical high in the A5 to A0 and M5 to M0 bits.

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2-Wire data transfer operation

The 2-wire serial port interface supports a bi-directional data transmission protocol with device addressing (Default address is 000). A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DLT-xx-251-Iw-Pyz module operates as a slave on the 2-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCLc or SCLd. Timing diagrams for the 2-wire serial port can be found in Figures "2-wire data transfer protocol" and "2-wire data transfer protocol". Timing information for the 2-wire serial port is provided in the following table.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line from HIGH to LOW while the clock is HIGH defines a START condition.

Stop data transfer: A change in the state of the data line from LOW to HIGH while the clock line is HIGH defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line can be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Figures 12 and 13 detail how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. Within the bus specifications a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The SLM module works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the SLM module slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

1. Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the command/control byte. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the command/control byte) to the slave. The slave then returns an acknowledge bit. Next, follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' can be returned.

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The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DLT-xx-251-Iw-Pyz module may operate in the following two modes:

1. Slave receiver mode: Serial data and clock are received through SDA and SCLc or SCLd, respectively. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave (device) address (default address is 000) and direction bit. Slave transmitter mode: The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DLT module, while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.
2. Slave Address: Command/control byte is the first byte received following the START condition from the master device. The command/control byte consists of a 4-bit control code. For the SLM module, this is set as ***1010*** binary for read/write operations. The next 3 bits of the command/ control byte are the device select bits or slave address (Default address is 000). When reading or writing the SLM module, the device-select bits must match the device-select pins (In-fab predefined to A2=0, A1=0, A0=0). The last bit of the command/control byte (R/W) defines the operation to be performed. When set to a 1, a read operation is selected, and when set to a 0, a write operation is selected.

Following the START condition, the DLT module monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the ***1010*** control code, the appropriate device address bits (default address is 000), and the read/write bit, the slave device outputs an acknowledge signal on the SDA line.

Module Address Presets

The modules are delivered with in-fab predefined device addresses:

- Main memory (controller): the device is responding to the address defined by the address pin A2, A1 and A0 value or by the internal address register. See the main memory description for detail.
- The driver memory is programmed to respond to address $(101)_b$ or $(05)_h$. Contact sales for address modifications or further information.

Write Protect

The write-protect input pin (WP) protects all memory (including EEPROM), control registers, and lookup tables from alteration in an application. However, this does not interfere with internal temperature/resistor updates. If set to a logic 0, the device is not write protected and can be written to via the 2-wire interface. This pin has an internal pull-up resistor.

Note: the I2C interface could not be use in conjunction with the JTAG interface. Disable JTAG before using the I2C by pulling low the TRSTn pin.

2-Wire data transfer protocol and chronograms

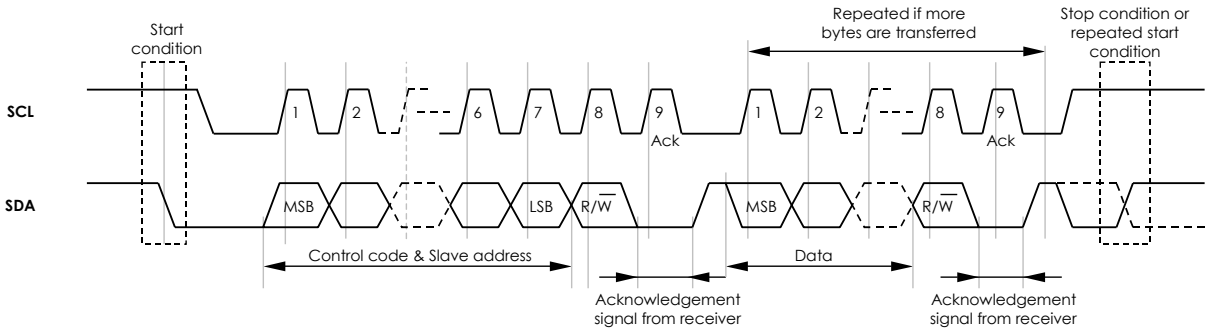

Figure 9 - 2-wire data transfer chronograms

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2-Wire AC Characteristics and timing

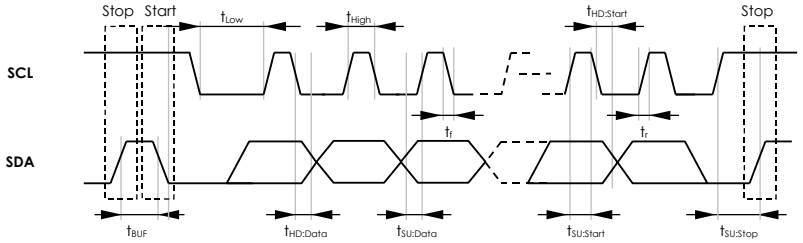

Figure 10 - 2-wire data transfer chronograms

Timing table (-40°C to +85°C, V_{CC} = 3.3V)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
Serial clock frequency	F_{SCL}	Fast mode	0	400	kHz	1
		Standard mode	0	100		
Bus free time between STOP and START	t_{BUF}	Fast mode	1.3	-	µs	1
		Standard mode	4.7	-		
Hold time for START condition	$t_{HD:Start}$	Fast mode	0.6	-	µs	1,2
		Standard mode	4.0	-		
Low period of SCL clock	t_{Low}	Fast mode	1.3	-	µs	1
		Standard mode	4.7	-		
High period of SCL clock	t_{High}	Fast mode	0.6	-	µs	1
		Standard mode	4.0	-		
Data set-up time	$t_{SU:Data}$	Fast mode	0	0.9	µs	1
		Standard mode	0	0.9		
Data hold time	$t_{HD:Data}$	Fast mode	0	0.9	µs	1,3,4
		Standard mode	0	0.9		
Set-up time for STOP and START conditions	$t_{SU:Stop}$	Fast mode	0.6	-	µs	1
		Standard mode	4.0	-		
Rise time	t_r	Fast mode	80	300	ns	-
		Standard mode	100	1000		
Fall time	t_f	Fast mode	80	300	ns	-
		Standard mode	100	1000		
EEPROM write time	t_w	-	5	20	ms	5

Notes:

1. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT}$ > 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{RMAX} + $t_{SU:DAT}$ = 1000ns + 250ns = 1250ns before the SCL line is released.
2. After this period, the first clock pulse is generated.
3. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
5. EEPROM write begins after a STOP condition occurs.

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JTAG and Boundary Scan Definition

The DLT-xx-251-lw-Pyz contains the following items, which meet the requirements, set by the IEEE-1149.1 standard Test Access Port and Boundary Scan Architecture, the IEEE 1149.6 Standard for Boundary-Scan Testing of Advanced Digital Networks as well as the AC boundary-scan Specification for IEEE from Cisco:

- Test Access Port (TAP)
- TAP Controller
- Instruction Register (3 Bit)
- Bypass Register (1 Bit)
- Boundary Scan Register (16 Bit)
- Device Identification Register (32 Bit)
- User Data Register (32 Bit)
- Certified 'AC Boundary Scan' as licensed from Cisco Systems, Inc.

Details on Boundary Scan Architecture and the Test Access Port can be found in IEEE 1149.1-2001, IEEE 1149.6-2003 and AC boundary-scan Specification for IEEE from Cisco (EDCS-134568 Rev B5, www.acextest.org).

Instruction Codes for the module Boundary Scan Architecture

Instruction	Selected Register	Instruction Codes
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
AC_EXTEST	AC Boundary Scan	100
SAMPLE/PRELOAD	Boundary Scan	010
IDCODE	Device Identification	001
SEL_INIT_SCAN	User Data Register	011
EXTEST_PULSE	AC Boundary Scan	101
EXTEST_TRAIN	AC Boundary Scan	110

Device Identification Register (32 Bits)

MSB LSB

31																															0
Version (4 Bits)				**Part Number (16 Bits)**																**Manufacturer Identity (11 Bits)**											**Fixed**
0001				000000 0000000110																00101011111											1

Boundary Scan Register (16 Bits)

This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells and is 16 bits in length. The table below shows all cell bit locations and definitions.

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RUN	nAlert	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	nStart	LDIS
In	Out	In	In	In	In	In	In	In	In	In	In	In	In	In	In
BC_4	BC_2	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	BC_4	BC_4
No AC	No AC	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	No AC	No AC

Notes:

BC_4: Observe only registers, BC_2: Control and observe registers, HEX_BC4_DIFF: AC Observe only registers

User Data Register (16 Bit)

This register contains a shift register path for different control signals and is 32 bits in length. The table below shows all signals connected to the user data register.

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Sup. H	Sup. L	nVvh	nVvl	sAVG	sMOD	fAVG	fMOD	Status	Res.	LDIS	Alert
Read	Read	Read	Read	Read	Read	Read	Read	Read	Read	Read	Read	Read	Read	Read	Read

Notes:

Res. : Reserved bit (Logical low), Sup.: Power supply monitor (H: High, L: Low), sXXX: Shorted XXX Pin, fXXX: Floating XXX Pin nXXX: inverted XXX value

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Channels distribution over the fiber and pigtail length

The following table shows the channel distribution over the 12 fiber ribbon configuration.

Fiber number	1	2	3	4	5	6	7	8	9	10	11	12
Color code	Aqua	Pink	Violet	Yellow	Black	Red	White	Grey	Brown	Green	Orange	Blue
DLT-02-251-...						Tx1	Tx2					
DLT-04-251-...					Tx1	Tx2	Tx3	Tx4				
DLT-08-251-...[1]			Tx1	Tx2	Tx3	Tx4	Tx5	Tx6	Tx7	Tx8		
DLT-12-251-...	Tx1	Tx2	Tx3	Tx4	Tx5	Tx6	Tx7	Tx8	Tx9	Tx10	Tx11	Tx12

Note:
1. DLT-08-251-Ix-Py1-Lvv or DLT-08-251-Ix-Py2-Lvv 8 channel devices are based on 12 channels devices with 4 channels disabled.

According to the previous table, the module pin is following the same distribution (pins are for IGM package option):

1. For a 2 channels transmitter having a fiber ribbon pigtail (DLT-02-251-Ix-Py1-Lvv or DLT-02-251-Ix-Py2-Lvv), the electrical input data will be distributed as stated on the table: channel #1 positive input is connected to D3+ (Pin A8) and negative input to D3- (Pin B8), channel #2 positive input is connected to D10+ (Pin B3) and negative input to D10- (Pin A3).
2. For a 4 channels transmitter having a fiber ribbon pigtail (DLT-04-251-Ix-Py1-Lvv or DLT-04-251-Ix-Py2-Lvv), the electrical input data will be distributed as stated on the table: channel #1 positive input is connected to D3+ (Pin A8) and negative input to D3- (Pin B8), channel #2 positive input is connected to D5+ (Pin A6) and negative input to D5- (Pin A5), channel #3 positive input is connected to D6+ (Pin B6) and negative input to D6- (Pin B5), channel #4 positive input is connected to D10+ (Pin B3) and negative input to D10- (Pin A3).
3. Same for 8 channels device.

Other Pin-out could be proposed under customer requirements.

The following table provides the pigtail length precision per length

Pigtail length (cm)	Standard Dimensions		Tight Tolerances (T option)	
	Tolerances	Resolution	Tolerances	Resolution
5 to 50	+/-15mm	10mm	+/-5mm	1mm
50 to 100	+/-20mm	15mm	+/-10mm	5mm
Above 100	+/-2%	15mm	Not Available	10mm

For Tight tolerances add "T" in the part number at the end of the "-Lvv" section followed by the millimeter value: "-LvvTw" for a length of vv.w cm. For example a transmitter with a pigtail of 12.3cm length will have the P/N: **DLT-12-251-Ix-Pyz-L12T3.**

Temperature and Mechanical Qualifications

D-Lightsys modules fully complies with the following Aeronautic/harsh environment standards:

- ARINC804, extended operation range,
- MIL-STD-883e (as specified with ARINC804),
- DO-160 (as specified with ARINC804).

Refer to the ARINC804, MIL-STD-883e and DO-160 standards for further details on the qualifications.
Note that the vibrations and shocks qualification results are related to the optical termini and package selected. Selecting a non-environmental qualified optical termini and/or packaging will limit the module environmental performances. Contact sales for details or recommended package/optical termini.

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Pin out description (Pin number corresponding 12 channel device with IGM package)

Signal	Pin number		Type	Description
	IGM	LCC		
DataIn1+ or D1+	E10	31	HS[1] Input	**Positive Data input for channel 1:** LVDS/CML positive high speed input
DataIn1- or D1-	D10	32	HS[1] Input	**Negative Data input for channel 1:** LVDS/CML negative high speed input
DataIn2+ or D2+	B10	33	HS[1] Input	**Positive Data input for channel 2:** LVDS/CML positive high speed input
DataIn2- or D2-	A10	34	HS[1] Input	**Negative Data input for channel 2:** LVDS/CML negative high speed input
DataIn3+ or D3+	A8	35	HS[1] Input	**Positive Data input for channel 3:** LVDS/CML positive high speed input
DataIn3- or D3-	B8	36	HS[1] Input	**Negative Data input for channel 3:** LVDS/CML negative high speed input
DataIn4+ or D4+	D8	37	HS[1] Input	**Positive Data input for channel 4:** LVDS/CML positive high speed input
DataIn4- or D4-	E8	38	HS[1] Input	**Negative Data input for channel 4:** LVDS/CML negative high speed input
DataIn5+ or D5+	A6	39	HS[1] Input	**Positive Data input for channel 5:** LVDS/CML positive high speed input
DataIn5- or D5-	A5	40	HS[1] Input	**Negative Data input for channel 5:** LVDS/CML negative high speed input
DataIn6+ or D6+	C6	41	HS[1] Input	**Positive Data input for channel 6:** LVDS/CML positive high speed input
DataIn6- or D6-	C5	42	HS[1] Input	**Negative Data input for channel 6:** LVDS/CML negative high speed input
DataIn7+ or D7+	E6	43	HS[1] Input	**Positive Data input for channel 7:** LVDS/CML positive high speed input
DataIn7- or D7-	E5	44	HS[1] Input	**Negative Data input for channel 7:** LVDS/CML negative high speed input
DataIn8+ or D8+	G6	45	HS[1] Input	**Positive Data input for channel 8:** LVDS/CML positive high speed input
DataIn8- or D8-	G5	46	HS[1] Input	**Negative Data input for channel 8:** LVDS/CML negative high speed input
DataIn9+ or D9+	E3	47	HS[1] Input	**Positive Data input for channel 9:** LVDS/CML positive high speed input
DataIn9- or D9-	D3	48	HS[1] Input	**Negative Data input for channel 9:** LVDS/CML negative high speed input
DataIn10+ or D10+	B3	1	HS[1] Input	**Positive Data input for channel 10:** LVDS/CML positive high speed input
DataIn10- or D10-	A3	2	HS[1] Input	**Negative Data input for channel 10:** LVDS/CML negative high speed input
DataIn11+ or D11+	A1	3	HS[1] Input	**Positive Data input for channel 11:** LVDS/CML positive high speed input
DataIn11- or D11-	B1	4	HS[1] Input	**Negative Data input for channel 11:** LVDS/CML negative high speed input

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DataIn12+ or D12+	D1	5	HS[1] Input	**Positive Data input for channel 12:** LVDS/CML positive high speed input
DataIn12- or D12-	E1	6	HS[1] Input	**Negative Data input for channel 12:** LVDS/CML negative high speed input
TxEnable	K1	13	Digital Input	**Transmitter Enable:** Enable the module (set to 1)
Imon	J2	15	Analog output	**VCSEL Current monitor:** An analog current flows from this pin proportional to the sum of the average current delivered to the VCSELs.. *See detailed characteristics for $N_{Avg.}$ value.*
VAVG	H9	26	Analog output	**VCSEL Average Voltage monitor:** An analog voltage proportional the VCSEL average current is provided to this pin.
VMOD	H2	25	Analog output	**VCSEL Modulation Voltage monitor:** An analog voltage proportional the VCSEL modulation current is provided to this pin.
Alert	H1	12	Digital Output (Open Drain)	**VCSEL Voltage supervisor:** This pin provides a digital output high when VCSEL voltage is below or above predefined voltage limits. This output could be use to provide an "End-of-life" information of the VCSEL.
Vtherm	J9	-	Analog output	**Driver temperature:** This analog output provides a voltage proportional to driver temperature.
CCM	K2	14	Digital input	**Over temperature Current Compensation Mode:** This pin is used to add extra-current at high temperature. When pulled high an extra amount of current is added to the programmed polarization point. In normal condition of operation this pin should be left open (internal pull-down).
Mode	J1	11	Digital Input	**Temperature compensation Mode selection:** The Mode pin selects between the temperature compensation and the digital mode of operation. When Mode is pulled up (tied to VCC), the module operate in the temperature compensation mode (normal mode of operation). When low the module is in digital mode. ***This pin should be pulled up for normal operation.***
SCLc	K10	24	Digital Input	**2-Wire Controller Serial Clock input:** The serial clock input is used to clock data (SDA pin) into the module controller memory on rising edges and clock data out on falling edges. Connected to GND not used.
SCLd	K9	-	Digital Input	**2-Wire Driver Serial Clock input:** The serial clock input is used to clock data (SDA pin) into the module driver memory (This clock should be different from SCLc if controller responding address is set to 101_b). Otherwise SCLc and SCLd could be connected together. Connected to GND not used.
SDA	J10	23	Digital In/output (Open Drain)	**2-Wire serial data interface:** The serial data pin is for serial data transfer to and from the module. The pin is open drain and may be wire-ORed with other open drain or open collector interfaces. Connected to GND not used.

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WP	H10	22	Digital Input	**Write protect:** If open or set to logic 1, all memory, control registers, and Look-up tables are write protected. If set to a logic 0, the device is not write protected and can be written to. The WP pin is pulled high internally.
A0	J7	-	Digital Input	**Module Serial Interface Address Bit 0:** Serial interface address Bit 0. See text for detail.
A1	J8	-	Digital Input	**Module Serial Interface Address Bit 1:** Serial interface address Bit 1. See text for detail.
A2	K8	-	Digital Input	**Module Serial Interface Address Bit 2:** Serial interface address Bit 2. See text for detail.
TDI	J5	-	JTAG Input	**Test Data Input:** TDI signal carries test data into the device via the IEEE P1149.1 test access port. TDI is sampled on rising edge of TCK. TDI has an integrated pull-up.
TDO	J6	-	JTAG Output	**Test Data Output:** TDO signal carries test data out of the device via the IEEE P1149.1 test access port. TDO is updated on falling edge of TCK. TDO is a tri-state out that is inactive except when scanning of data in progress.
TCK	K5	-	JTAG Input	**Test Clock:** TCK signal provides timing for the test operations that are carried out using the IEEE P1149.1 test access port. When this pin is not used, an external pull down is recommended.
TMS	K6	-	JTAG Input	**Test Mode Select:** TMS signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integrated pull-up.
TRSTn	K7	-	JTAG Input	**Active Low Test Reset:** TRSTn signal provides an asynchronous test access port reset via the IEEE P1149.1 test access port. TRSTn must be pulled low during normal device operation. This place the JTAG logic into the reset state.
V_{CC1}	G1,G2, G9,G10	8	Power	**Positive supply rail for digital parts:** +3.3Volts positive power supply for the transmitter.
V_{CC2}	G3,H3, G8,H8	9	Power	**Positive supply rail for the driver stage:** +3.3Volts positive power supply for the transmitter.
GND	A2,A4,A7,A9, B2,B4,B7,B9, C1-C4, C7-C10, D2, D4-D7,D9, E2,E4,E7,E9, F1-F10,G4,G7, H4-H7	7,10, 16-21, 27,30	Power	**Negative supply rail:** negative power supply tied to GND (0 Volt) for the transmitter.
NC	J3,J4,K3 ,K4	-	-	**Not connected Input Pins:** Do not connect those pins. For manufacturing test purpose only.

Notes: [1]: HS pin type: High Speed inputs CML/LVDS compatible input pins.

[2]: Tri-state input pin allows three input voltage: High, Medium (not connected) and Low operations.

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2 to 12 channels 4.25 Gbps optoelectronic transmitter

Meg-Array Package Pin Layout (DLT-xx-25x-IGM-Pyz-Lvv Option)

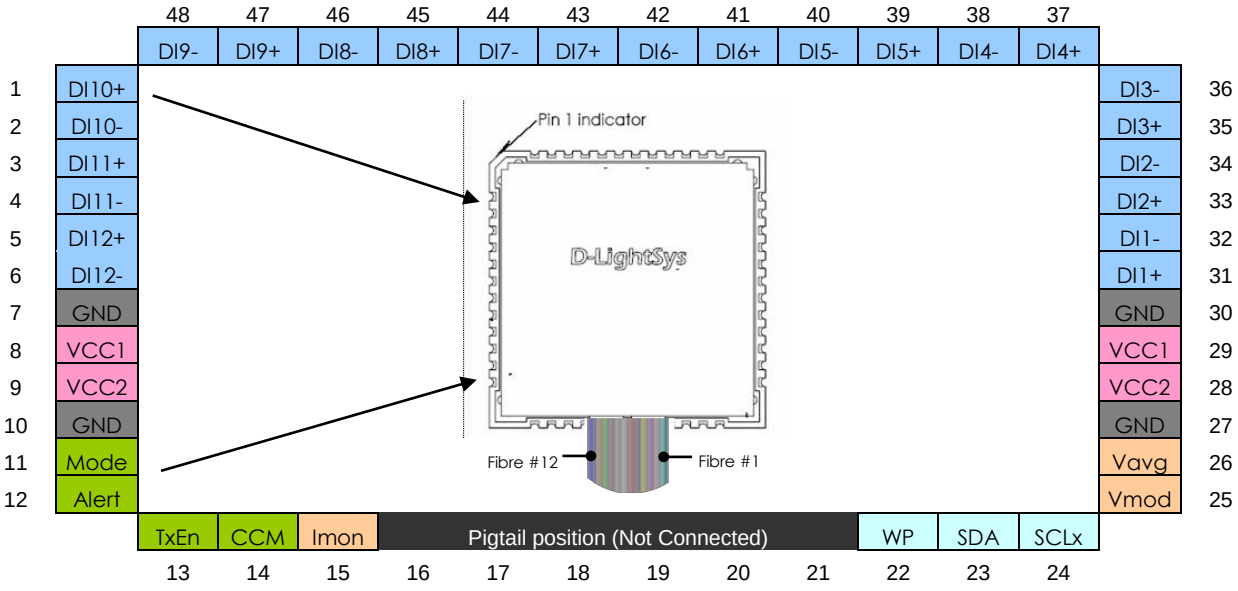
	1	2	3	4	5	6	7	8	9	10
A	D11+	GND	D10-	GND	D5-	D5+	GND	D3+	GND	D2-
B	D11-	GND	D10+	GND	GND	GND	GND	D3-	GND	D2+
C	GND	GND	GND	GND	D6-	D6+	GND	GND	GND	GND
D	D12+	GND	D9-	GND	GND	GND	GND	D4+	GND	D1-
E	D12-	GND	D9+	GND	D7-	D7+	GND	D4-	GND	D1+
F	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
G	VCC1	VCC1	VCC2	GND	D8-	D8+	GND	VCC2	VCC1	VCC1
H	Alert	Vmod	VCC2	GND	GND	GND	GND	VCC2	Vavg	WP
J	Mode	Imon	NC	NC	TDI	TDO	A0	A1	Vther	SDA
K	TxEn	CCM	NC	NC	TCK	TMS	TRST	A2	SCLD	SCLC

(View from top or from the application board)

HSLink
Power Supply
Analog monitors/controls
Digital monitors/controls
Ground pins
JTAG Interface
Serial interface
Non Connected

Note that the module pin numbering is independent from the Meg-Array numbering, in order to allow module keying by rotating the Meg-Array by 90° steps. Contact sales or technical support for module keying options.

LCC Package Pin Layout (DLT-xx-25x-IL-Pyz-Lvv Option)



DATASHEET

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Package mechanical drawings

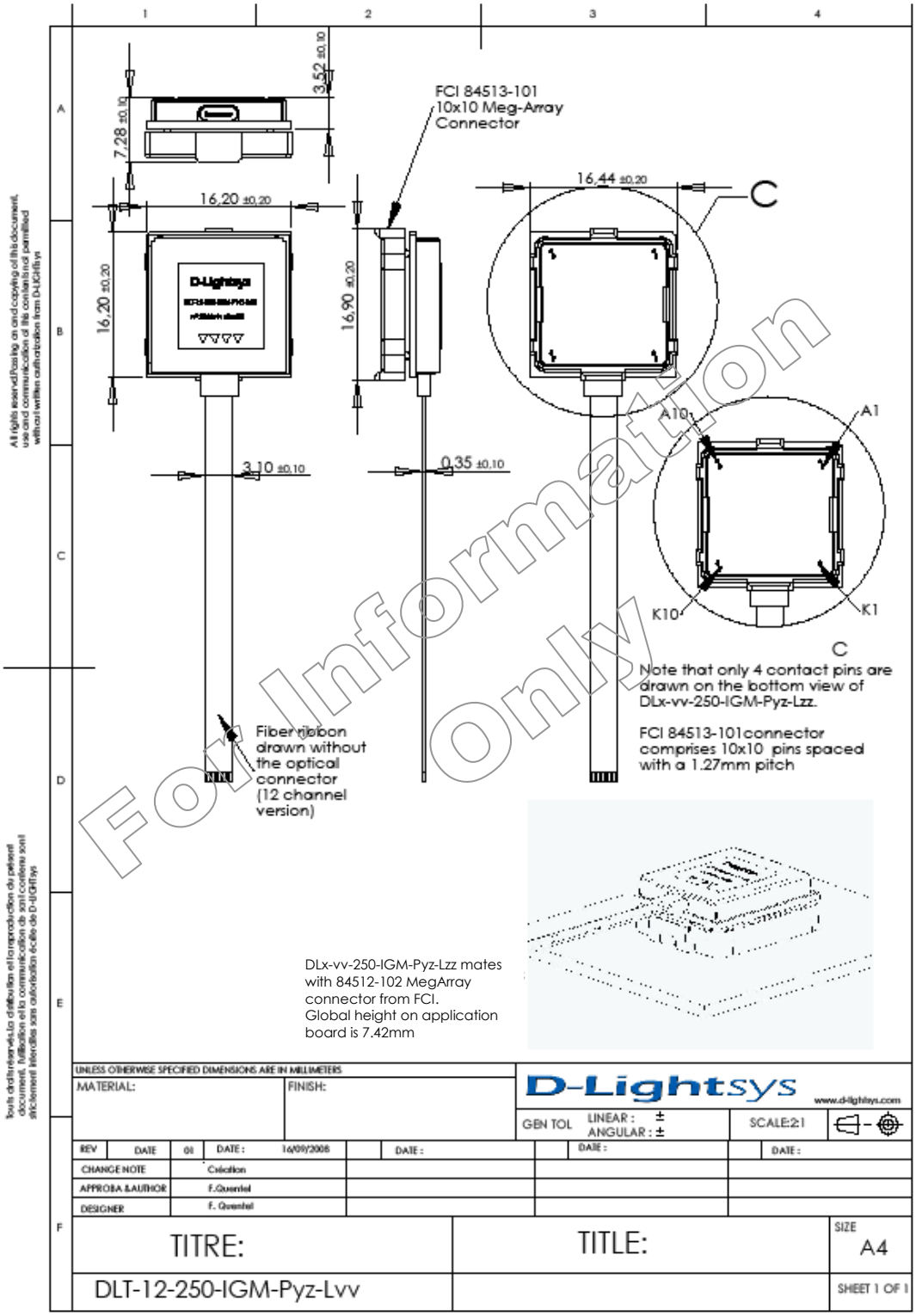

Figure 11 - DLT-xx-25x-IGM-Pyz mechanical drawing

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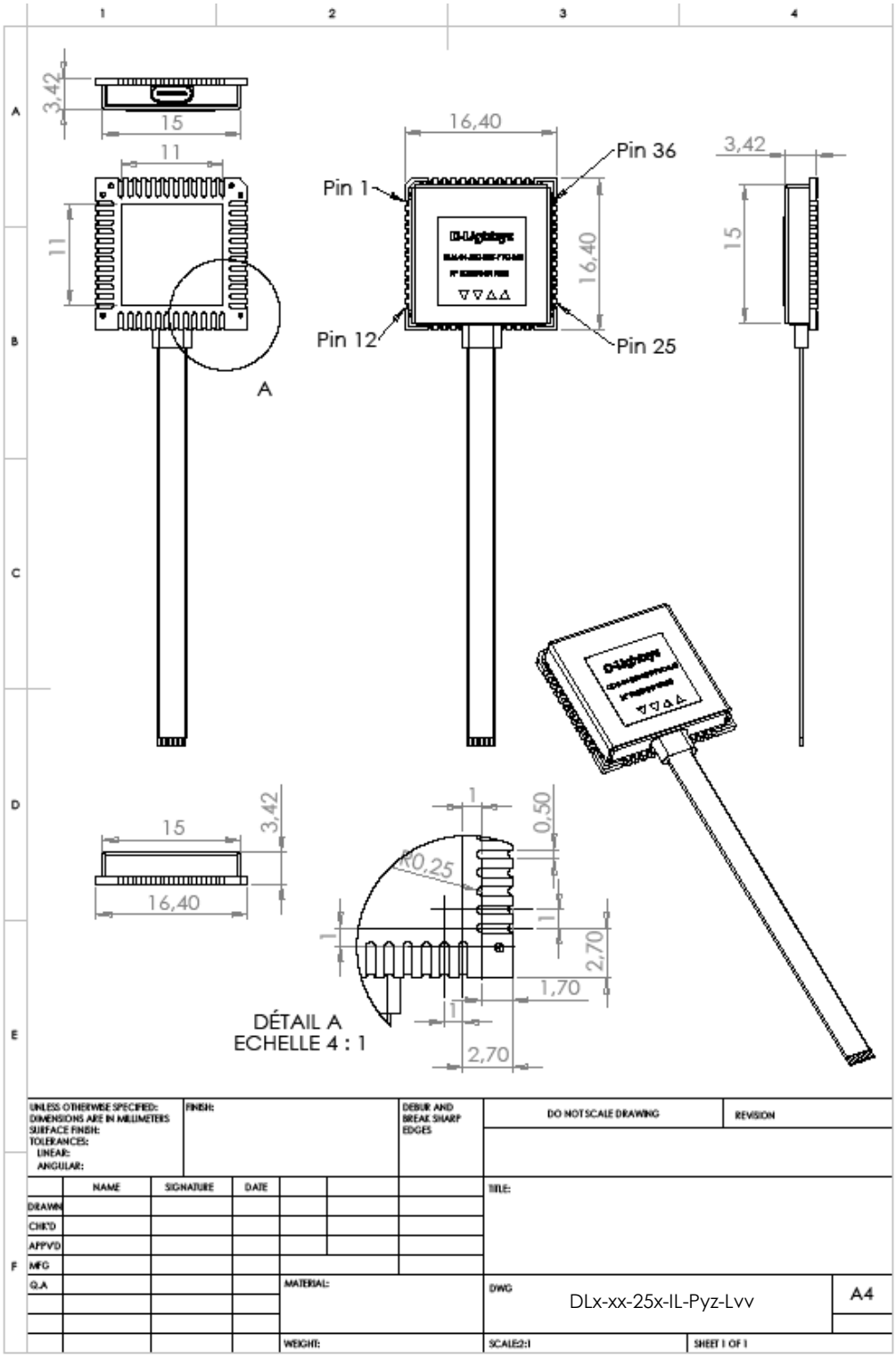

Figure 12 - DLT-xx-25x-IL-Pyz mechanical drawing

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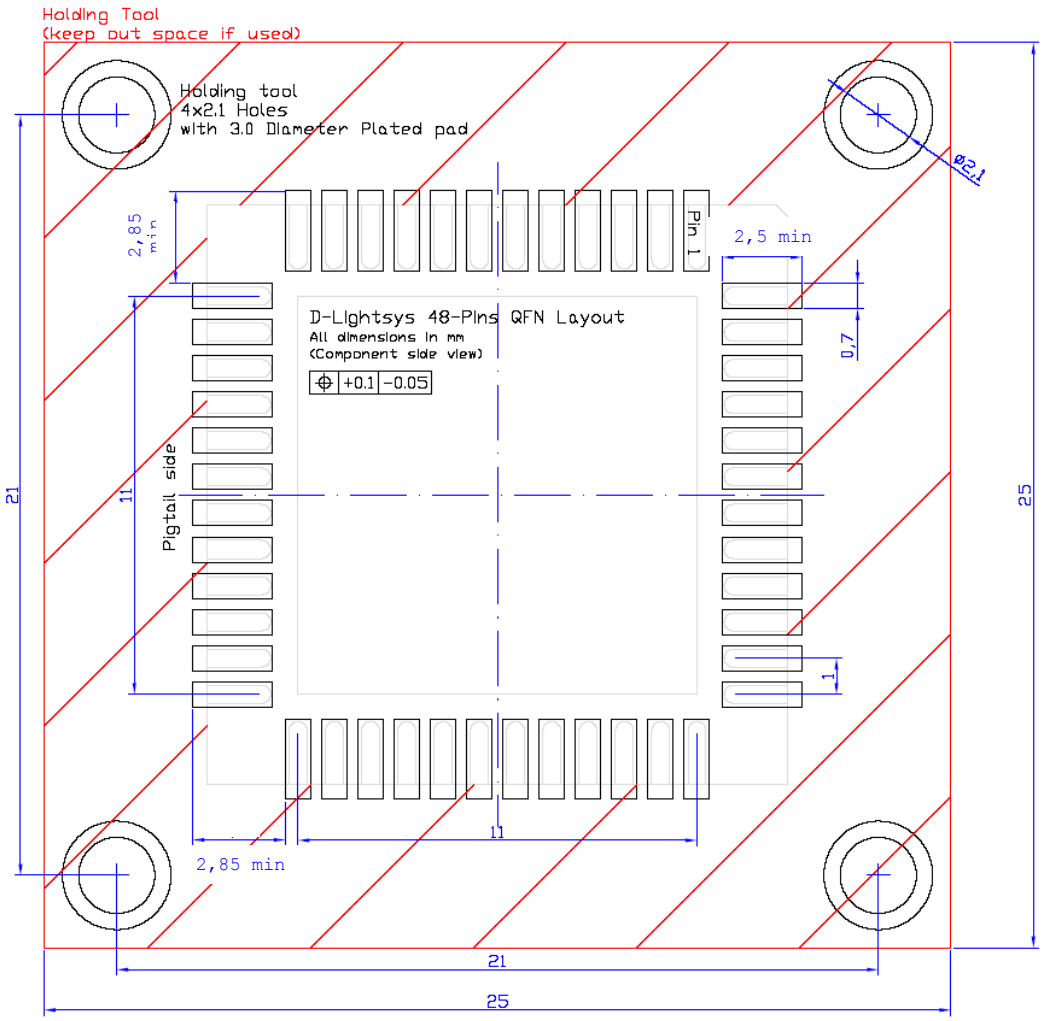
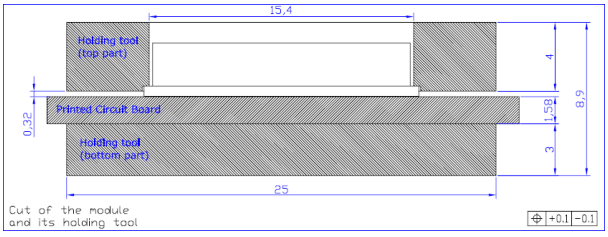
Module holding tool option:
If the module is intended to be used with the holding tool (Ref: HT-DLM-v1.0), The 4xØ2.1mm diameter holes and the the keep out space (Both sides) presented in the previous figure should be used. If the module is directly soldered on board, 4xØ2.1mm Holes and keep out space could be omitted.

LCC package PCB Layout drawings

A typical PCB footprint is shown on the following figure (dimension are in mm).



Note:
If the module is intended to be used with the holding tool (Ref: HT-DLM-v1.0), The 4xØ2.1mm diameter holes and the the keep out space (Both sides) presented in the previous figure should be used. If the module is directly soldered on board, 4xØ2.1mm Holes and keep out space could be omitted.



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D-Light DLT-xx-251-Iw-Pyz-Lvv
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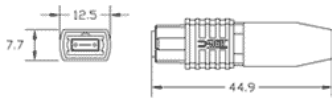
Pigtail information

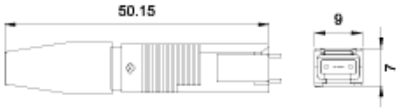
The DLT-xx-251-Iw-Pyz optical pigtail consists of a standard fiber ribbon optical cable terminated by an MT-compatible connector. Pigtail length can be adjusted to fit the customer's requirements.

The following pigtail connectors are available.

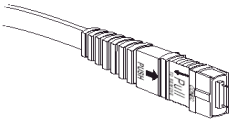
- **O option :** MPO connector (based on MT ferrule).



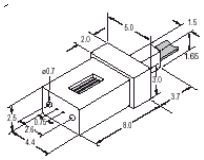
- **X option :** MPX connector (based on MT ferrule).



- **T option :** MTP connector (based on MT ferrule).



- **N option :** No connector Pigtail mount with MT ferrule.



Related literature (distributed under Non-Disclosure Agreement)

Application Notes:

Ref: AN-SLM/01 *"S-Light Transceiver Usage"* Version 1.1
Ref: AN-SLM/02 *"S-Light and D-Light 2 wire serial interface usage"* Version 1.0
Ref: AN-SLM/03 *"D-Light and S-Light Input/Output Stage modeling"* Version 1.0
Ref: AN-SLM/04 *"S-Light Reliability Data"* Version 0.1
Ref: AN-SLM/05 *"S-Light and D-Light surface mount process"* Version 0.3
Ref: AN-SLM/06 *"S-Light and D-Light surface mount bonding process"* Version 1.0
Ref: AN-SLM/07 *"D-Light thermal modeling"* Version 0.1
Ref: AN-SLM/08 *"Hand soldering process for D-Lightsys QFN package"* Version 1.0
Ref: AN-SLM/09 *"10Gbps operation of EVM-SLM/02 FR-4 evaluation board analysis"* Version 1.0

Evaluation board & Software materials:

Ref: EVM-DLx/01 "*DLx-www-xy-Pz* Evaluation board documentations" Version 1.0
Ref: SOF-DLM/01 "Windows Based D-Light family module programming software user's guide"

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