SN65DP141 DisplayPort Linear Redriver

1 Features

- Supports VESA DisplayPort 1.3, and eDP 1.4
- Quad Channel Linear Redriver Supporting Data Rates up to 12 Gbps including DisplayPort RBR, HBR, HBR2 and HBR3
- Protocol Agnostic
- Transparent to DP Link Training
- Position Independent on the Link Suitable for Source, Sink and Cable Applications
- 15-dB Analog Equalization at 6 GHz
- Output Linear Dynamic Range: 1200 mV
- Bandwidth: >20 GHz
- Better than 16-dB Return Loss at 6 GHz
- 2.5-V or 3.3-V ±5% Single Power Supply Option
- Low Power Consumption with 80 mW per channel at 2.5 V V_{CC}
- GPIO or I^2C Control

2 Applications

- Tablets
- Notebooks
- Desktops
- Docking Stations

3 Description

The SN65DP141 is an asynchronous, protocol-agnostic, low latency, four-channel linear equalizer optimized for use up to 12 Gbps and compensates for losses due to board traces and cables.

The device is transparent to DisplayPort (DP) link training such a way that a DP source and a sink can perform effective link training overcoming traditional “aux snooping” re-drivers’ shortcomings. Additionally, the device is position independent. It can be placed inside source, cable or sink effectively providing a “negative loss” component to the overall link budget. Linear equalization inside SN65DP141 also increases link margin when used with a receiver implementing Decision Feedback Equalization (DFE).

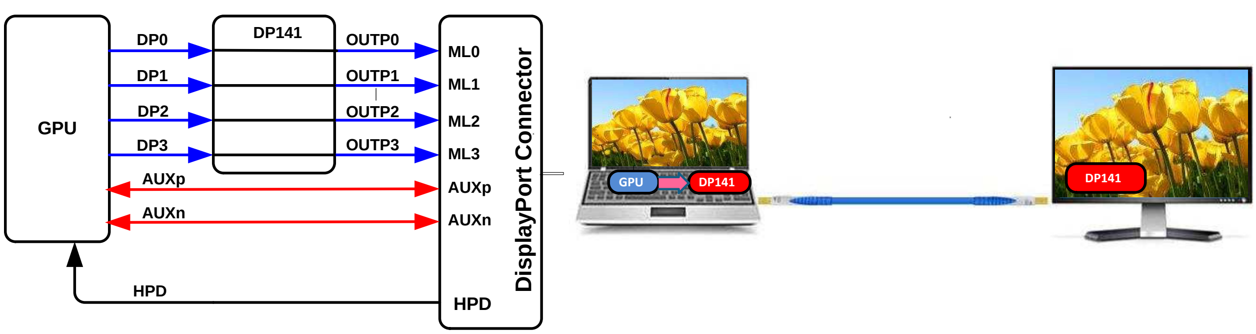
SN65DP141 allows independent channel control for equalization, gain, dynamic range using both I^2C and GPIO configurations.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65DP141	WQFN (38)	7.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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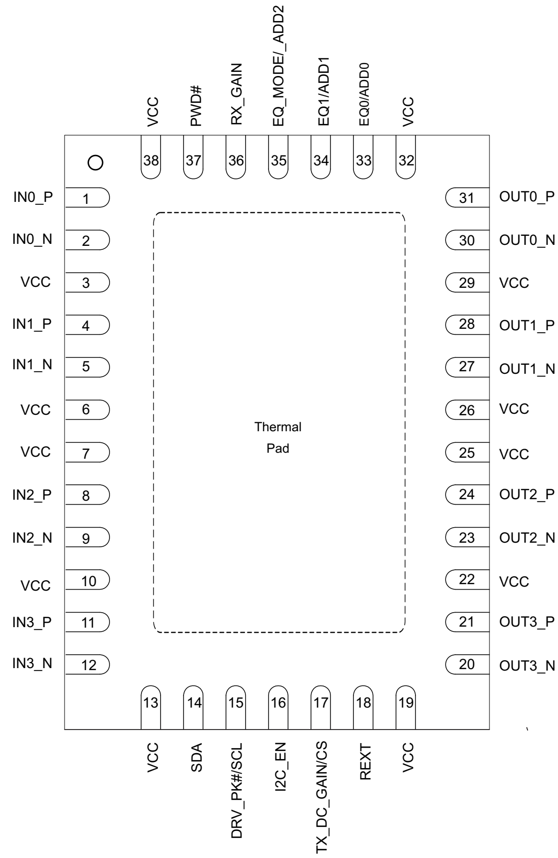
4 Revision History

DATE	REVISION	NOTES
February 2016	*	Initial release.

5 Pin Configuration and Functions

RLJ Package
38 Pins (WQFN)
Top View



It is required for thermal pad to be soldered to ground for better thermal performance.

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DIFFERENTIAL HIGH-SPEED I/O			
IN0_P	1	I	Differential input, lane 0 (with 50 Ω termination to input common mode)
IN0_N	2	I	
IN1_P	4	I	Differential input, lane 1 (with 50 Ω termination to input common mode)
IN1_N	5	I	
IN2_P	8	i	Differential input, lane 2 (with 50 Ω termination to input common mode)
IN2_N	9	I	
IN3_P	11	I	Differential input, lane 3 (with 50 Ω termination to input common mode)
IN3_N	12	I	
OUT0_P	31	O	Differential output, lane 0
OUT0_N	30	O	
OUT1_P	28	O	Differential output, lane 1
OUT1_N	27	O	
OUT2_P	24	O	Differential output, lane 2
OUT2_N	23	O	
OUT3_P	21	O	Differential output, lane 3
OUT3_N	20	O	

Pin Functions (continued)

PIN		I/O	DESCRIPTION	
NAME	NO.			
CONTROL SIGNALS				
SDA	14	I/O (open drain)	GPIO mode: No action needed.	I^{2}C mode: I^{2}C data. Connect a 10-kΩ pull-up resistor externally.
DRV_PK#/SCL	15	I (with 200-kΩ internal pull-up)	GPIO mode: HIGH: disable Driver peaking LOW: enables Driver 6-dB AC peaking	I^{2}C mode: I^{2}C CLK. Connect a 10-kΩ pull-up resistor externally.
I2C_EN	16	I (with 200-kΩ internal pull-up)	Configures the device operation for I^{2}C or GPIO mode: HIGH: enables I2C mode LOW: enables GPIO mode	
TX_DC_GAIN/CS	17	I (with 200-kΩ Internal pull-down, 2.5V/3.3V CMOS)	GPIO mode: HIGH: 6 dB DC gain for transmitter LOW: 0 dB DC gain for transmitter	I^{2}C mode: HIGH: acts as Chip Select LOW: disables I^{2}C interface
REXT	18	I (analog)	External Bias Resistor: 1,200 Ω to GND	
EQ0/ADD0	33	I (2.5V/3.3V CMOS - 3-state)	GPIO mode: Working with RX_GAIN and EQ1 to determine the receiver DC and AC gain.	I^{2}C mode: ADD0 along with pins ADD1 and ADD2 comprise the three bits of I^{2}C slave address. ADD2:ADD1:ADD0:XXX
EQ_MODE/ ADD2	35	I (with 200-kΩ Internal pull-down, 2.5V/3.3V CMOS)	GPIO mode: HIGH: Trace mode LOW: Cable mode	I^{2}C mode: ADD2 along with pins ADD1 and ADD0 comprise the three bits of I^{2}C slave address. ADD2:ADD1:ADD0:XXX
RX_GAIN	36	I (2.5V/3.3V CMOS - 3-state)	GPIO mode: Working with EQ0 and EQ1 to determine the receiver DC and AC gain.	I^{2}C mode: No action needed
PWD#	37	I (with 200-kΩ Internal pull-up, 2.5V/3.3V CMOS)	HIGH: Normal Operation LOW: Power downs the device, inputs off and outputs disabled, resets I^{2}C	
EQ1/ADD1	34	I (2.5V/3.3V CMOS - 3-state)	GPIO mode: Working with RX_GAIN and EQ0 to determine the receiver DC and AC gain.	I^{2}C mode: ADD1 along with pins ADD0 and ADD2 comprise the three bits of I^{2}C slave address ADD2:ADD1:ADD0:XXX
POWER SUPPLY				
VCC	3, 6, 7, 10, 13, 19, 22, 25, 26, 29, 32, 38	Power	Power supply 2.5V ±5%, 3.3V ±5%	
GND Center Pad		Ground	The ground center pad is the metal contact at the bottom of the package. This pad must be connected to the GND plane. At least 15 PCB vias are recommended to minimize inductance and provide a solid ground. Refer to the package drawing (RLJ-package) for the via placement.	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage range	VCC	–0.3	4	V
Differential voltage between INx_P and INx_N	VIN, DIFF	–2.5	2.5	V
Voltage at INx_P and INx_N,	VIN+, IN–	–0.5	V_{CC} + 0.5	V
Voltage on control IO pins, V_{IO}		–0.5	V_{CC} + 0.5	V
Continuous current at high speed differential data inputs(differential)	IN+, IN–	–25	25	mA
Continuous current at high speed differential data outputs	IOUT+, IOUT–	–25	25	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. .

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DR	Operating data rate			12	Gbps
V_{CC}	Supply voltage	2.375	2.5/3.3	3.465	V
T_C	Junction temperature	–10		125	°C
T_A	Operating free-air temperature	–40		85	°C
CMOS DC SPECIFICATIONS					
V_{IH}	Input high voltage	0.8 x V_{CC}			V
$V_{(MID)}$	Input middle voltage	V_{CC} x 0.4		V_{CC} x 0.6	V
V_{IL}	Input low voltage	–0.5		0.2 x V_{CC}	V

6.4 Thermal Information

THERMAL METRIC(1)		SN65DP141	UNIT
		RLJ (WQFN)	
		38 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER CONSUMPTION						
P_{DL}	Device Power dissipation	V_{OD} = Low, V_{CC} = 3.3 V and all 4 channels active		450	625	mW
		V_{OD} = Low, V_{CC} = 2.5 V and all 4 channels active		317	475	mW
P_{DH}	Device Power dissipation	V_{OD} = High, V_{CC} = 3.3 V and all 4 channels active		697	925	mW
		V_{OD} = High, V_{CC} = 2.5 V and all 4 channels active		485	675	mW
P_{DOFF}	Device power with all 4 channels switched off	Refer to I2C section for device configuration		10		mW
CMOS DC SPECIFICATIONS						
I_{IH}	High level input current	V_{IN} = 0.9 × V_{CC}	-40	17	40	µA
I_{IL}	Low level input current	V_{IN} = 0.1 × V_{CC}	-40	17	40	µA
CML INPUTS (IN[3:0]_P, IN[3:0]_N)						
R_{IN}	Differential input resistance	INx_P to INx_N		100		Ω
V_{IN}	Input linear dynamic range	Gain = 0.5		1200		mVpp
V_{ICM}	Input common mode voltage	Internally biased		V_{CC} – 0.8		V
SCD11	Input differential to common mode conversion	100 MHz to 6 GHz		-20		dB
SDD11	Differential input return loss	100 MHz to 6 GHz		-15		dB
CML OUTPUTS (OUT[3:0]_P, OUT[3:0]_N)						
V_{OD}	Output linear dynamic range	R_L = 100 Ω, V_{OD} = HIGH		1200		mVpp
		R_L = 100 Ω, V_{OD} = LOW		600		mVpp
V_{OS}	Output offset voltage	R_L = 100 Ω, 0 V applied at inputs		10		mVpp
V_{OCM}	Output common mode voltage			V_{CC} – 0.4		V
$V_{CM(RIP)}$	Common mode output ripple	K28.5 pattern at 12 Gbps on all 4 channels, No interconnect loss, V_{OD} = HIGH		10	20	mVRMS
$V_{OD(RIP)}$	Differential path output ripple	K28.5 pattern at 12 Gbps on all channels, No interconnect loss, V_{IN} = 1200 mVpp.			20	mVpp
$V_{OC(SS)}$	Change in steady-state common mode output voltage between logic states			±10		mV

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML OUTPUTS (OUT[3:0]_P, OUT[3:0]_N)						
t_R	Rise time (1)	Input signal with 30 ps rise time, 20% to 80%, ee Figure 7		31		ps
t_F	Fall time (1)	Input signal with 30 ps fall time, 20% to 80%, See Figure 7		32		ps
SDD22	Differential output return loss	6 GHz (12 Gbps)		-14		dB
		4.05 GHz (HBR3, 8.1 Gbps)		–9.33		dB
		4.05 GHz (HBR3, 8.1 Gbps)		–6.35		dB
		1.35 GHz (HBR, 2.7Gbps)		–3.5		dB
t_{PLH}	Low-to-high propagation delay	See Figure 6		65		ps
t_{PHL}	High-to-low propagation delay			65		ps
$t_{SK(O)}$	Inter-Pair (lane to lane) output skew (2)	All outputs terminated with 100 Ω, See Figure 8		8		ps
$t_{SK(PP)}$	Part-to-part skew (3)	All outputs terminated with 100 Ω			50	ps
r_{OT}	Single ended output resistance	Single ended on-chip termination to V_{CC}, Outputs are AC coupled		50		Ω
r_{OM}	Output termination mismatch at 1 MHz	$\Delta r_{OM} = 2 \times \left(\frac{rp - rn}{rn + rp} \right) \times 100$		5%		
	Channel-to-channel isolation	Frequency at 6 GHz	35	45		dB
	Output referred noise (4)	10 MHz to 6 GHz, No other noise source present, V_{OD} = LOW		400		µVRMS
		10M Hz to 6 GHz, No other noise source present, V_{OD} = HIGH		500		µVRMS
EQUALIZATION						
G	At 6 GHz input signal	Equalization Gain, EQ = MAX		15		dB
$V_{(pre)}$	Output pre-cursor pre-emphasis	Input signal with 3.75 pre-cursor and measure it on the output signal, See Figure 9		3.75		dB
$V_{(pst)}$	Output post-cursor pre-emphasis	Input signal with 12 dB post-cursor and measure it on the output signal, See Figure 9		12		dB

(1) Rise and Fall measurements include board and channel effects of the test environment, refer to Figure 5 and Figure 7.
(2) $t_{SK(O)}$ is the magnitude of the time difference between the channels.
(3) $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same
(4) All noise sources added.

6.7 Switching Characteristics, I²C Interface

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency			400	KHz
t_{BUF}	Bus free time between START and STOP conditions	1.3			µs
t_{HDSTA}	"Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HIGH}	High period of the SCL clock	0.6			µs
t_{SUSTA}	Setup time for a repeated START condition	0.6			µs
t_{HDDAT}	Data HOLD time	0			µs
t_{SUDAT}	Data setup time	100			µs
t_R	Rise time of both SDA and SCL signals			300	µs
t_F	Fall time of both SDA and SCL signals			300	µs
t_{SUSTO}	Setup time for STOP condition	0.6			µs

6.8 Typical Characteristics

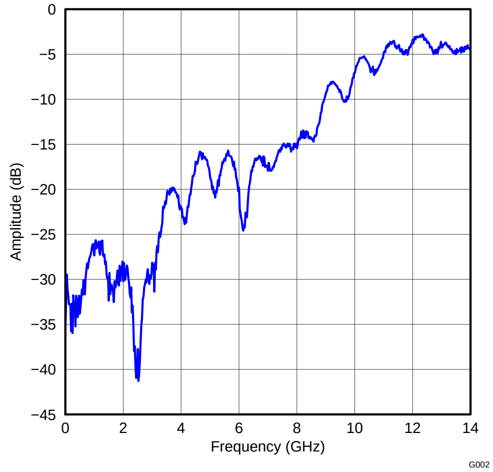


Figure 1. Differential Input Return Loss

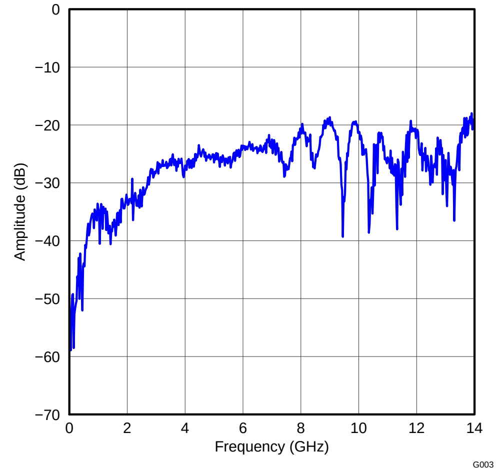


Figure 2. Differential to Common Mode Conversion

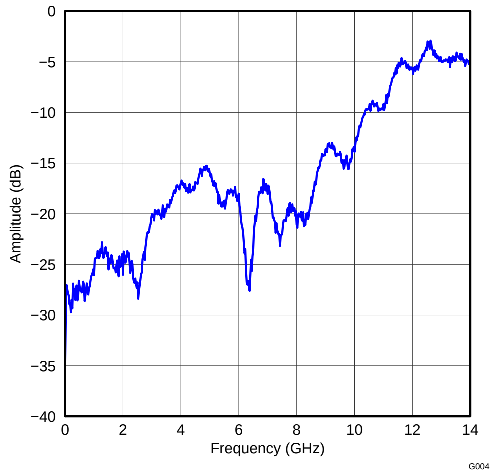


Figure 3. Differential Output Return Loss

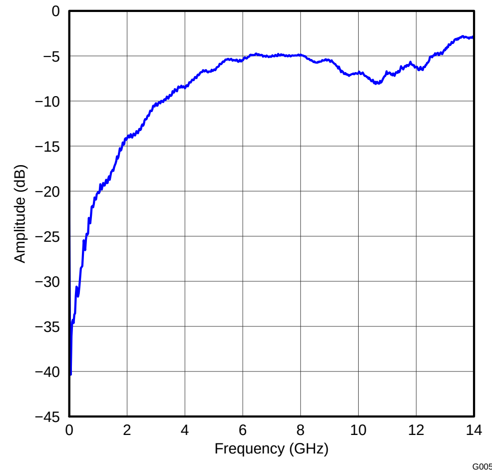


Figure 4. Common Mode Output Return Loss

7 Parameter Measurement Information

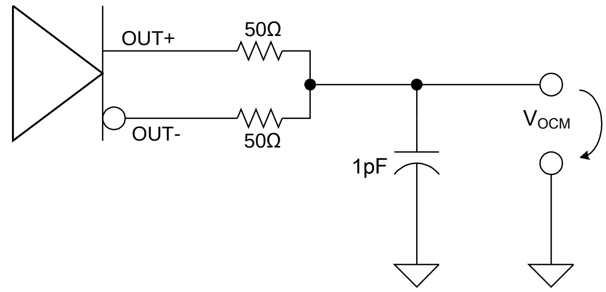


Figure 5. Common Mode Output Voltage Test Circuit

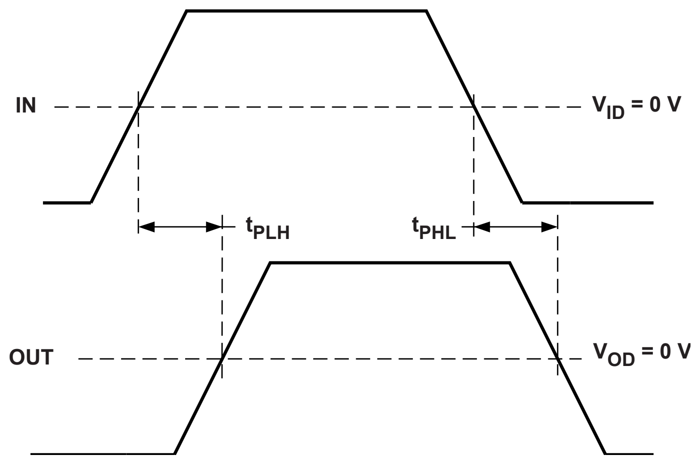


Figure 6. Propagation Delay Input to Output

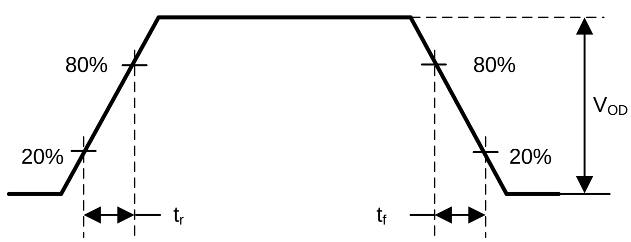


Figure 7. Output Rise and Fall Times

Parameter Measurement Information (continued)

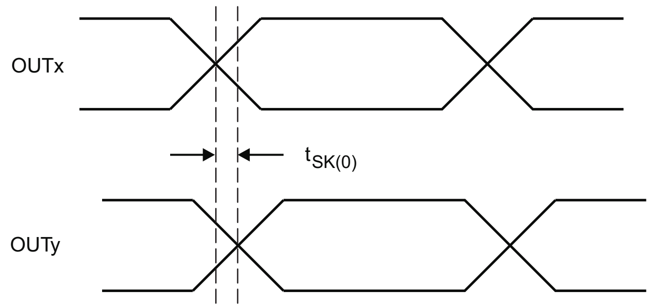


Figure 8. Output Inter-Pair Skew

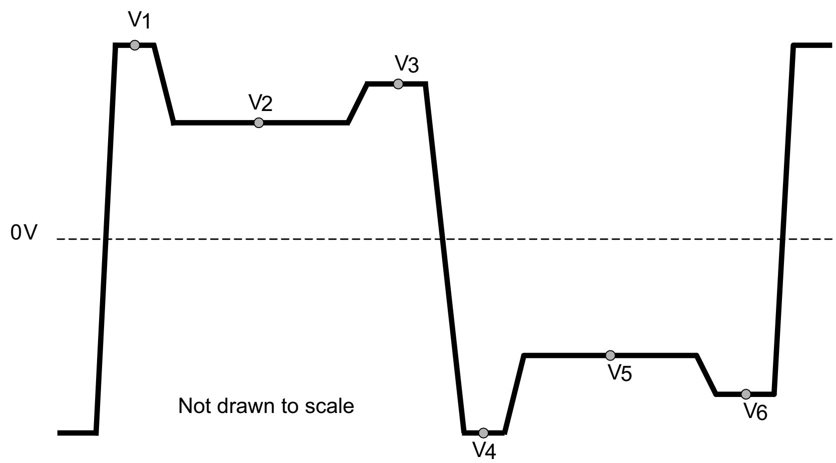


Figure 9. $V_{(pre)}$ and $V_{(post)}$ (test pattern is 1111111100000000 (8-1s, 8-0s))

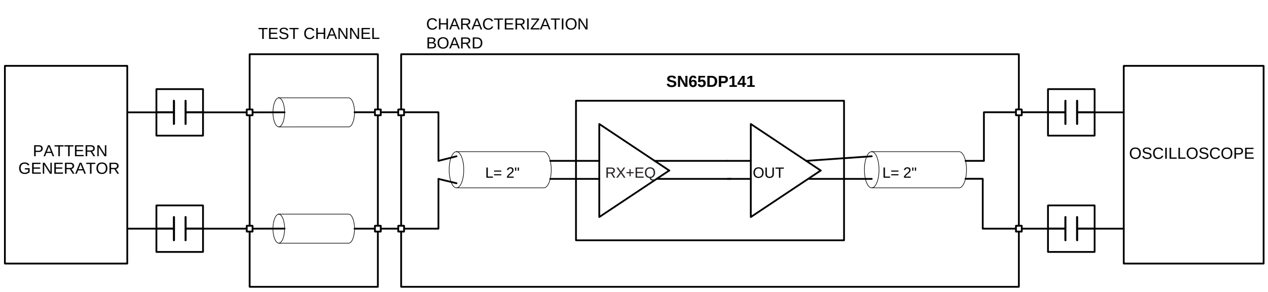


Figure 10. Receive Side Performance Test Circuit

Parameter Measurement Information (continued)

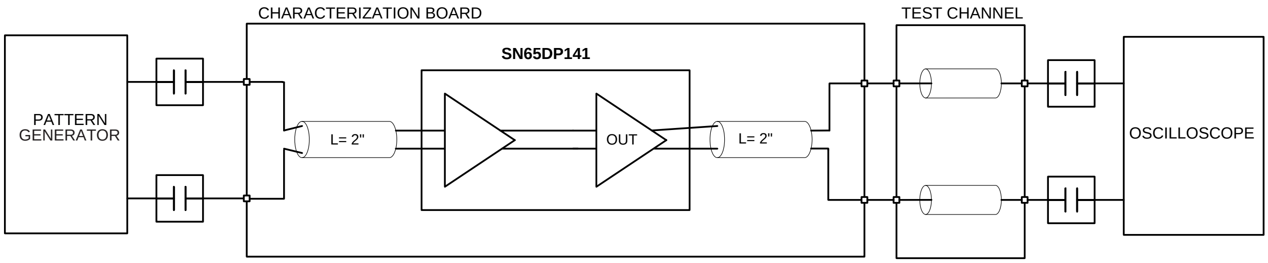


Figure 11. Transmit Side Performance Test Circuit

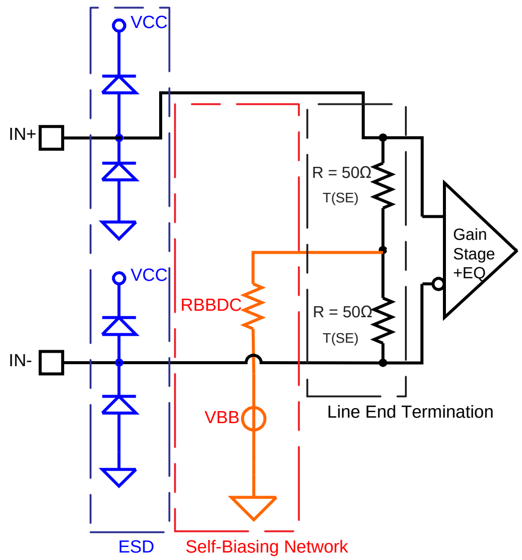


Figure 12. Equivalent Input Circuit

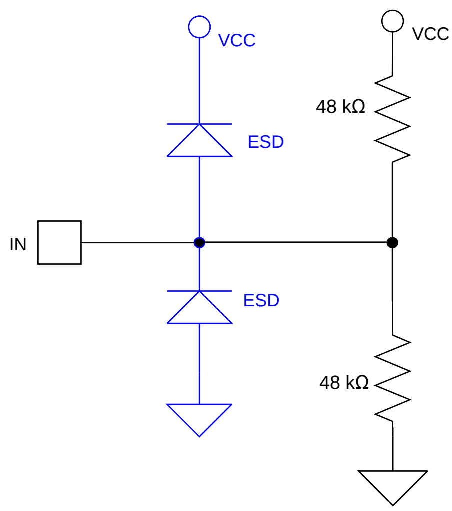


Figure 13. 3-Level Input Biasing Network

Parameter Measurement Information (continued)

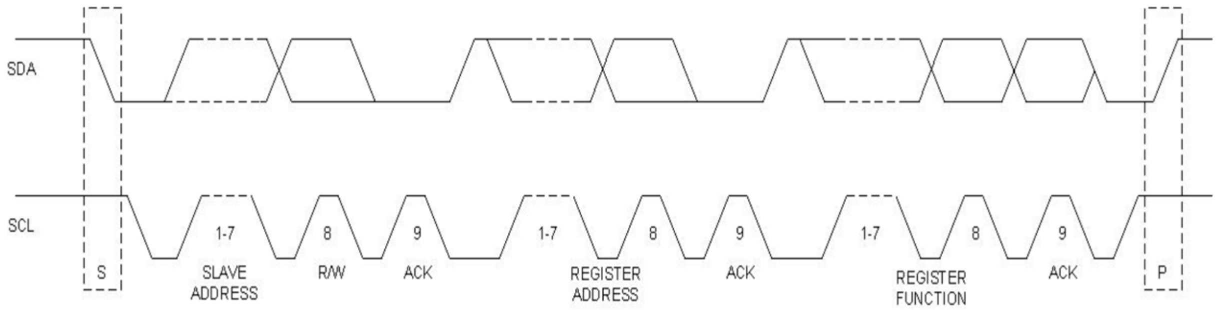


Figure 14. Two - Wire Serial Interface Data Transfer

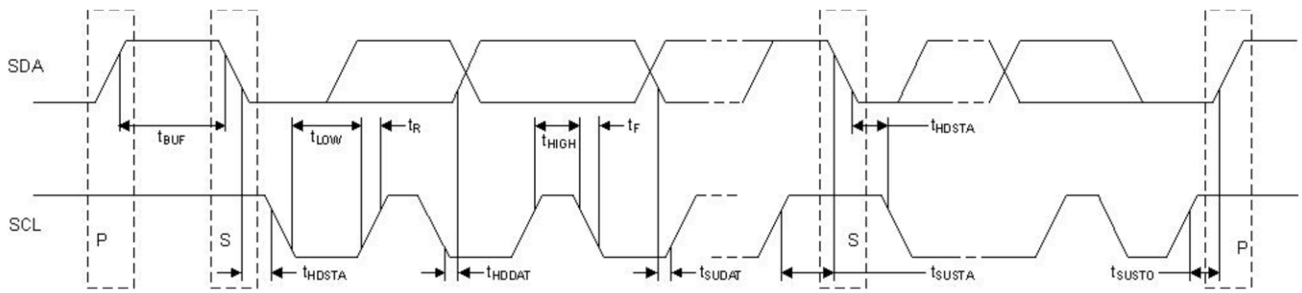


Figure 15. Two - Wire Serial Interface Timing Diagram

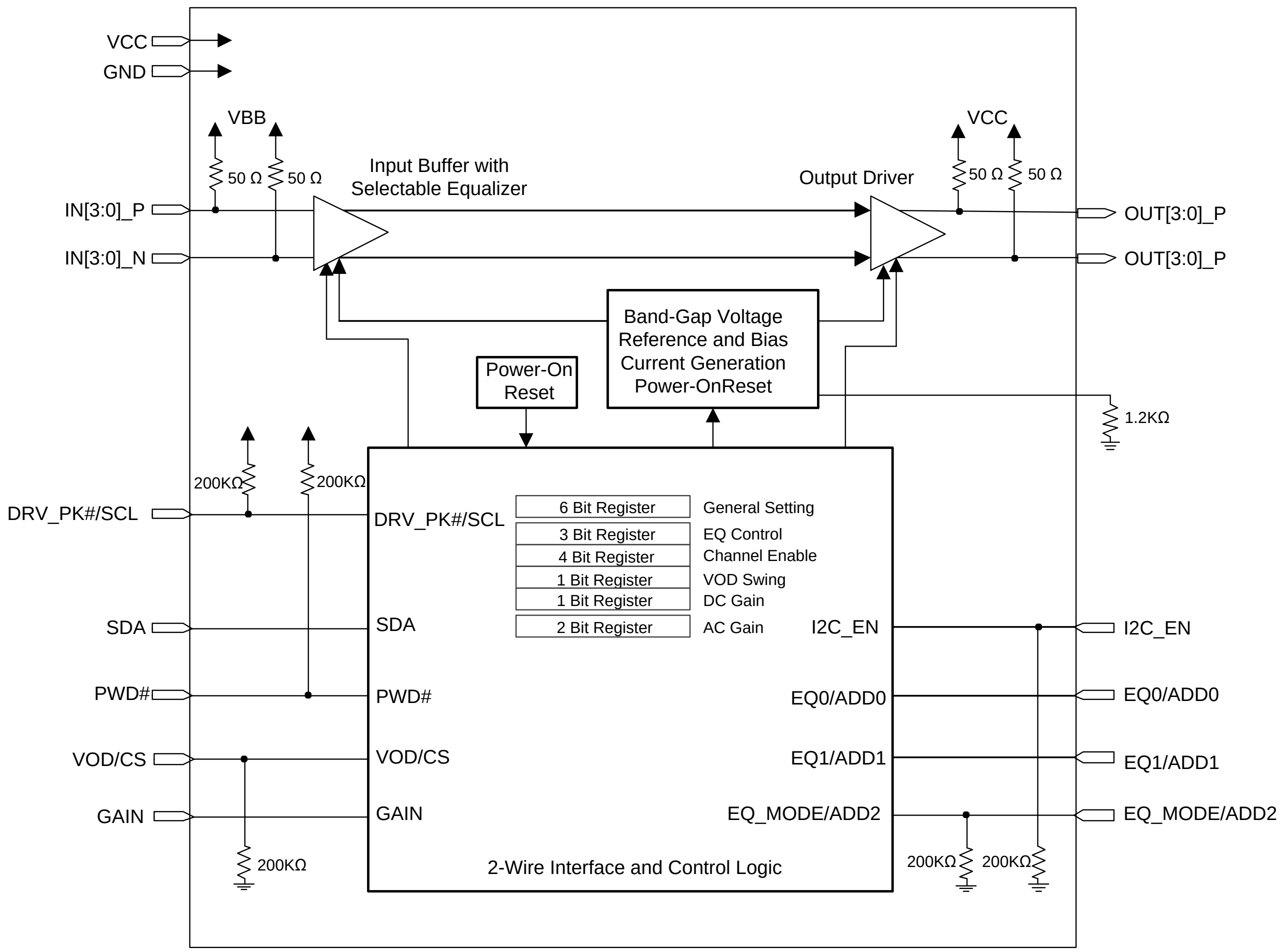
8 Detailed Description

8.1 Overview

The SN65DP141 is an asynchronous, protocol-agnostic, low latency, four-channel linear equalizer optimized for use up to 12 Gbps. The characteristics of this device make it transparent to DisplayPort (DP) link training, it supports all the available DP bit rates from RBR to HBR3 (1.6 Gbps, 2.7 Gbps, 5.4 Gbps and 8.1 Gbps respectively). Additionally, the SN65DP141 is configurable to a trace or cable mode, and hence improves its performance depending on the type of channel it is being used. Its transparency to the DP link training makes the SN65DP141 a position independent device, suitable for source/sink or cable applications, effectively providing a “negative loss” component to the overall link budget, in order to compensate the signal degradation over the channel.

The SN65DP141 is configurable by means of I^{2}C and GPIOs, allowing independent channel control for activation, equalization, gain, dynamic range.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DC and AC Independent Gain Control

Besides the functional block diagram, the behavior of the SN65DP141 can be described as it is shown in Figure 16; where the input stage first applies a DC gain (0 dB or –6 dB), and then equalizes the signal, which is driven to the output stage, where the SN65DP141 applies an output DC gain (0 dB or 6 dB).

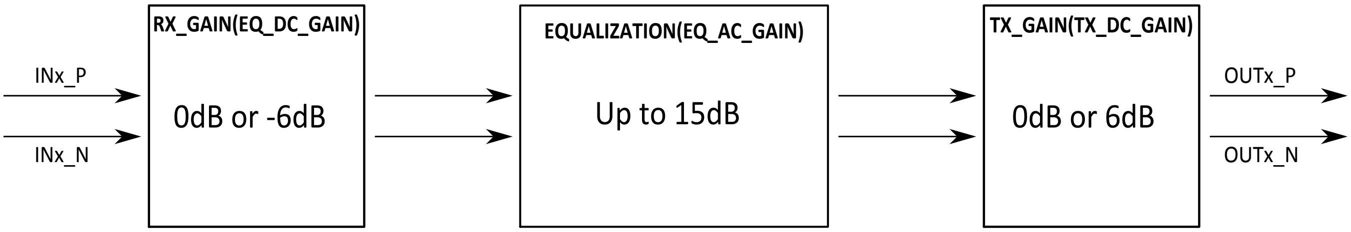


Figure 16. DP141 Signal Chain Gain Control

8.3.2 Two-Wire Serial Interface and Control Logic

The SN65DP141 uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCL, are driven, respectively, by the serial data and serial clock from a microcontroller, for example. The SDA and SCK pins require external 10 kΩ pull-ups to VCC.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out control and status signals. The SN65DP141 is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7 bit slave address (0000ADD [2:0]) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ. The ADD [2:0] address bits change with the status of the ADD2, ADD1, and ADD0 device pins, respectively. If the pins are left floating or pulled down, the 7 bit slave address is 0000000.
3. 8-bit register address
4. 8-bit register data word
5. STOP command

Regarding timing, the SN65DP141 is I^2C compatible. The typical timing is shown in Figure 15 and a complete data transfer is shown in Figure 14. Parameters for these figures are defined in the I^2C Interface section of the *Switching Characteristics*.

8.3.3 Bus Idle

Both SDA and SCL lines remain HIGH

8.3.4 Start Data Transfer

A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

8.3.5 Stop Data Transfer

A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Feature Description (continued)

8.3.6 Data Transfer

The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

8.3.7 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

8.4 Device Functional Modes

8.4.1 TRACE and CABLE Equalization Modes

The SN65DP141 is optimized for both trace and cable application at its input. The device pin EQ_MODE sets the EQ gain curve profile suitable for these two use cases.

8.4.2 Control Modes

The SN65DP141 features two control modes: GPIO and I2C, and the selection between these two modes is by means of the I2C_EN terminal, which activates the GPIO when tied to LOW; otherwise; the I2C mode is active due to its internal pull-up resistance.

8.4.3 GPIO MODE

Device Pins RX_GAIN, EQ1 and EQ0 determines receiver DC and AC gain as shown in Table 1 and Table 2.

Table 1. EQ Pin Settings

EQ1	EQ0	EQ Setting
GND	GND	000
GND	HiZ	000
GND	VCC	001
HiZ	GND	010
HiZ	HiZ	011
HiZ	VCC	100
VCC	GND	101
VCC	HiZ	110
VCC	VCC	111

Table 2. RX DC and AC GAIN Settings

EQ Configuration		EQ Gain	
EQ Setting	RX_GAIN	EQ_DC_GAIN (dB)	EQ_AC_GAIN (dB)
000 - 111	LOW	–6	1 - 9
000 - 111	HiZ	–6	7 - 17
000 - 111	HIGH	0	1 - 9

8.4.4 I²C Mode

Table 3. I2C Control Settings Description for RX DC and AC GAIN

EQ_MODE	EQ_DC GAIN	RX_GAIN<1:0>	EQ_Setting<2:0>	DC GAIN (dB)	AC GAIN (dB)	APPLICATION
0	0	00	000 to 111	–6	1 to 9	Short Input Cable; Large Input Swing
		11	000 to 111	–6	7 to 17	Long Input Cable; Large Input Swing
	1	01	000 to 111	0	1 to 9	Short Input Cable; Small Input Swing
		11	000 to 111	0	2 to 10	Short Input Cable, Small Input Swing
1	0	00	000 to 111	–6	1 to 9	Short Input Trace; Large Input Swing
		11	000 to 111	–6	7 to 17	Long Input Trace; Large Input Swing
	1	01	000 to 111	0	1 to 9	Short Input Trace; Small Input Swing
		11	000 to 111	0	2 to 10	Short Input Trace, Small Input Swing

8.5 Register Maps

8.5.1 Register 0x00 (General Device Settings) (offset = 00000000) [reset = 00000000]

Figure 17. Register 0x00 (General Device Settings)

7	6	5	4	3	2	1	0
SW_GPIO	PWRDOWN	SYNC_01	SYNC_23	SYNC_ALL	EQ_MODE		RSVD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. Register 0x00 (General Device Settings)

Bit	Field	Type	Reset	Description
7	SW_GPIO	R/W	0	Switching logic is controlled by GPIO or I2C: 0 = I2C control 1 = GPIO control
6	PWRDOWN	R/W	0	Power down the device: 0 = Normal operation 1 = Powerdown
5	SYNC_01	R/W	0	All settings from channel 1 will be used for channel 0 and 1: 0 = Channel 0 tracking channel 1 settings 1 = No tracking tracking
4	SYNC_ 23	R/W	0	All settings from channel 2 will be used for channel 2 and 3: 0 = Channel 3 tracking channel 2 settings 1 = No channel tracking
3	SYNC_ALL	R/W	0	All settings from channel 1 will be used on all channels: 0 = All channels tracking channel 1 1 = No channel tracking Overwrites SYNC_01 and SYNC_23
2	EQ_MODE	R/W	0	Set EQ mode: 0 = Cable mode 1 = Trace mode
1		R/W	0	
0	RSVD	R/W	0	For TI use only

8.5.2 Register 0x01 (Channel Enable) (offset = 00000000) [reset = 00000000]

Figure 18. Register 0x01 (Channel Enable)

7	6	5	4	3	2	1	0
				LN_EN_CH3	LN_EN_CH2	LN_EN_CH1	LN_EN_CH0
R	R	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Register 0x01 (Channel Enable)

Bit	Field	Type	Reset	Description
7		R	0	
6		R	0	
5		R	0	
4		R	0	
3	LN_EN_CH3	R/W	0	Channel 3 enable: 0 = Enable 1 = Disable
2	LN_EN_CH2	R/W	0	Channel 3 enable: 0 = Enable 1 = Disable
1	LN_EN_CH1	R/W	0	Channel 1 enable: 0 = Enable 1 = Disable
0	LN_EN_CH0	R/W	0	Channel 0 enable: 0 = Enable 1 = Disable

8.5.3 Register 0x02 (Channel 0 Control Settings) (offset = 00000000) [reset = 00000000]

Figure 19. Register 0x02 (Channel 0 Control Settings)

7	6	5	4	3	2	1	0
RSVD	EQ Setting<2>	EQ Setting<1>	EQ Setting<0>	TX_GAIN	EQ_DC_GAIN	RX_GAIN<1>	RX_GAIN<0>
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Register 0x02 (Channel 0 Control Settings)

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0	
6	EQ Setting<2>	R/W	0	Equalizer adjustment setting: 000 = Minimum equalization setting 111 = Maximum equalization setting
5	EQ Setting<1>	R/W	0	
4	EQ Setting<0>	R/W	0	
3	TX GAIN	R/W	0	Channel [0] TX_DC_GAIN control: 0 = Set 0 dB DC gain for transmitter 1 = Set 6 dB DC gain for transmitter
2	EQ_DC_GAIN	R/W	0	Channel [0] EQ DC gain: 0 = Set EQ DC gain to -6 dB 1 = Set EQ DC gain to -0 dB
1	RX_GAIN<1>	R/W	0	Equivalent to RX_GAIN control pin for channel [0]. 00: RX_GAIN = Low 01: RX_GAIN = HiZ 11: RX_GAIN = High
0	RX_GAIN<0>	R/W	0	

8.5.4 Register 0x03 (Channel 0 Enable Settings) (offset = 00000000) [reset = 00000000]

Figure 20. Register 0x03 (Channel 0 Enable Settings)

7	6	5	4	3	2	1	0
					DRV_PEAK	EQ_EN	DRV_EN
R	R	R	R	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Register 0x03 (Channel 0 Enable Settings)

Bit	Field	Type	Reset	Description
7		R	0	
6		R	0	
5		R	0	
4		R	0	
3		R	0	
2	DRV_PEAK	R/W	0	Channel [0] driver peaking: 0 = Disables driver Peaking 1 = Enables driver 6 db AC Peaking"
1	EQ_EN	R/W	0	Channel [0] EQ stage enable: 0 = Enable 1 = Disable
0	RSVDRV_EN	R/W	0	Channel [0] driver stage enable: 0 = Enable 1 = Disable

8.5.5 Register 0x05 (Channel 1 Control Settings) (offset = 00000000) [reset = 00000000]

Figure 21. Register 0x05 (Channel 1 Control Settings)

7	6	5	4	3	2	1	0
RSVD	EQ Setting<2>	EQ Setting<1>	EQ Setting<0>	TX_GAIN	EQ_DC_GAIN	RX_GAIN<1>	RX_GAIN<0>
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Register 0x05 (Channel 1 Control Settings)

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0	
6	EQ Setting<2>	R/W	0	Equalizer adjustment setting: 000 = Minimum equalization setting 111 = Maximum equalization setting
5	EQ Setting<1>	R/W	0	
4	EQ Setting<0>	R/W	0	
3	TX_GAIN	R/W	0	Channel [1] TX_DC_GAIN control: 0 = Set 0 dB DC gain for transmitter 1 = Set 6 dB DC gain for transmitter
2	EQ_DC_GAIN	R/W	0	Channel [1] EQ DC gain: 0 = Set EQ DC gain to -6 dB 1 = Set EQ DC gain to -0 dB
1	RX_GAIN<1>	R/W	0	Equivalent to RX_GAIN control pin for channel [1]. 00: RX_GAIN = Low 01: RX_GAIN = HiZ 11: RX_GAIN = High
0	RX_GAIN<0>	R/W	0	

8.5.6 Register 0x06 (Channel 1 Enable Settings) (offset = 00000000) [reset = 00000000]

Figure 22. Register 0x06 (Channel 1 Enable Settings)

7	6	5	4	3	2	1	0
					DRV_PEAK	EQ_EN	DRV_EN
R	R	R	R	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Register 0x06 (Channel 1 Enable Settings)

Bit	Field	Type	Reset	Description
7		R	0	
6		R	0	
5		R	0	
4		R	0	
3		R	0	
2	DRV_PEAK	R/W	0	Channel [1] driver peaking: 0 = Disables driver Peaking 1 = Enables driver 6 db AC Peaking
1	EQ_EN	R/W	0	Channel [1] EQ stage enable: 0 = Enable 1 = Disable
0	DRV_EN	R/W	0	Channel [1] driver stage enable: 0 = Enable 1 = Disable

8.5.7 Register 0x08 (Channel 2 Control Settings) (offset = 00000000) [reset = 00000000]

Figure 23. Register 0x08 (Channel 2 Control Settings)

7	6	5	4	3	2	1	0
RSVD	EQ Setting<2>	EQ Setting<1>	EQ Setting<0>	TX_GAIN	EQ_DC_GAIN	RX_GAIN<1>	RX_GAIN<0>
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. Register 0x08 (Channel 2 Control Settings)

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0	
6	EQ Setting<2>	R/W	0	Equalizer adjustment setting: 000 = Minimum equalization setting 111 = Maximum equalization setting
5	EQ Setting<1>	R/W	0	
4	EQ Setting<0>	R/W	0	
3	TX_GAIN	R/W	0	Channel [2] TX_DC_GAIN control: 0 = Set 0 dB DC gain for transmitter 1 = Set 6 dB DC gain for transmitter
2	EQ_DC_GAIN	R/W	0	Channel [2] EQ DC gain: 0 = Set EQ DC gain to -6 dB 1 = Set EQ DC gain to -0 dB
1	RX_GAIN<1>	R/W	0	Equivalent to RX_GAIN control pin for channel [2]. 00: RX_GAIN = Low 01: RX_GAIN = HiZ 11: RX_GAIN = High
0	RX_GAIN<0>	R/W	0	

8.5.8 Register 0x09 (Channel 2 Enable Settings) (offset = 00000000) [reset = 00000000]

Figure 24. Register 0x09 (Channel 2 Enable Settings)

7	6	5	4	3	2	1	0
					DRV_PEAK	EQ_EN	DRV_EN
R	R	R	R	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. Register 0x09 (Channel 2 Enable Settings)

Bit	Field	Type	Reset	Description
7		R	0	
6		R	0	
5		R	0	
4		R	0	
3		R	0	
2	DRV_PEAK	R/W	0	Channel [2] driver peaking: 0 = Disables driver Peaking 1 = Enables driver 6 db AC Peaking
1	EQ_EN	R/W	0	Channel [2] driver stage enable: 0 = Enable 1 = Disable
0	DRV_EN	R/W	0	Channel [2] driver stage enable: 0 = Enable 1 = Disable

8.5.9 Register 0x0B (Channel 3 Control Settings) (offset = 00000000) [reset = 00000000]

Figure 25. Register 0x0B (Channel 3 Control Settings)

7	6	5	4	3	2	1	0
RSVD	EQ Setting<2>	EQ Setting<1>	EQ Setting<0>	TX_GAIN	EQ_DC_GAIN	RX_GAIN<1>	RX_GAIN<0>
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. Register 0x0B (Channel 3 Control Settings)

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0	
6	EQ Setting<2>	R/W	0	Equalizer adjustment setting: 000 = Minimum equalization setting 111 = Maximum equalization setting
5	EQ Setting<1>	R/W	0	
4	EQ Setting<0>	R/W	0	
3	TX_GAIN	R/W	0	Channel [3] TX_DC_GAIN control: 0 = Set 0 dB DC gain for transmitter 1 = Set 6 dB DC gain for transmitter
2	EQ_DC_GAIN	R/W	0	Channel [3] EQ DC gain: 0 = Set EQ DC gain to -6 dB 1 = Set EQ DC gain to -0 dB
1	RX_GAIN<1>	R/W	0	Equivalent to RX_GAIN control pin for channel [3]. 00: RX_GAIN = Low 01: RX_GAIN = HiZ 11: RX_GAIN = High
0	RX_GAIN<0>	R/W	0	

8.5.10 Register 0x0C (Channel 3 Control Settings) (offset = 00000000) [reset = 00000000]

Figure 26. Register 0x0C (Channel 3 Enable Settings)

7	6	5	4	3	2	1	0
					DRV_PEAK	EQ_EN	DRV_EN
R	R	R	R	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. Register 0x0C (Channel 3 Enable Settings)

Bit	Field	Type	Reset	Description
7		R	0	
6		R	0	
5		R	0	
4		R	0	
3		R	0	
2	DRV_PEAK	R/W	0	Channel [3] driver peaking: 0 = Disables driver Peaking 1 = Enables driver 6db AC Peaking
1	EQ_EN	R/W	0	Channel [3] EQ stage enable: 0 = Enable 1 = Disable
0	RSVDRV_EN	R/W	0	Channel [3] driver stage enable: 0 = Enable 1 = Disable

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN65DP141 can be used in Source, Sink, cable and dongle applications, where the device is transparent to the DisplayPort link layer. For illustrating purposes, this section shows the implementation of a DisplayPort dongle, Figure 27 shows an example of the SN65DP141 on a dongle board, where the AUX channel is directly connected from source to sink, meanwhile the power can be provided either way from the DP source or an external power source.

9.2 Typical Application

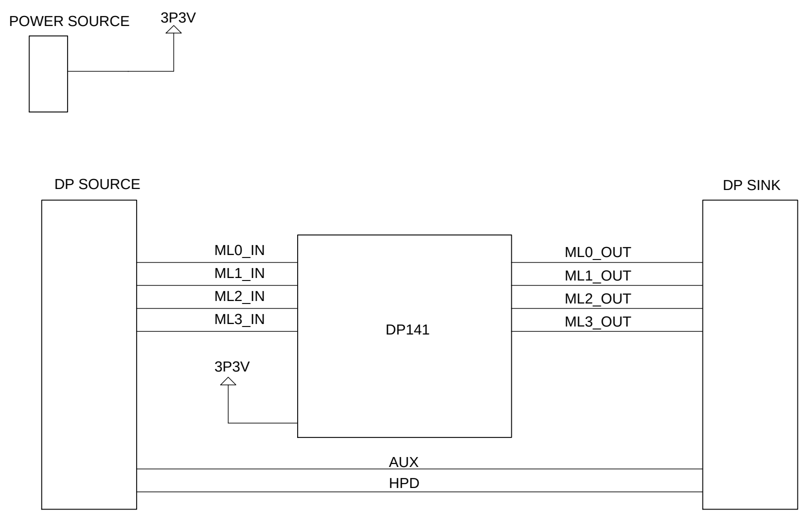


Figure 27. SN65DP141 Application Diagram

9.2.1 Design Requirements

The SN65DP141 can be designed into many types of applications. All applications have certain requirements for the system to work properly. The voltage rails are required to support the lowest possible power consumption. Configure the device by using I2C. The GPIO configuration is provided as I^2C is not available in all cases. Because sources may have different naming conventions, confirm the link between source and sink is correctly mapped through the SN65DP141.

Table 14. Design Parameters

PARAMETER	VALUE
Operating data rate	HBR3 (8.1 Gbps)
Supply voltage	3.3 V
Main link input voltage	V_{ID} = 75 mVpp to 1.2 Vpp
Control pin Low	1 KΩ pulled to GND
Control pin Mid	No Connect
Control pin Low	1 KΩ pulled to High
Main link AC decoupling capacitor	75 to 200 nF, recommend 100 nF

First approach for GAIN configuration: It is highly recommend that DC GAIN be set to 1, this leads the output to preserve the input amplitude (GAIN = 1):

- For GPIO implementation: Use a pull-up resistor on the GAIN terminal (pin 36), refer to the schematic in Figure 28.
- For I²C implementation: write a 1 to the bit 2 of the registers 0x02, 0x05, 0x08 and 0x0B. Refer to *Two-Wire Serial Interface and Control Logic* for a detailed description of the I²C interface

9.2.2 Detailed Design Procedure

Designing in the SN65DP141 requires the following:

- Determine the loss profile on the DP input and output channels and cables.
- Based upon the loss profile and signal swing, determine the optimal configuration for the SN65DP141, to pass electrical compliance (Equalization mode, EQ Gain, DC gain, AC Gain).
- See Figure 28 for information on using the AC coupling capacitors and control pin resistors, as well as for recommended decouple capacitors from VCC pins to ground.
- Configure the TheSN65DP141 using the GPIO terminals or the I²C interface:
  - GPIO – Using the terminals EQ_MODE, EQ1, EQ1 and gain.
  - I²C – Refer to the I2C *Register Maps* and the *Two-Wire Serial Interface and Control Logic* sections for a detailed configuration procedures.
- The thermal pad must be connected to ground.

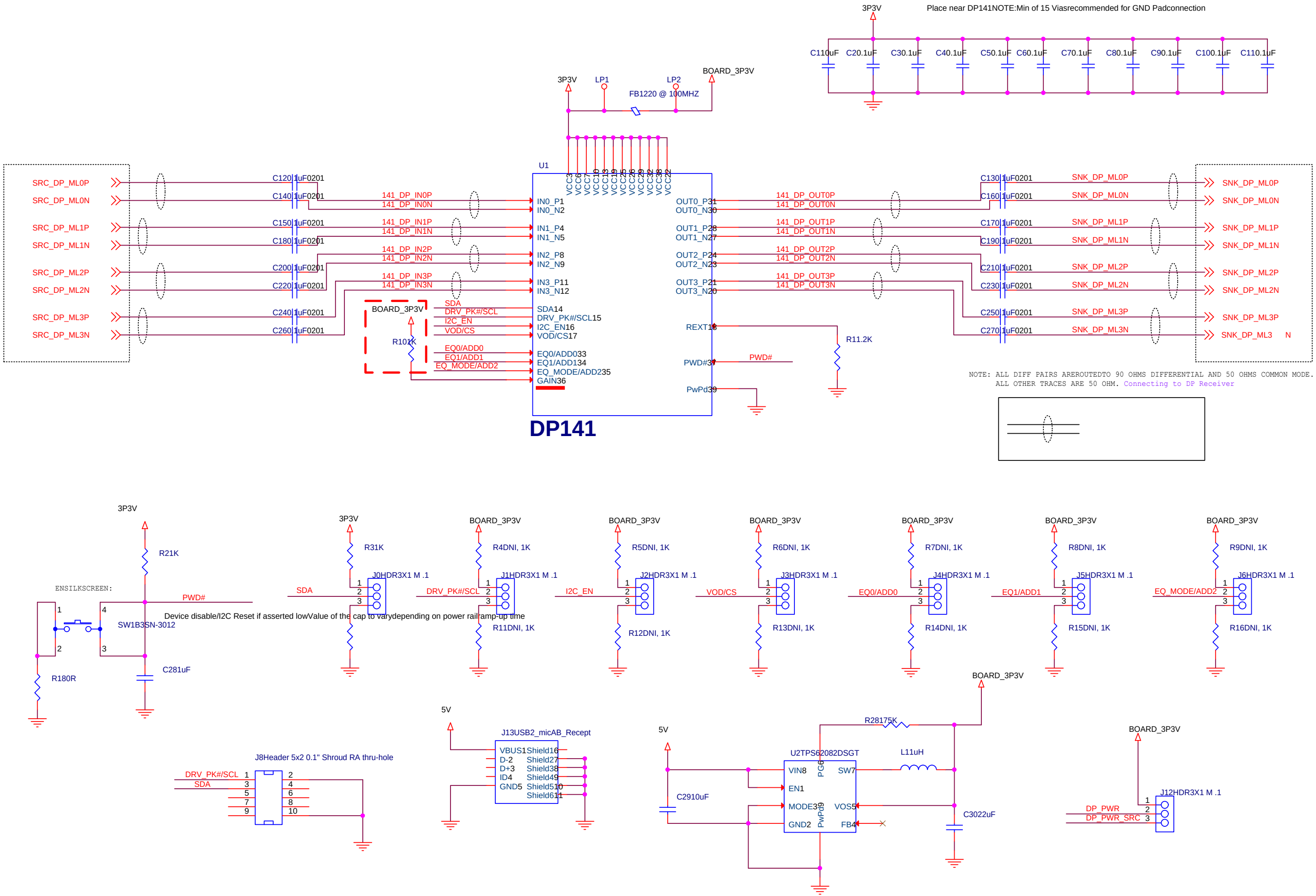
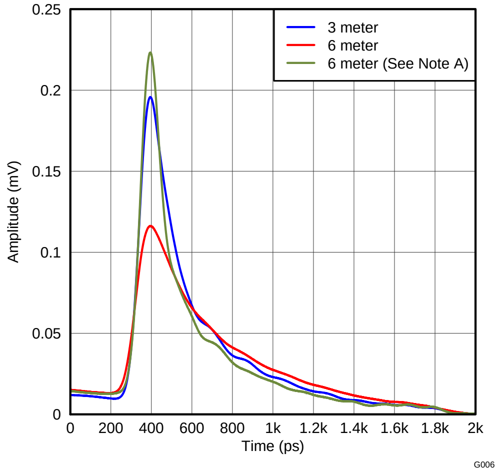


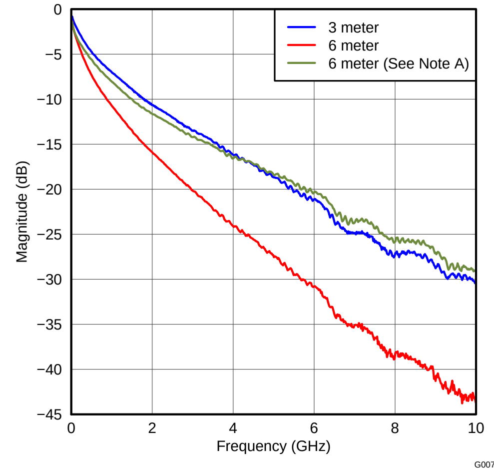
Figure 28. SN65DP141 Application Schematic

9.2.3 Application Curves



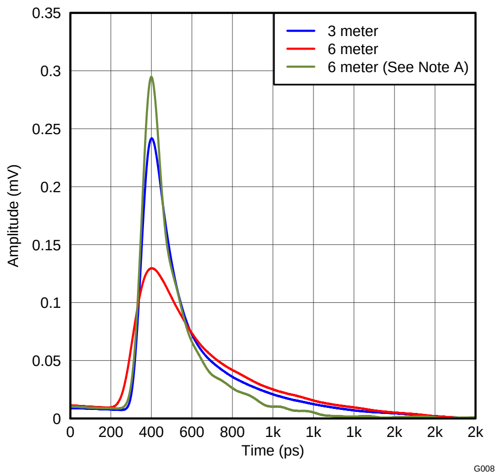
With SN65DP141 -> EQ = 4, VOD = High, ACGain = HiZ, DCGain = Low

Figure 29. Cable Mode – Symbol Response



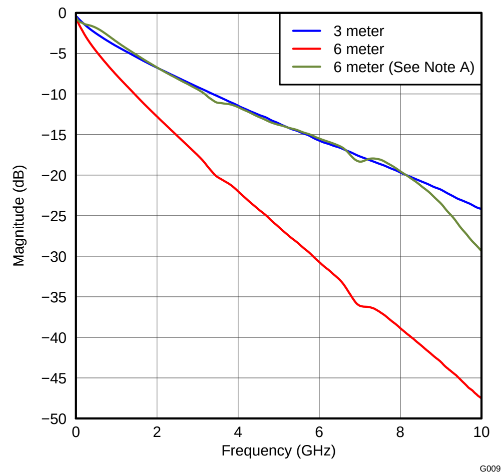
With SN65DP141 -> EQ = 4, VOD = High, ACGain = HiZ, DCGain = Low

Figure 30. Cable Mode – Frequency Domain



With SN65DP141 -> EQ = 7, VOD = High, ACGain = High, DCGain = Low

Figure 31. Trace Mode – Symbol Response



With SN65DP141 -> EQ = 7, VOD = High, ACGain = High, DCGain = Low

Figure 32. Trace Mode - Frequency Domain

10 Power Supply Recommendations

To minimize the power supply noise floor, provide good decoupling near the SN65DP141 power pins. It is recommended to place one 0.01-µF ceramic capacitor at each power pin, and two 0.1-µF ceramic capacitors on each power node. The distance between the SN65DP141 and capacitors should be minimized to reduce loop inductance and provide optimal noise filtering. Placing the capacitor underneath the SN65DP141 on the bottom of the PCB is often a good choice. A 100-pF ceramic capacitor can be put at each power pin to optimize the EMI performance.

11 Layout

11.1 Layout Guidelines

- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high frequency bypass capacitance significantly.
- The control pin pull-up and pull-down resistors are shown in application section for reference. If a high level is needed then only uses the pull up. If a low level is needed only use the pull down.
- Place passive components within the signal path, such as source-matching resistors or ac-coupling capacitors, next to each other. Routing as in case a) creates wider trace spacing than in b), the resulting discontinuity, however, is limited to a far narrower area.
- When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.
- Avoid metal layers and traces underneath or between the pads off the DisplayPort connectors for better impedance matching. Otherwise they will cause the differential impedance to drop below 75 Ω and fail the board during TDR testing.
- Use solid power and ground planes for 100 Ω impedance control and minimum power noise.
- For a multi-layer PCB, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane. For 100 Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.
- Keep the trace length as short as possible to minimize attenuation.
- Place bulk capacitors (that is, 10 μF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.

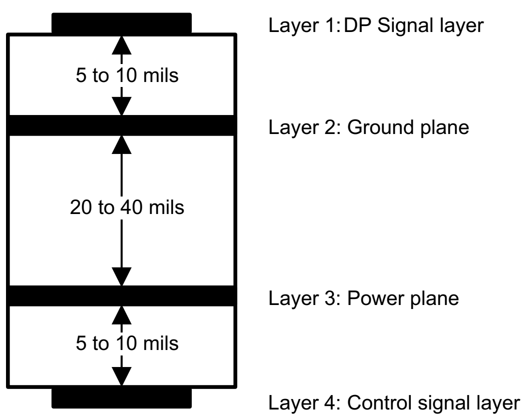


Figure 33. PCB Stack

11.2 Layout Example

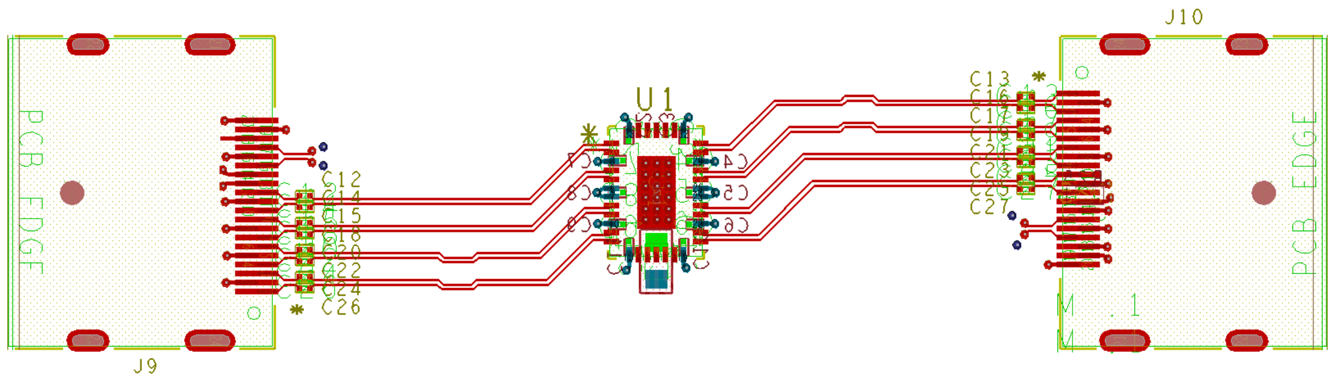


Figure 34. Example Layout (Top)

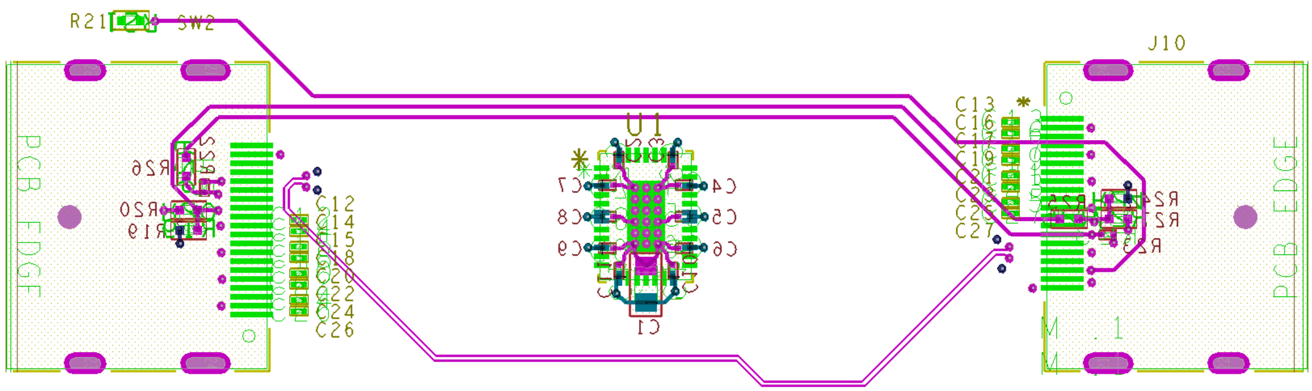


Figure 35. Example Layout (Top)

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65DP141RLJR	ACTIVE	WQFN	RLJ	38	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DP141	Samples
SN65DP141RLJT	ACTIVE	WQFN	RLJ	38	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DP141	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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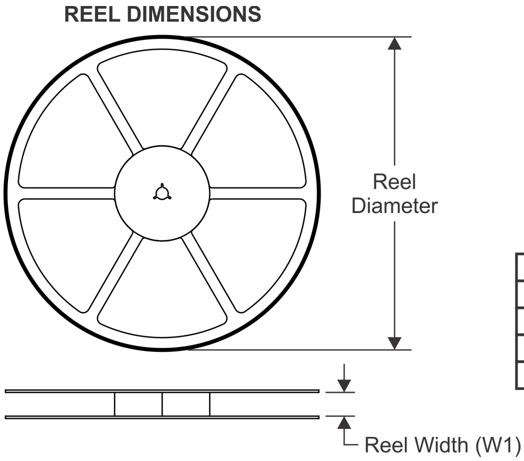
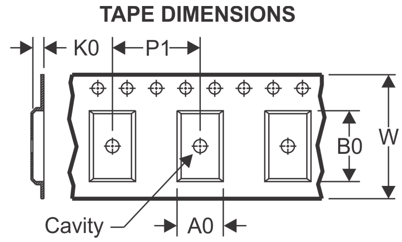
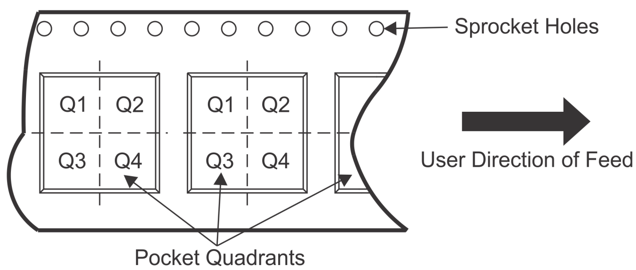
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

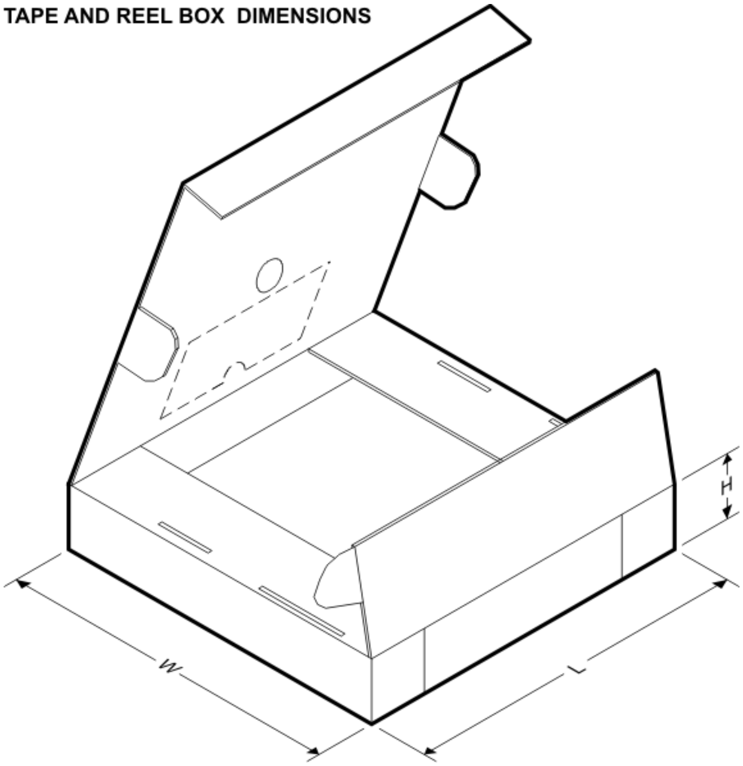
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65DP141RLJR	WQFN	RLJ	38	3000	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1
SN65DP141RLJT	WQFN	RLJ	38	250	330.0	16.4	5.25	7.25	1.45	8.0	16.0	Q1

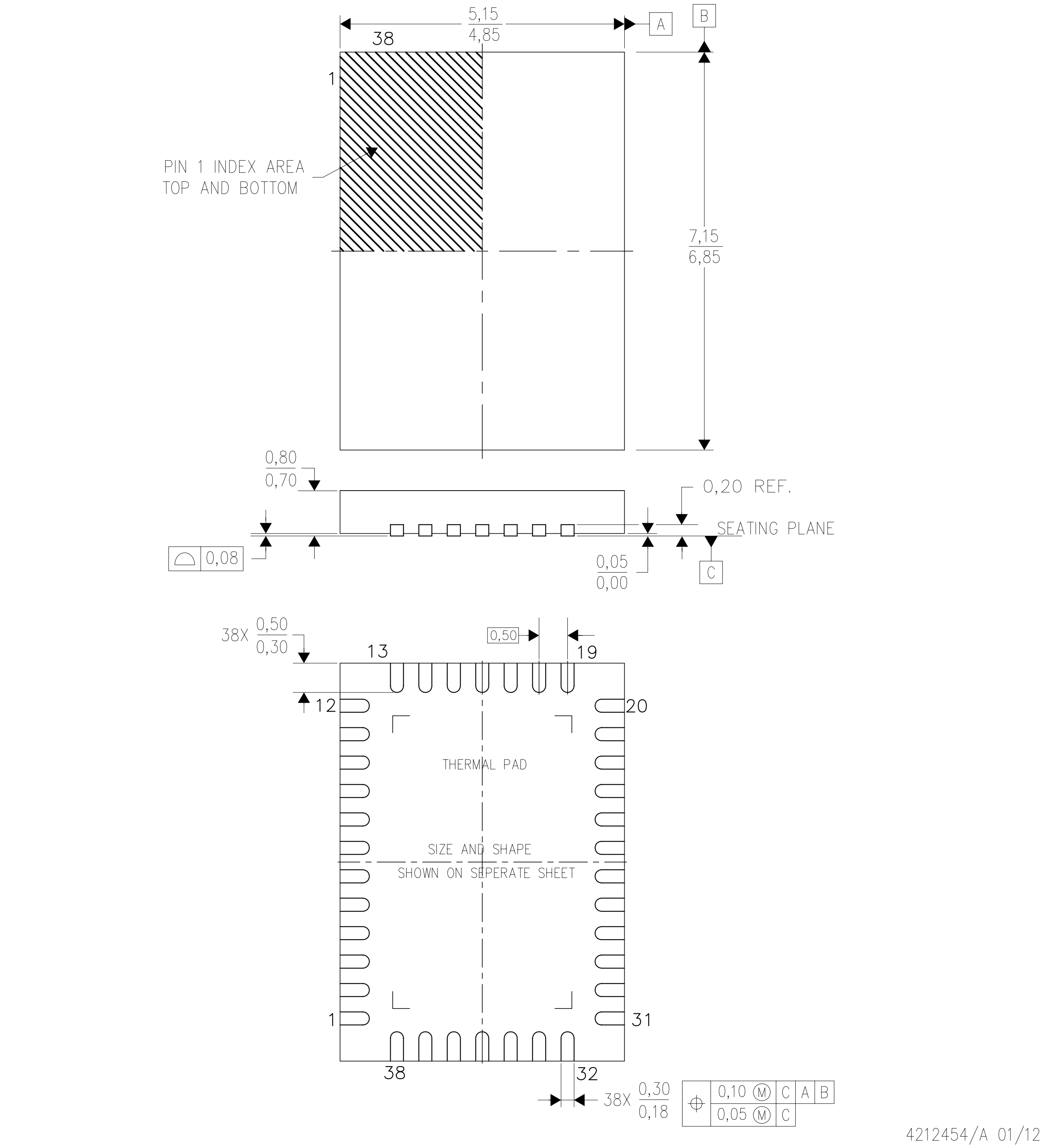
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65DP141RLJR	WQFN	RLJ	38	3000	367.0	367.0	38.0
SN65DP141RLJT	WQFN	RLJ	38	250	367.0	367.0	38.0

RLJ (R-PWQFN-N38) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.

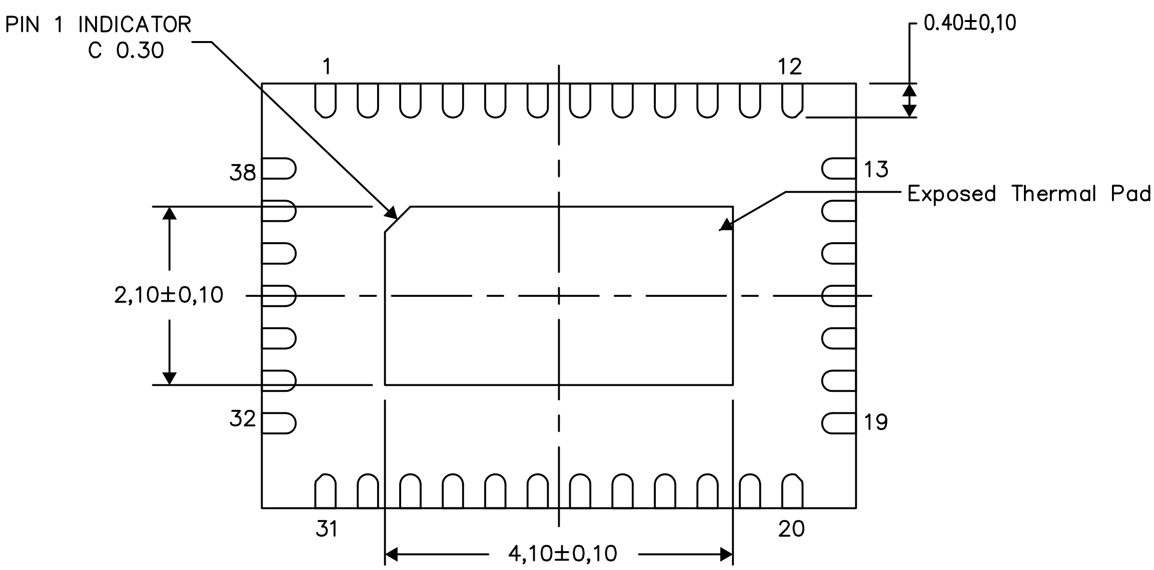
RLJ (R-PVQFN-N38) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



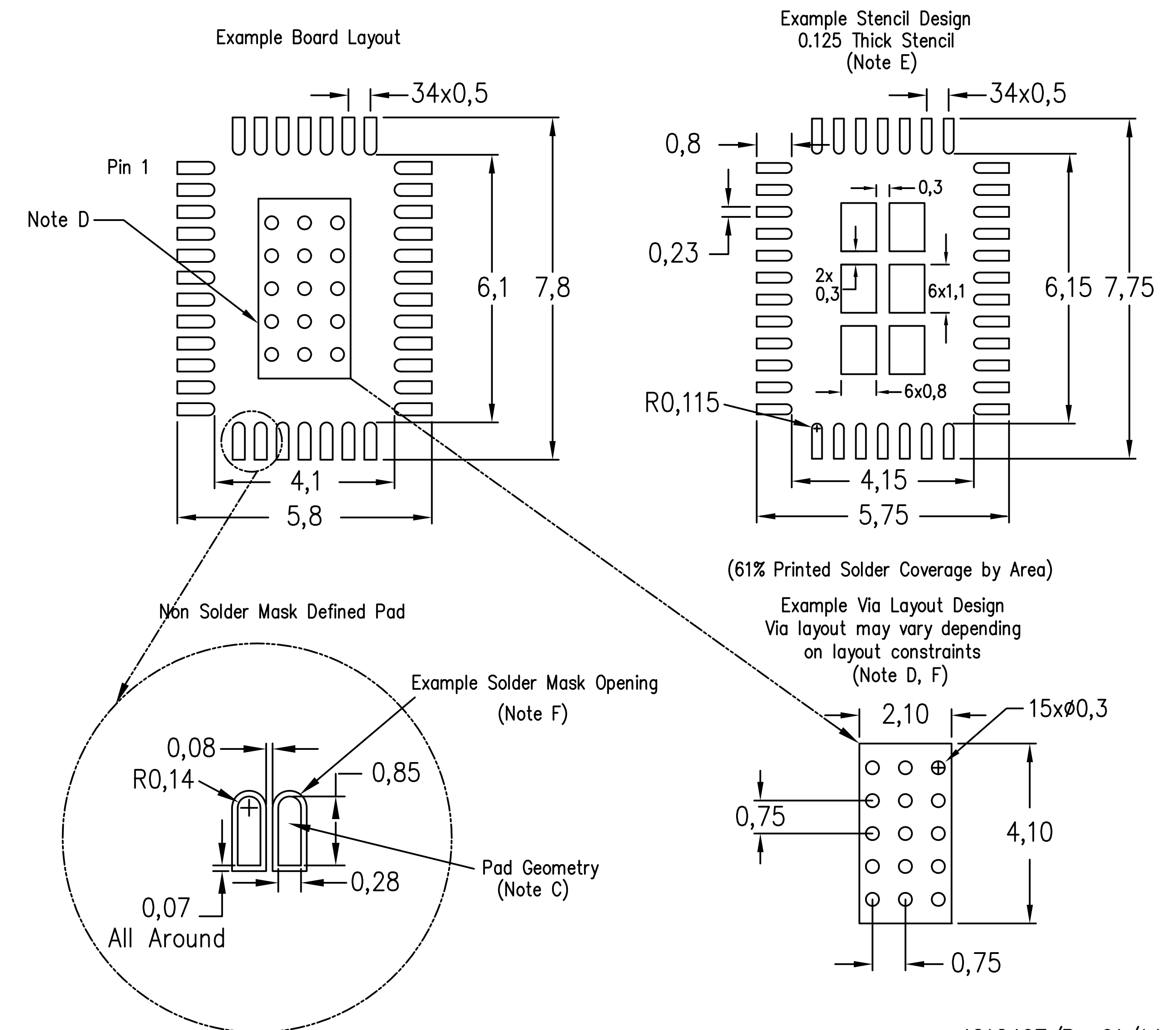
Bottom View

Exposed Thermal Pad Dimensions

4212466/B 01/14

NOTE: All linear dimensions are in millimeters

RLJ (R–PVQFN–N38) PLASTIC QUAD FLATPACK NO–LEAD



4212467/B 01/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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