

## Evaluation Board for the **ADG5404F** Overvoltage Protected 4:1 Mux

### FEATURES

#### Supply voltages

Dual supply:  $\pm 5$  V to  $\pm 22$  V

Single supply: 8 V to 44 V

#### Protected against overvoltage on source pins

Signal voltages up to  $-55$  V and  $+55$  V

#### LED for visual overvoltage indication

#### Parallel interface compatible with 3 V logic

#### On-board low dropout (LDO) regulator for digital supply and control if required

### ONLINE RESOURCES

#### Evaluation Kit Contents

[EVAL-ADG5404F](#)

#### Documents Needed

[ADG5404F](#) data sheet

### EQUIPMENT NEEDED

#### DC voltage source

$\pm 22$  V for dual supply

44 V for single supply

#### Optional digital voltage source: 3 V to 5 V

#### Analog signal source

#### Method to measure voltage, such as digital multimeter (DMM)

### GENERAL DESCRIPTION

This user guide describes the evaluation board for the [ADG5404F](#), which is a 4-channel multiplexer. The [ADG5404F](#) has overvoltage detection and protection circuitry on the source pins and is protected against signals up to  $-55$  V and  $+55$  V in both the powered and unpowered state.

Figure 1 shows the [EVAL-ADG5404FEBZ](#) in a typical setup. The [ADG5404F](#) is soldered to the center of the board and wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals are used to power the device, with a fourth terminal used to provide a user defined digital voltage if required. Alternatively, an LDO regulator is provided for 5 V digital voltage control and to supply the LED, which is mounted to provide visual indication of the fault status of the switch.

### TYPICAL SETUP

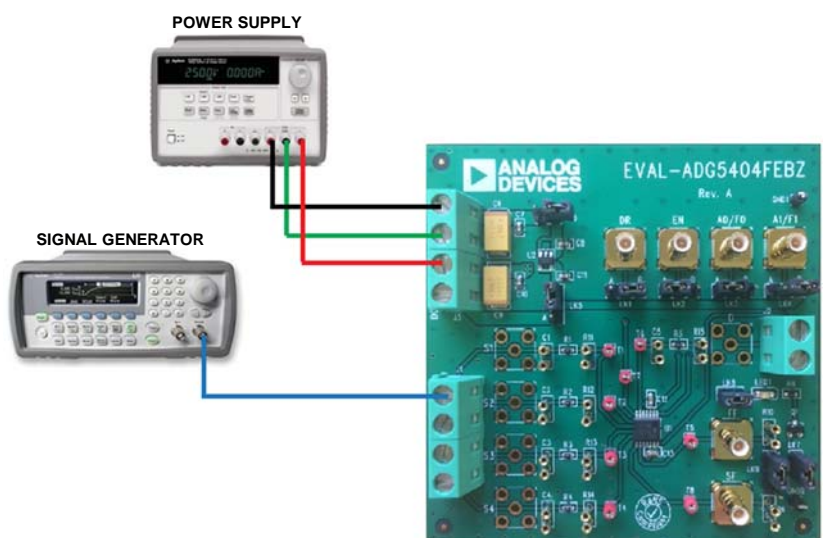


Figure 1. [EVAL-ADG5404FEBZ](#), Power Supply, and Signal Generator

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REVISION HISTORY

2/15—Revision 0: Initial Version



## EVALUATION BOARD HARDWARE

The operation of the [ADG5404F](#) is evaluated using the [EVAL-ADG5404FEBZ](#). Figure 1 shows a typical setup where only a power supply and signal generator are required. Figure 2 shows a block diagram of the main components of the evaluation board.

The connectors on the board pass signals through the [ADG5404F](#) switch. The source pins have fault detection circuitry that reacts to an overvoltage. During an overvoltage event, the switch is turned off and the FF pin is pulled low. The SF pin is pulled low when the source where the overvoltage occurs is the one selected by the A0/F0 and A1/F1 pins. See the [ADG5404F](#) data sheet for further details.

### POWER SUPPLIES

Connector J3 provides access to the supply pins of the [ADG5404F](#). VDD, GND, and VSS link to the appropriate pins on the [ADG5404F](#). For dual supply voltages, power the evaluation board from  $\pm 5$  V to  $\pm 22$  V. For single supply voltages, connect the GND and V<sub>SS</sub> terminals and power the evaluation board with 8 V to 44 V. Additionally, an on-board LDO regulator is provided for digital control voltage. If necessary, connect a secondary voltage source to DC\_V1 and use it as the digital control voltage. To use DC\_V1, place the header of LK5 into Position A.

### INPUT SIGNALS

Two screw connectors are provided to connect to both the source and drain pins of the [ADG5404F](#). Additional subminiature Version B (SMB) connector pads have been laid out if extra connections are required.

The [ADG5404F](#) is overvoltage protected on the source side, and the maximum voltage that can be applied to S1 to S4 is  $-55$  V or  $+55$  V. See the [ADG5404F](#) data sheet for more details.

Each trace on the source and drain side includes two sets of gold pin connectors that are used to place a load on the signal path to ground. A  $0\ \Omega$  resistor is placed in the signal path and

can be replaced with a user defined value. Use the resistor combined with the gold pin connectors to create a simple resistor/capacitor (RC) filter.

The [ADG5404F](#) uses parallel interface channels (A0/F0, A1/F1) to control the operation of the switches. Use the headers on LK2 to LK4 to manually control the operation of the switches, or connect an external controller directly to the control pins by using the SMB connectors, A0/F0, A1/F1, and EN, and removing the link headers on LK2 to LK4.

### OUTPUT SIGNALS

There are two outputs on the [ADG5404F](#). The FF pin indicates when the device is operating normally or whether there is an overvoltage fault on one of the source pins. The SF pin also indicates when an overvoltage occurs on one of the source pins and transitions low only when an overvoltage occurs on the channel selected by the A0/F0 and A1/F1 inputs. For visual indication, an LED is mounted on the evaluation board. Use LK8 to connect the LED circuit. When the device is operating normally, the FF pin remains high and the LED turns on. If an overvoltage occurs at any of the source pins, the FF pin is pulled low and the LED turns off.

The LK9 selector allows the user to choose which output controls the LED. Putting the header on Position A allows the FF pin to control the LED. On Position B, the SF pin controls the LED.

SMB connectors are provided to interface the evaluation board with external controllers, and two gold pin connectors are provided to connect a pull-up resistor between the FF and SF signals and the digital supply.

The DR pin allows the user to choose the state of the drain pin when the device is deactivated during an overvoltage. The LK1 selector allows the user to choose between open circuit and pulling to the rails.

## JUMPER SETTINGS

### LINK HEADERS

Use the link headers to control the [ADG5404F](#) manually, to configure the digital control voltage, and to isolate the LED from the system. Table 2 shows a summary of the link headers and how they are used on the evaluation board.

Use LK3 and LK4 to control the switches of the [ADG5404F](#). Use LK2 to enable or disable the device.

Position A is tied to GND and sets the logic low, whereas Position B is tied to DC\_V1 and sets the logic high.

**Table 1. [ADG5404F](#) Truth Table**

LK2 (EN)	LK3 (A0)	LK4 (A1)	Connected Sx
A	X <sup>1</sup>	X <sup>1</sup>	All switches off
B	A	A	S1
B	B	A	S2
B	A	B	S3
B	B	B	S4

<sup>1</sup> X = don't care.

LK1 allows the user to configure the state of the drain during an overvoltage condition.

LK6 connects the on-board LDO regulator to the  $V_{DD}$  supply. Remove the header to protect the LDO regulator from voltages higher than 28 V or to use an alternative digital control voltage. Change the header on LK5 to Position B to connect to DC\_V1.

LK8 connects the LED to the digital power supply, and LK7 connects the FF or SF pin of the [ADG5404F](#) to the LED.

### SMB CONNECTORS

Control the parallel interface of the [ADG5404F](#) manually using the link headers of LK2 to LK4, or access it using the SMB connectors, A0/F0, A1/F1, and EN. To use the SMB connectors, remove the link headers of LK2 to LK4. Use the FF/SF SMB connectors to access the FF/SF digital outputs from the [ADG5404F](#).

**Table 2. Link Header Descriptions**

Link Header	Position	Description
LK1	A	$V_{DD}$ or $V_{SS}$ during an overvoltage
	B	Open circuit during an overvoltage
LK2	A	All switches off (disabled)
	B	Device enabled (EN pin), switch function set by A0/F0 and A1/F1 pins
LK3	A	Logic 0 on A0/F0 pin
	B	Logic 1 on A0/F0 pin
LK4	A	Logic 0 on A1/F1 pin
	B	Logic 1 on A1/F1 pin
LK5	A	DC_V1 digital voltage
	B	On-board LDO regulator digital voltage
LK6	Inserted	LDO regulator powered up
	Removed	LDO regulator unpowered
LK7	Inserted	FF/SF pins connected to LED
	Removed	FF/SF pins disconnected from LED
LK8	Inserted	LED powered up
	Removed	LED unpowered
LK9	A	FF pin controls the LED
	B	SF pin controls the LED

## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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