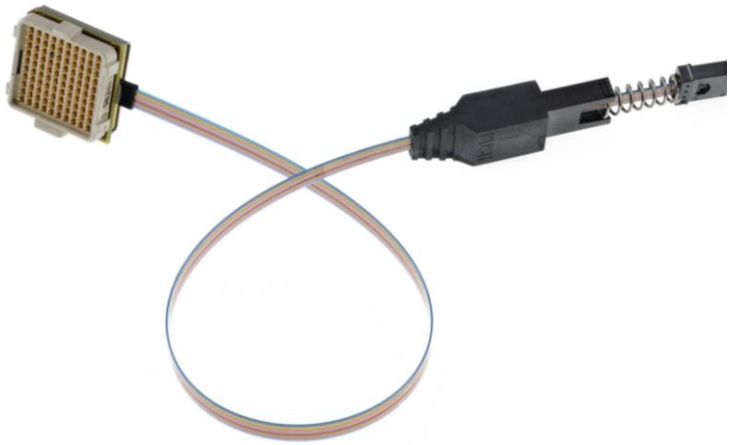
D-Light DLR-xx-251-lw-Pyz-Lv
2 to 12 channels 4.25 Gbps optoelectronic receiver

Features

- Up to 4.25 Gbps per channel
- 2 to 12 independent receivers in a single package
- Each channel complies with IEEE Std. 802.3z Gigabit Ethernet 1000 Base-Sx PMD requirements
- Also suitable for Fibre Channel, Infiniband and VSR-1 requirements
- Qualified over the industrial temperature range [-40;+85°C]
- Standard electrical plug/socket interface
- Small package size (16x16x3mm)
- Pigtailed optical connectics
- Low power consumption
- Single 3.3 V power supply



Applications

- Sensors interconnects
- Numerical video transmission
- Board-to-board communications
- Severe environment interconnects
- Space application

Product Description

D-Light DLR-xx-251-lw-Pyz-Lvv parallel optoelectronic modules receive high data rate signals on either 2, 4, 8 or 12 independent channels. They are optimized for short distance high data rate optical communications on multimode fiber ribbon and fully comply with ARINC804 Standard. They are protocol independent and can be applied to Gigabit Ethernet (both 1GBE and 10 GBE), Fibre Channel, Infiniband or any specific communication application in the qualified temperature range [-40;+85°C].
DLR-xx-251-lw-Pyz-Lvv modules integrate state-of-the art GaAs PIN photodiode arrays and are optimized for low power consumption (<125 mW for each receiver channel).
DLR-xx-251-lw-Pyz-Lvv are available in various package such as surface mount or pluggable ones and various multimode fiber ribbon pigtail termination are offered around the standardized MT ferrule.

Ordering Information

Several versions of D-Light optoelectronic receivers are currently available. All use 50/125 or 62.5/125µm fiber ribbon cables.

DLR-xx-251-lw-Pyz-Lvv

- vv : Pigtail Length
  - Length in cm (see page15 for details)
- z : Fibres diameter
  - 1 ↔ 50/125µm Bare fibre ribbon
  - 2 ↔ 62.5/125µm Bare fibre ribbon
- y : Connector type
  - O ↔ MPO connector
  - X ↔ MPX connector
  - T ↔ MTP connector
  - N ↔ No connector (MT ferule only)
  - M ↔ MT ferule plus spring
- w : Packaging option
  - L ↔ 48-Pin LCC package
  - GM↔ 100-Pin Meg-Array socketed package
- xx : number of channel
  - 02 ↔ 2 channels
  - 04 ↔ 4 channels
  - 08 ↔ 8 channels
  - 12 ↔ 12 channels

DATASHEET

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Absolute Maximum Ratings

Stress beyond the values stated below may cause permanent damage to the device.

Parameter	Symbol	Min	Max	Unit	Notes
Storage temperature	T_{st}	-55	+125	°C	-
Soldering temperature	T_{sol}	-	230	°C	-
Soldering time	t_{sol}	-	60	s	-
Supply voltage	V_{CC}	-0.3	+4.0	V	-
Signal pins voltage range	V_{pin}	V_{EE}-0.3	V_{CC}+0.3	V	-
Junction temperature	T_j	-	130	°C	-
ESD resistance voltage	ESD	-	1	KV	-

Notes:

1. Human Body Model (HBM) according to JESD22-A114-B.

Module specifications – General

VCC =3.3V, VEE=GND= 0V

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply voltage		V_{CC}	3.0	3.3	3.6	V	-
Supply voltage noise		N_{VCC}	-	-	100	mV	1
Supply current		I_{CC}	-	xx•35	xx•42	mA	2
Power supply noise rejection		PSR	-	-	15	dB	-
Power consumption	12 channels	P_{tot}		xx•125	xx•150	mW	2
	Per channel	P_{ch}	-	-	125	mW	2
Rx enable/disable voltage	Disabled	V_{dis}	0	-	0.8	V	3
	Enabled	V_{en}	V_{CC}-1.3	-	V_{CC}	V	3
Data rate per channel		B	0.01	2.5	4.25	Gbps	4
Qualified temperature		T_{op}	-40	-	+85	°C	5

Notes:

1. For noise frequencies < 10MHz
2. xx represents the number of channel. Power consumption per Rx channel operating at full speed.
3. The module is normally enabled (i.e. when the RxEnable control input is not connected).
4. Bit rate of 4.25Gbps can be achieved with an optical input sensitivity reduced to –15 dBm typ.
5. Module operates over [-55;+100°C] with limited degraded performances.

Module specifications – Electrical

VCC_x =3.3V, VEE_x=GND_x= 0V, Temp = [-40;+85°C]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Number of channels		N_{ch}	4	-	12	-	-
Differential output voltage		V_{OUTpp}	250	300	400	mV	-
Output stage power supply range		V_{OREF}	1.8	-	V_{CC}	V	1
Output impedance		Z_{out}	80	100	120	Ω	-
Channel crosstalk penalty		X_{Popt}	-	1	2	dB	2
Link Monitor Output	High	V_{OH}	2.4	-	V_{CC}	V	3, 4
	Low	V_{OL}	0	-	0.5	V	3, 4
Total jitter receiver		T_J	-	-	150	ps	5
Rise/Fall time		τ_R, τ_F	40	-	120	ps	5
Rx electrical power consumption (1 ch.)		P_{Rx}	-	125	150	mW	-

Notes:

1. Output stage complies with CML 3.3 to 1.8V standards. See description for details.
2. For adjacent channels in worst case at full speed (one channel at sensitivity & adjacent channel at saturation), squelch function OFF.
3. Compatible with LVTTL/CMOS digital level specifications.
4. The Link Monitor circuit monitors the incoming optical signal level and generates a logic LOW signal when insufficient photocurrent is produced (see detailed description below).
5. Measured at 1.25Gbps and with 20% / 80% levels.

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Module specifications - Optical

VCCx=3.3V, VEE= 0V, Temp = [-40;+85°C]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Center wavelength		λ_C	760	850	860	nm	-
Spectral width – rms		$\Delta\lambda$	-	-	1	nm	-
Core diameter of the Rx optical fiber pigtail		D_C	50	-	62.5	µm	-
Optical sensitivity	1.25 Gbps	P_{in}	-	-18	-17	dBm	1
	2.5 Gbps		-	-17	-16	dBm	1
	4.25 Gbps		-	-16	-15	dBm	1
Optical modulation amplitude		OMA	50	-	-	µW	-
Optical return loss		ORL	-30	-	-	dB	-
SDx optical sensitivity	SDx = High	$P_{optTh}(H)$	-19.2	-18	-16.5	dBm	2
	SDx = Low	$P_{optTh}(L)$	-22.2	-21	-19.2	dBm	2
Signal Detect volatge	Normal	$V_{SD\ Norm}$	V_{CC}-0.5	-	V_{CC}	V	3
	Fault	$V_{SD\ Fault}$	V_{EE}	-	V_{EE}+0.5	V	3

Notes:

1. For BER=10^{-12} measured at the specified bit rate with a 2^7-1 PRBS signal
2. Assuming a receiver sensitivity of 0.5A/W.
3. Signal Detect is LVTTL. Logic "1" indicates normal operation; logic "0" indicates no signal is detected.

Functional block diagram

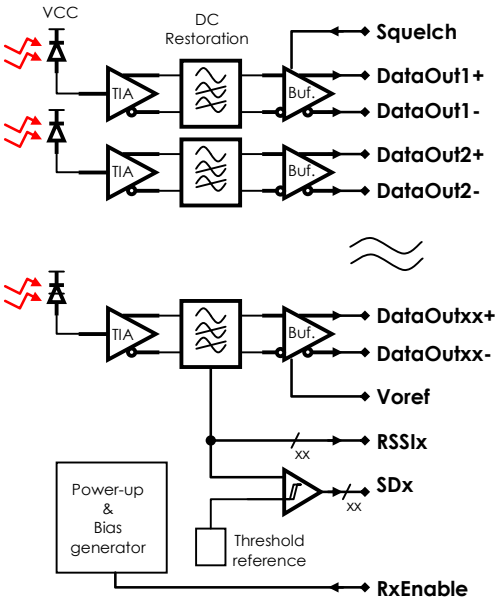

Figure 1 - DLR-xx-251-Iw-Pyz-Lvv block schematic

D-Light DLR-xx-251-Iw-Pyz-Lv
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Description

General

DLR-xx-251-Iw-Pyz-Lvv modules are optimized for high speed DC-coupled serial links: the maximum bit rate is up to 4.25Gbits/s/ch. The module is 3.3 Volts single supplied for low power consumption. The module dimensions are 16×16×3 mm.
DLR-xx-251-Iw-Pyz-Lvv modules are based on high speed GaAs photodiode arrays and on high performances BiCMOS transimpedance (TIA) and limiting (LA) amplifiers arrays. The signal path is AC-coupled and allows 2R (reshape and reclock) recovery.

Several features allow a large range of applications.

- LVCMOS input compatible Run/shutdown commands permit low power consumption.
- Analog inputs & outputs monitor each channel state and performance.

Receiver controls

The following input/output pins permit a complete monitoring of the module:

- **RxEnable**. All receiver channels can be disabled by pulling down the enable input pin.
- **Receiver Strengh Signal Indicator** (RSSIx). Each DC/low-frequency output RSSIx sources a current proportional to the average input photocurrent of the considered photodiode.
- Link Monitors or **Signal Detect** (SDx). Each Signal detect output indicates a presence or a loss-of signal. When peak to peak photocurrent is below the sensitivity limit of the circuit.
- **Squelch**: this digital input pin enables the squelch function.

Detail description

The receiver part of the DLR-xx-251-Iw-Pyz-Lvv module is based on high speed GaAs photodiode array and high performances BiCMOS transimpedance (TIA) and limiting (LA) amplifiers array. Some input and output signals have been added to the design for complete controlling of the module (in particular a link monitor with a threshold selector has been added to comply with standard specifications SDH STM-16).

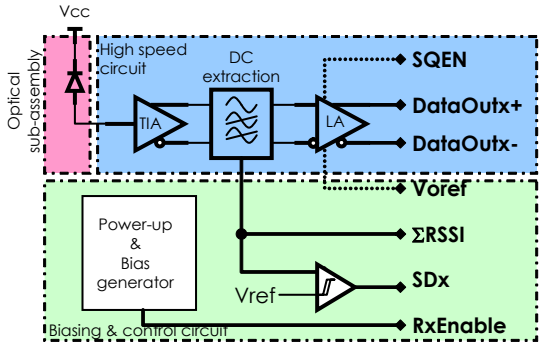

Figure 2 - Receiver bloc diagram (1ch)

The signal path is AC-coupled and allows 2R (reshape and reclock) recovery. The minimum lower cut-off frequency is dependent on the pattern spreading but can be as low as 100KHz. This circuit is therefore compatible with data rates ranging from 10Mbps to 4.25 Gbps.

Photodiode input stage

The photodiode input stage is a differential transimpedance amplifier with high sensitivity that operates with input current as low as $12\mu A_{pp}$. Typical photodiode sensitivity at 850nm is 0.6A/W: the optical sensitivity is therefore as low as –18dBm (@1.25Gbps). The amplifier incorporates a compensation capacitor.

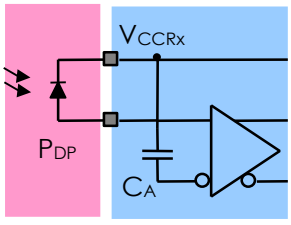

Figure 3 - Photodiode input stage

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Data Output stage

The output stage is a differential current-mode-logic (CML) driver (cf. Figure 4). The pull-up resistors are tied to a separated supply pin V_{OREF} which, according to the applied voltage, allows the stage to be compatible with LVDS level. Provided the load impedances at the two outputs are matched, the switching noise can be minimized. The general characteristics of the output stage are the following (See application note for usage):

- Switched current I_0 of 9mA,
- pull-ups R_{OL} 2x50Ω to V_{OREF}.
- A squelch function is implemented to turn off the output stage when no input power is detected.
- Free choice of V_{OREF} and 50Ω load resistor connection, as long as operating conditions are fulfilled.
- Only a small amount of noise is generated on V_{OREF} and GND.
- Output swing selectable (SWS pin).

For differential DC-coupled termination with negative power supply (V_{CC} and V_{OREF} should be connected to ground and GND to the negative supply): The outputs are then connected to 50Ω tracks, terminated by two 50Ω loads to ground, or a floating 100Ω load.
For single-ended AC-coupled : both outputs should see equal load impedances.
For LVDS-level compatibility : V_{OREF} should be tied to VEE_{RX}+2.4V. The resulting levels are then compatible with an IEEE P1596.3 LVDS input stage.

VOREF voltage range allows compatibility with CML common mode voltage from 1.8V to 3.3V.

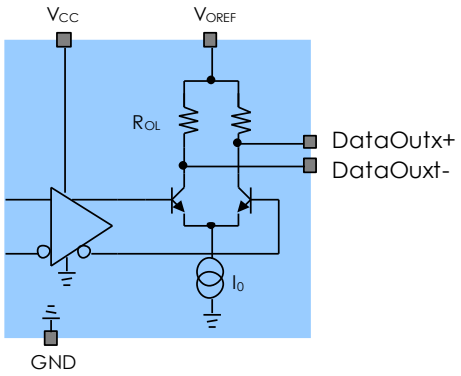

Figure 4 - Data output stage

The output stage is equipped with a squelch function that turn off the output stage when the input optical power of the corresponding channel is below a threshold (typically -18dBm). In addition to this function a Swing Size (SWS pin) select feature is implemented to increase the size of output swing as a Pre-emphasis feature (PE[2:0] pins).

Receiver controls

Note that all the receiver controls are not available for all the module package option. We describe hereafter all the receiver controls available (accessible in the IGM option : 100-pin Meg-Array socket).

- **Receiver Signal Strength Indicator (RSSIx):** the DC/low-frequency outputs source a current proportional to the average input photocurrent (internally loaded by a Resistor to provide a Voltage output) of the corresponding channel provided that V_{RSSIx} is within the operating range specified (V_{RSSIx}≤ 2.0 V) to obtain best linearity (see receiver characteristics table). This output can be used to monitor the optical power incident on the photodiode. It may be left open if not used. The upper corner frequency of the output is equal to the roll-on frequency f_{Low} of the high-speed data path (Figure 5 & Receiver characteristics table).

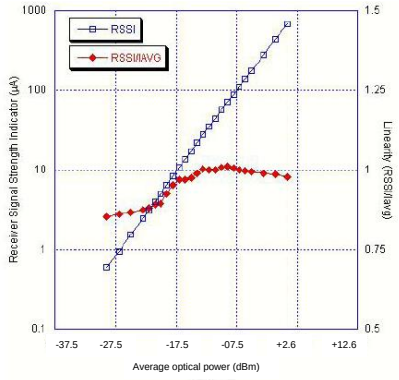

Figure 5 - Typical average monitor current and RSSI voltage (one channel)

Receiver incident optical power computation

The voltage at $RSSI_x$ output pin is proportional to the input optical power of the receiver thought the following equation:

$$RSSI_x = \frac{1}{k} \cdot \frac{R_{ext} \times 10000}{R_{ext} + 10000} \cdot P_{opt} \quad \rightarrow \quad Popt = k \cdot RSSI_x \cdot \frac{R_{ext} + 10000}{R_{ext} \times 10000} \text{ (µW)}$$

Where R_{ext} is the resistor attached to $RSSI_x$ pin, k a internal coefficient and P_{opt} the incident receiver optical power in µW. Note that linearity is maintained for RSSI ≤ 2.0V. RSSI accuracy is depending to the accuracy value of the internal k coefficient.

	Symbol	Min.	Typ.	Max.
Internal coefficient for RSSI	k	-20%	2	+20%

- Signal Detect: The signal detect circuitry is available for each channel. The circuitry compares the average current of a channel to the threshold current. If it is below the threshold, the signal detect condition is de-asserted. A hysteresis function of greater than 1dB prevents chattering of the signal detect signal. The channel level signal detect pads (SDx) are open drain outputs with weak pull-ups.

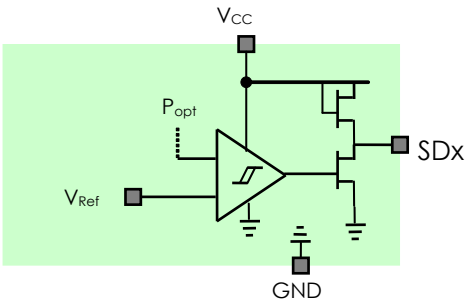

Figure 6 - Link monitor output stage

- Squelch (**SQS**): this digital input pin enables the squelch function i.e. the data outputs of the corresponding channel are set to "0" when Signal Detect signals are asserted (no sufficient P_{opt}).
- **RxEnable**: the receiver side of the module can be disabled by pulling down the RxEnable input pin.
- Swing Size Select (**SWS**): This function is used to increase the size of the output swings. When SWS is high, the output voltage swing (differential, pp) is set to a min. value of 500mV with a max. value of 800mV (+400mV to -400mV). These values correspond to the single ended swings of 250 and 400mV. When SWS is low, the voltage swing is increased by approximately 50%. The output voltage swing (differential, pp) is set to min. 750mV and a max. 1100mV (+550mV to -550mV). These values correspond to the single ended voltage swings of 375mV and 550mV.
- The common mode level (**VOREF**) of the output is adjustable in order to interface to different kind of logic levels (LVDS for examples).
- Pre-emphasis Control (**PE[2:0]**): The Pre-emphasis technique is used to partially negate the effect of high frequency attenuation of signals traveling through PCB due to skin effect and dielectric loss. Pre-emphasis increase the high frequency component of a pulse by re-shaping it. The pre-emphasis scheme emphasizes the high frequency components to P_1 during the t_0 period of the bit transition. When there is no switching in subsequent bit period, the voltage level stays at P_0. The T_0 value is tuned towards operation at 3.125Gbps. Lower data rate will not require pre-emphasis.

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The amount of pre-emphasis that is needed is highly dependent on the characteristics of the trace. The designer will need to set the pre-emphasis based on the actual measurements from the board. There are seven different settings for pre-emphasis and one setting to turn-off the function (PE[2:0]=000).

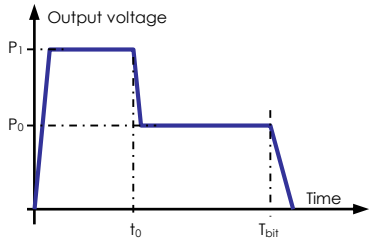

Figure 7 - Pulse shape with pre-emphasis

PE[2:0]	P_0	P_1
000	300mV	0mV
001	280mV	20mV
010	-	-
011	230mV	100mV
100	-	-
101	200mV	200mV
110	-	-
111	150mV	250mV

Pre-emphasis will increase the power consumption of the module. Pre-emphasis can only be used with SWS=1. Using it with SWS=0 lowers the long term reliability of the module.

Power supply noise rejection

Even though bypass capacitors are integrated inside the module, additional filtering can reduce the noise penalty above 10 MHz. For a supply noise V_{PSN} = 100 mV_{PP} a 0.5 dB sensitivity penalty can be reached over the whole frequency range by using a first order low-pass filter with f_c = 10 MHz on the power supply. See figure 8 for a typical power supply filter.

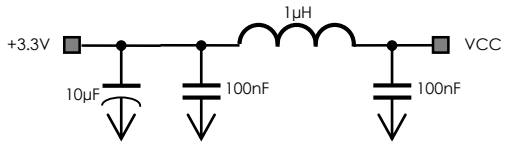

Figure 8 - Typical power supply filter

Module power supplies (VCC and VOREF) should be correctly filtered in order to sufficiently reject the digital noise produced by the output stage on the VOREF power supply rail from the analog power supply rail (VCC). A 15dB rejection ratio between VCC and VOREF is recommended.

The previous proposed filter could be used on both VCC and VOREF rails, assuming the decoupling caps are RF ones.

Memory Mapping

The module memory is mapped in one memory area. The memory is accessible through a common 2-wire serial interface. The following figure details the module memory organization.

Function	Index	D7	D6	D5	D4	D3	D2	D1	D0
Link Monitor 1	0x00	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1
Link Monitor 2	0x01	X	X	X	X	SD12	SD11	SD10	SD9
Channel Powerdown 1	0x02	DIS8	DIS7	DIS6	DIS5	DIS4	DIS3	DIS2	DIS1
Channel Powerdown 2	0x03	X	X	X	X	DIS12	DIS11	DIS10	DIS9
Pre-emphasis Ch 1 and 2	0x04	X	X	PECH2[2]	PECH2[1]	PECH2[0]	PECH1[2]	PECH1[1]	PECH1[0]
Pre-emphasis Ch 3 and 4	0x05	X	X	PECH4[2]	PECH4[1]	PECH4[0]	PECH3[2]	PECH3[1]	PECH3[0]
Pre-emphasis Chl 5 and 6	0x06	X	X	PECH6[2]	PECH6[1]	PECH6[0]	PECH5[2]	PECH5[1]	PECH5[0]
Pre-emphasis Chl 7 and 8	0x07	X	X	PECH8[2]	PECH8[1]	PECH8[0]	PECH7[2]	PECH7[1]	PECH7[0]
Pre-emphasis Ch 9 and 10	0x08	X	X	PECH10[2]	PECH10[1]	PECH10[0]	PECH9[2]	PECH9[1]	PECH9[0]
Pre-emphasis Chl 11 and 12	0x09	X	X	PECH12[2]	PECH12[1]	PECH12[0]	PECH11[2]	PECH11[1]	PECH11[0]
Vendor ID code 1	0x0A	M7	M6	M5	M4	M3	M2	M1	M0
Vendor ID code 2	0x0B	X	X	X	X	X	M10	M9	M8
Global Link Monitor	0x0C	X	X	X	X	X	X	X	SD_ALL
Increment mode	0x0D	X	X	X	X	X	X	X	NOTINCR

Figure 9 - DLR-xx-251-Iw-Pyz-Lvv memory organization

Note: the I2C interface could not be use in conjunction with the JTAG interface. Disable JTAG before using the I2C by pulling low the TRSTn pin.

Receiver memory description

The receiver memory is accessible only in R/W. The receiver memory responds to address $(1010010)_b$ or $(52)_h$ and $(1010011)_b$ or $(53)_h$.

Receiver memory

Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
00	SRAM	R	N/A	Link Monitor Register #1	The bit indicates the signal detect status. When the bit is set, it indicates that the peak to peak input current is above the threshold I_{thSD}. When the bit is cleared, the signal level is below the threshold. There is a hysteresis circuit to avoid chatter on this signal. These bits do not latch the outputs and are an instantaneous indication of the signal levels. 7 … 0 SD 8 | SD 7 | SD 6 | SD 5 | SD 4 | SD 3 | SD 2 | SD 1
01	SRAM	R	N/A	Link Monitor Register #2	Link Monitor register for channel 9 to 12. 7 … 0 Res | Res | Res | Res | SD 12 | SD 11 | SD 10 | SD 9 Res : Reserved

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Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
02	SRAM	R/W	N/A	Channel Power Down #1	The Channel Disable bits are used to disable individual channels. The transimpedance amplifier stage, the limiting amplifier and the CML output stage for the specific channel are turned off to reduce power consumption. When the channel is disabled, the CML outputs are both at the VOREF level and the signal detect for the channel is high. When the bit is cleared, the channels will operate according to RUN and SEL12. When RUN is low, it overrides this register and disables all channels. When RUN is high, the channels (subject to SEL12 settings) with channel disable set are powered down. 7 … 0 DIS 8 | DIS 7 | DIS 6 | DIS 5 | DIS 4 | DIS 3 | DIS 2 | DIS 1
03	SRAM	R/W	N/A	Channel Power Down #2	The Channel Disable bits for channel 9 to 12. 7 … 0 Res | Res | Res | Res | DIS 12 | DIS 11 | DIS 10 | DIS 9 Res : Reserved
04	SRAM	R/W	00	Pre-emphasis Register for channel 1 & 2	The three bits are used to set the level of pre-emphasis used for each channel. The default value on power up has pre-emphasis off. When the value of the register is set to a high value $(111)_b$, the amount of high frequency component being added to the bit is the maximum value for the circuits. For each register, pre-emphasis settings for two channels can be made. 7 … 0 Res | Res | PE2 [2] | PE2 [1] | PE2 [0] | PE1 [2] | PE1 [1] | PE1 [0] Res : Reserved
05	SRAM	R/W	00	Pre-emphasis Register for channel 3 & 4	7 … 0 Res | Res | PE4 [2] | PE4 [1] | PE4 [0] | PE3 [2] | PE3 [1] | PE3 [0] Res : Reserved
06	SRAM	R/W	00	Pre-emphasis Register for channel 5 & 6	7 … 0 Res | Res | PE6 [2] | PE6 [1] | PE6 [0] | PE5 [2] | PE5 [1] | PE5 [0] Res : Reserved
07	SRAM	R/W	00	Pre-emphasis Register for channel 7 & 8	7 … 0 Res | Res | PE8 [2] | PE8 [1] | PE8 [0] | PE7 [2] | PE7 [1] | PE7 [0] Res : Reserved
08	SRAM	R/W	00	Pre-emphasis Register for channel 9 & 10	7 … 0 Res | Res | PE10 [2] | PE10 [1] | PE10 [0] | PE9 [2] | PE9 [1] | PE9 [0] Res : Reserved
09	SRAM	R/W	00	Pre-emphasis Register for channel 11 & 12	7 … 0 Res | Res | PE12 [2] | PE12 [1] | PE12 [0] | PE11 [2] | PE11 [1] | PE11 [0] Res : Reserved

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Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
0A	SRAM	R/W	5F	ID Code 1 Register	These bits are used for the identification code (ID Code). The 11 bits are split into two registers. These registers can be written and read. 7 … 0 M7 M6 M5 M4 M3 M2 M1 M0 The default reads (00101011111).
0B	SRAM	R/W	01	ID Code 2 Register	The ID Code 2 Register contains the most significant bits of the vendor code. 7 … 0 Res Res Res Res Res M10 M9 M8 The default reads (00101011111).
0C	SRAM	R/W	N/A	Global Signal Detect Register	Only the LSB bit is valid and corresponds to SD_All. The SD_All bit is a logical AND of the signal detect of all channels. When it is high, all channels are registering signal level above I_{thSD}. When it is low, one or more channels have signal level below I_{thSD}. This SD_ALL bit is not latched.
0D	SRAM	R/W	x0	Increment Mode Register	The LSB bit of this register is used to enable the auto-increment mode. When the bit is set, the auto-increment mode is disabled. All other bits are not used.

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2-Wire data transfer operation

The 2-wire serial port interface supports a bi-directional data transmission protocol with device addressing (Default address is 1010010_b). A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DLR-xx-251-Iw-Pyz module operates as a slave on the 2-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCLc or SCLd (when present). Timing diagrams for the 2-wire serial port can be found in Figures "2-wire data transfer protocol" and "2-wire data transfer protocol". Timing information for the 2-wire serial port is provided in the following table.

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line from HIGH to LOW while the clock is HIGH defines a START condition.

Stop data transfer: A change in the state of the data line from LOW to HIGH while the clock line is HIGH defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line can be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Figures 12 and 13 detail how data transfer is accomplished on the 2-wire bus. Depending upon the state of the R/W bit, two types of data transfer are possible.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. Within the bus specifications a regular mode (100kHz clock rate) and a fast mode (400kHz clock rate) are defined. The SLM module works in both modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the SLM module slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

1. Data transfer from a master transmitter to a slave receiver. The first byte transmitted by the master is the command/control byte. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
2. Data transfer from a slave transmitter to a master receiver. The master transmits the first byte (the command/control byte) to the slave. The slave then returns an acknowledge bit. Next, follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a 'not acknowledge' can be returned.

The master device generates all serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The DLR-xx-251-Iw-Pyz-Lvv module may operate in the following two modes:

1. Slave receiver mode: Serial data and clock are received through SDA and SCLc or SCLd, respectively. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave (device) address (default address is 000) and direction bit. Slave transmitter mode: The first byte is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DLT module, while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.
2. Slave Address: Command/control byte is the first byte received following the START condition from the master device. The command/control byte consists of a 4-bit control code. For the SLM module, this is set as ***1010*** binary for read/write operations. The next 3 bits of the command/ control byte are the device select bits or slave address. When reading or writing the SLM module, the device-select bits must match the device-select pins. The last bit of the command/control byte (R/W) defines the operation to be performed. When set to a 1, a read operation is selected, and when set to a 0, a write operation is selected.

Following the START condition, the DLR module monitors the SDA bus checking the device type identifier being transmitted. Upon receiving the ***1010*** control code, the appropriate device address bits (default address is 010), and the read/write bit, the slave device outputs an acknowledge signal on the SDA line.

Module Address Presets

The modules are delivered with two in-fab predefined device addresses selectable through the **Module Serial Interface Address Selection pin (SERADD):** The Serial Address pad selects the slave address of the serial interface that the device will respond to. When the input is low, it will respond to 7 bits address: **$(1010010)_b$**. When the input is high, it will respond to 7 bits address: **$(1010011)_b$**.

The SERADR can be changed only when there are no transactions on the serial interface.

Note that the I2C interface is only accessible when the JTAG interface is disabled (TRTn pin set to 0).

2-Wire data transfer protocol and chronograms

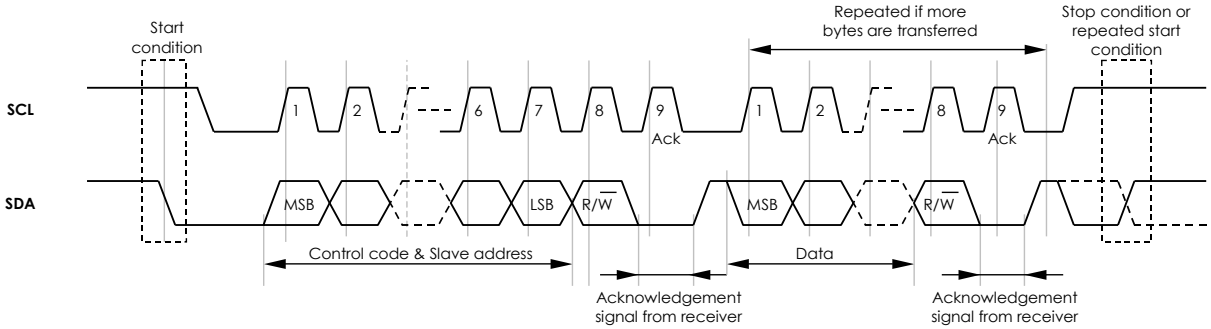

Figure 10 - 2-wire data transfer chronograms

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2-Wire AC Characteristics and timing

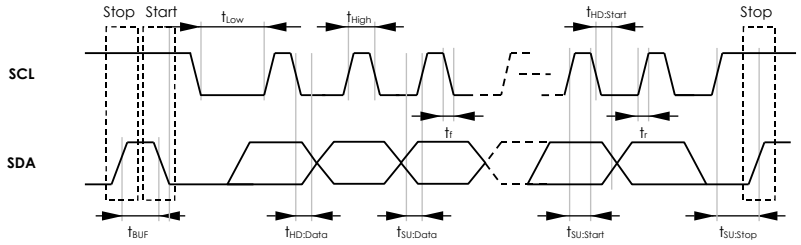

Figure 11 - 2-wire data transfer chronograms

Timing table (-40°C to +85°C, V_{CC} = 3.3V)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
Serial clock frequency	F_{SCL}	Fast mode	0	400	kHz	1
		Standard mode	0	100		
Bus free time between STOP and START	t_{BUF}	Fast mode	1.3	-	µs	1
		Standard mode	4.7	-		
Hold time for START condition	$t_{HD:Start}$	Fast mode	0.6	-	µs	1,2
		Standard mode	4.0	-		
Low period of SCL clock	t_{Low}	Fast mode	1.3	-	µs	1
		Standard mode	4.7	-		
High period of SCL clock	t_{High}	Fast mode	0.6	-	µs	1
		Standard mode	4.0	-		
Data set-up time	$t_{SU:Data}$	Fast mode	0	0.9	µs	1
		Standard mode	0	0.9		
Data hold time	$t_{HD:Data}$	Fast mode	0	0.9	µs	1,3,4
		Standard mode	0	0.9		
Set-up time for STOP and START conditions	$t_{SU:Stop}$	Fast mode	0.6	-	µs	1
		Standard mode	4.0	-		
Rise time	t_r	Fast mode	80	300	ns	-
		Standard mode	100	1000		
Fall time	t_f	Fast mode	80	300	ns	-
		Standard mode	100	1000		
EEPROM write time	t_w	-	5	20	ms	5

Notes:

1. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT}$ > 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{RMAX} + $t_{SU:DAT}$ = 1000ns + 250ns = 1250ns before the SCL line is released.
2. After this period, the first clock pulse is generated.
3. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
5. EEPROM write begins after a STOP condition occurs.

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JTAG and Boundary Scan Definition

The DLR-xx-251-Iw-Pyz-Lvv contains the following items, which meet the requirements, set by the IEEE-1149.1 standard Test Access Port and Boundary Scan Architecture, the IEEE 1149.6 Standard for Boundary-Scan Testing of Advanced Digital Networks as well as the AC boundary-scan Specification for IEEE from Cisco:

- Test Access Port (TAP)
- TAP Controller
- Instruction Register (3 Bit)
- Bypass Register (1 Bit)
- Boundary Scan Register (16 Bit)
- Device Identification Register (32 Bit)
- User Data Register (32 Bit)
- Certified 'AC Boundary Scan' as licensed from Cisco Systems, Inc.

Details on Boundary Scan Architecture and the Test Access Port can be found in IEEE 1149.1-2001, IEEE 1149.6-2003 and AC boundary-scan Specification for IEEE from Cisco (EDCS-134568 Rev B5, www.acextest.org).

Instruction Codes for the module Boundary Scan Architecture

Instruction	Selected Register	Instruction Codes
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
AC_EXTEST	AC Boundary Scan	100
SAMPLE/PRELOAD	Boundary Scan	010
IDCODE	Device Identification	001
SEL_INIT_SCAN	User Data Register	011
EXTEST_PULSE	AC Boundary Scan	101
EXTEST_TRAIN	AC Boundary Scan	110

Device Identification Register (32 Bits)

MSB LSB

31																															0
Version (4 Bits)				**Part Number (16 Bits)**																**Manufacturer Identity (11 Bits)**											**Fixed**
0001				000000 0000000101																00101011111											1

Boundary Scan Register (16 Bits)

This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells and is 16 bits in length. The table below shows all cell bit locations and definitions.

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	RUN	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	SD_All	SQS
-	Out	Out	Out	Out	Out	Out	Out	Out	Out	Out	Out	Out	Out	Out	In
-	BC_2	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	HX_BC4_DIFF	BC_2	BC_4
-	No AC	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	AC_Extest	No AC	No AC

Notes:

BC_4: Observe only registers
BC_2: Control and observe registers
HEX_BC4_DIFF: AC Observe only registers

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User Data Register (16 Bit)

This register contains a shift register path for different control signals and is 32 bits in length. The table below shows all signals connected to the user data register.

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1
Read	Read	Read	Read	Read	Read	Read	Read	Read	Read	Read	Read	Read	Read	Read	Read

Notes:

Res. : Reserved bit (Logical low)

Channels distribution over the fiber and pigtail length

The following table shows the channel distribution over the 12 fiber ribbon configuration.

Fiber number	12	11	10	9	8	7	6	5	4	3	2	1
Color code	Blue	Orange	Green	Brown	Grey	White	Red	Black	Yellow	Violet	Pink	Aqua
DLR-02- 251-…						Rx2	Rx1					
DLR-04-251-…					Rx4	Rx3	Rx2	Rx1				
DLR-08-251-…[1]			Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Rx1		
DLR-12-251-…	Rx12	Rx11	Rx10	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Rx1

Note:

1. DLR-08-251-Ix-Py1-Lvv or DLR-08-251-Ix-Py2-Lvv 8 channel devices based on 12 channel version with 4 channels permanently disabled.

According to the previous table, the module pin is following the same distribution (pins are for IGM package option):

1. For a 2 channels receiver having a fiber ribbon pigtail (DLR-02-251-Ix-Py1-Lvv or DLR-02-251-Ix-Py2-Lvv), the electrical input data will be distributed as stated on the table: channel #1 positive input is connected to D3+ (Pin A3) and negative input to D3- (Pin B3), channel #2 positive input is connected to D10+ (Pin B8) and negative input to D10- (Pin A8).
2. For a 4 channels receiver having a fiber ribbon pigtail (DLR-04-251-Ix-Py1-Lvv or DLR-04-251-Ix-Py2-Lvv), the electrical input data will be distributed as stated on the table: channel #1 positive input is connected to D3+ (Pin A3) and negative input to D3- (Pin B3), channel #2 positive input is connected to D8+ (Pin A5) and negative input to D8- (Pin A6), channel #3 positive input is connected to D7+ (Pin C5) and negative input to D7- (Pin C6), channel #4 positive input is connected to D10+ (Pin B8) and negative input to D10- (Pin A8).
3. Same for 8 channels device.

Other Optical pin-out could be proposed under customer requirements.

The following table provides the pigtail length precision per length (measure from module edge to optical end-face)

Pigtail length (cm)	Standard Dimensions		Tight Tolerances (T option)	
	Tolerances	Resolution	Tolerances	Resolution
5 to 50	+/-15mm	10mm	+/-5mm	1mm
50 to 100	+/-20mm	15mm	+/-10mm	5mm
Above 100	+/-2%	15mm	Not Available	10mm

For Tight tolerances add "T" in the part number at the end of the "-Lvv" section followed by the millimeter value: "-LvvTw" for a length of vv.w cm. For example a receiver with a pigtail of 12.3cm length will have the P/N: **DLR-12-251-Ix-Pyz-L12T3.**

Temperature and Mechanical Qualifications

D-Lightsys modules fully complies with the following Aeronautic/harsh environment standards:

- ARINC804, extended operation range,
- MIL-STD-883e (as specified with ARINC804),
- DO-160 (as specified with ARINC804).

Refer to the ARINC804, MIL-STD-883e and DO-160 standards for further details on the qualifications.

Note that the vibrations and shocks qualification results are related to the optical termini and package selected. Selecting a non-environmental qualified optical termini and/or packaging will limit the module environmental performances. Contact sales for details or recommended package/optical termini.

Pin out description

D-Light DLR-xx-251-Iw-Pyz-Lv
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Signal	Pin number		Type	
	IGM	IL		
DataOut1+ or D1+	E1	6	HS[1] output	**Positive Data output for channel 1:** LVDS/CML positive high speed output
DataOut1- or D1-	D1	5	HS[1] output	**Negative Data output for channel 1:** LVDS/CML negative high speed output
DataOut2+ or D2+	B1	4	HS[1] output	**Positive Data output for channel 2:** LVDS/CML positive high speed input
DataOut2- or D2-	A1	3	HS[1] output	**Negative Data output for channel 2:** LVDS/CML negative high speed output
DataOut3+ or D3+	A3	2	HS[1] output	**Positive Data output for channel 3:** LVDS/CML positive high speed output
DataOut3- or D3-	B3	1	HS[1] output	**Negative Data output for channel 3:** LVDS/CML negative high speed output
DataOut4+ or D4+	D3	48	HS[1] output	**Positive Data output for channel 4:** LVDS/CML positive high speed output
DataOut4- or D4-	E3	47	HS[1] output	**Negative Data output for channel 4:** LVDS/CML negative high speed output
DataOut5+ or D5+	G5	46	HS[1] output	**Positive Data output for channel 5:** LVDS/CML positive high speed output
DataOut5- or D5-	G6	45	HS[1] output	**Negative Data output for channel 5:** LVDS/CML negative high speed output
DataOut6+ or D6+	E5	44	HS[1] output	**Positive Data output for channel 6:** LVDS/CML positive high speed output
DataIn6- or D6-	E6	43	HS[1] Input	**Negative Data output for channel 6:** LVDS/CML negative high speed output
DataOut7+ or D7+	C5	42	HS[1] output	**Positive Data output for channel 7:** LVDS/CML positive high speed output
DataOut7- or D7-	C6	41	HS[1] output	**Negative Data output for channel 7:** LVDS/CML negative high speed output
DataOut8+ or D8+	A5	40	HS[1] output	**Positive Data output for channel 8:** LVDS/CML positive high speed output
DataOut8- or D8-	A6	39	HS[1] output	**Negative Data output for channel 8:** LVDS/CML negative high speed output
DataOut9+ or D9+	E8	38	HS[1] output	**Positive Data output for channel 9:** LVDS/CML positive high speed output
DataOut9- or D9-	D8	37	HS[1] output	**Negative Data output for channel 9:** LVDS/CML negative high speed output
DataIn10+ or D10+	B8	36	HS[1] output	**Positive Data output for channel 10:** LVDS/CML positive high speed output
DataOut10- or D10-	A8	35	HS[1] output	**Negative Data output for channel 10:** LVDS/CML negative high speed output
DataIn11+ or D11+	A10	34	HS[1] output	**Positive Data output for channel 11:** LVDS/CML positive high speed output
DataOut11- or D11-	B10	33	HS[1] output	**Negative Data output for channel 11:** LVDS/CML negative high speed output
DataOut12+ or D12+	D10	32	HS[1] output	**Positive Data output for channel 12:** LVDS/CML positive high speed output

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DataOut12- or D12-	E10	31	HS[1] output	**Negative Data output for channel 12:** LVDS/CML negative high speed output
RxEnable	K10	24	Digital Input	**Receiver Enable:** Enable the module (set to 1 to enable the receiver)
SQUEN	K2	12	Digital Input	**SQUELCH Enable:** The active high Squelch Enable pad enables the circuitry that will hold the differential data output at low when the signal level is below the signal-detect level for the channel. When SQEN is low, the differential data output may chatter even when the signal level is below the signal-detect threshold. This signal may be left unconnected to enable the squelch feature.
RSSI	J2	25	Analog output	**Receiver Strength Signal Indicator:** The Receiver Signal Strength Indicator output pad is a single analog output that sources a current proportional to the sum of the average photo-detector currents on each of the channels. The output is used during manufacturing for active alignment and for diagnostic purposes. It is should be left unconnected when not being used.
nTESTD	H10	-	Digital Output	**Test Device (Reserved):** The active-low Test Device input (nTESTD) is an input pad to enter a test mode reserved for D-Lightsys. It is should be left unconnected when the LEGACY mode is not active.
SD6 (Legacy mode only)	H2	-	Digital Output	**SD6:** This pad has no function in the non-legacy mode. It is only defined in legacy mode as SD6.
nPOR	J10	-	Digital input	**Power on Reset:** The active low Power on Reset (nPOR) pin is used to reset the receiver digital memory. The nPOR pad is used as an External notPOR when LEGACY is low. It should be left unconnected in normal operation.
SD_ALL	J3	11	Digital Output Open Drain	**Signal Detect All:** This output pin is high when all active channels have signals levels above the threshold. When the optical signal on any channel is below a threshold, SD_ALL is low. The signal detect signal uses a hysteresis circuit to avoid chatter.
SCL	K1	13	Digital Input	**2-Wire Controller Serial Clock input:** The serial clock input is used to clock data (SDA pin) into the module controller memory on rising edges and clock data out on falling edges. Connected to GND not used.
SDA	J1	14	Digital In/output	**2-Wire serial data interface:** The serial data pin is for serial data transfer to and from the module. The pin is open drain and may be wire-ORed with other open drain or open collector interfaces. Connected to GND not used.

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SERADD (SADD)	H1	15	Digital Input	**Module Serial Interface Address Selection:** The Serial Address pad (SERADD) selects the slave address of the serial interface that the device will respond to. When the input is low, it will respond to 7 bits address: $(1010010)_b$. When the input is high, it will respond to 7 bits address: $(1010011)_b$. The SERADR can be changed only when there are no transactions on the serial interface.
SELL12	K9	-	Digital Input	**Reserved:** This pin is used to only validate channel 1 to 4, all other channels are disabled. The default mode (NC) is all channel enabled.
TDI	J5	-	JTAG Input	**Test Data Input:** TDI signal carries test data into the device via the IEEE P1149.1 test access port. TDI is sampled on rising edge of TCK. TDI has an integrated pull-up.
TDO	J6	-	JTAG Output	**Test Data Output:** TDO signal carries test data out of the device via the IEEE P1149.1 test access port. TDO is updated on falling edge of TCK. TDO is a tri-state out that is inactive except when scanning of data in progress.
TCK	K5	-	JTAG Input	**Test Clock:** TCK signal provides timing for the test operations that are carried out using the IEEE P1149.1 test access port. When this pin is not used, an external pull down is recommended.
TMS	K6	-	JTAG Input	**Test Mode Select:** TMS signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integrated pull-up.
TRSTn	K7	-	JTAG Input	**Active Low Test Reset:** TRSTn signal provides an asynchronous test access port reset via the IEEE P1149.1 test access port. TRSTn must be pulled low during normal device operation. This place the JTAG logic into the reset state.

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<table>
<tr>
<td>LEGACY</td>
<td>K3</td>
<td>-</td>
<td>Digital Input
(Pull-Up)</td>
<td>Legacy Mode: The active-high Legacy Mode Enable (LEGACY) redefines the pad definitions such that signal detect for each channel is available on individual outputs. Due to the number of pads required for individual signal detects, the JTAG and serial interfaces are not available in legacy mode.
When this pad is unconnected, it is in legacy mode.

When LEGACY is high, the pads are redefined as signal detect signals:
<table>
<tr><th>Pad Name</th><th>Function when Legacy is high</th></tr>
<tr><td>TDO</td><td>SD1: Signal Detect Channel 1</td></tr>
<tr><td>TRSTN</td><td>SD2: Signal Detect Channel 2</td></tr>
<tr><td>SD_ALL</td><td>SD3: Signal Detect Channel 3</td></tr>
<tr><td>SDA</td><td>SD4: Signal Detect Channel 4</td></tr>
<tr><td>SCL</td><td>SD5: Signal Detect Channel 5</td></tr>
<tr><td>M2</td><td>SD6: Signal Detect Channel 6</td></tr>
<tr><td>nPOR</td><td>SD7: Signal Detect Channel 7</td></tr>
<tr><td>nTESTD</td><td>SD8: Signal Detect Channel 8</td></tr>
<tr><td>SERADDR</td><td>SD9: Signal Detect Channel 9</td></tr>
<tr><td>TCK</td><td>SD10: Signal Detect Channel 1</td></tr>
<tr><td>TMS</td><td>SD11: Signal Detect Channel 11</td></tr>
<tr><td>TDI</td><td>SD12: Signal Detect Channel 12</td></tr>
</table>
Connect to GND to disable the Legacy mode and enter the serial interface mode.</td>
</tr>
<tr>
<td>V_{CC}</td>
<td>G1,G2, G9,G10</td>
<td>8,29</td>
<td>Power</td>
<td>Positive supply rail for digital parts: +3.3Volts positive power supply for the receiver.</td>
</tr>
<tr>
<td>V_{oref}</td>
<td>G3,H3, G8,H8</td>
<td>9,28</td>
<td>Power</td>
<td>Positive supply rail for the output stage: +3.3Volts positive power supply for the receiver in CML operation. See text for different voltage compatibility.</td>
</tr>
<tr>
<td>GND</td>
<td>A2,A4,A7, A9, B2,B4,B7,B 9, C1-C4, C7-C10, D2, D4-D7,D9, E2,E4,E7,E9 , F1-F10,G4,G7, H4-H7</td>
<td>7,10,16-23,26-27,30</td>
<td>Power</td>
<td>Negative supply rail: negative power supply tied to GND (0 Volt) for the transmitter.</td>
</tr>
<tr>
<td>NC</td>
<td colspan="2">J4,K4,J7,J8,J9, H9, K8</td>
<td>-</td>
<td>Not connected Input Pins: Do not connect those pins. For manufacturing test purpose only.</td>
</tr>
</table>

Notes: [1]: HS pin type: High Speed inputs CML/LVDS compatible input pins.

[2]: Tri-state input pin allows three input voltage: High, Medium (not connected) and Low operations.

Note that the LEGACY mode is not accessible in the LCC package.

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Socketed Package Pin Layout (DLR-xx-251-IGM-Pyz-Lvv Option)

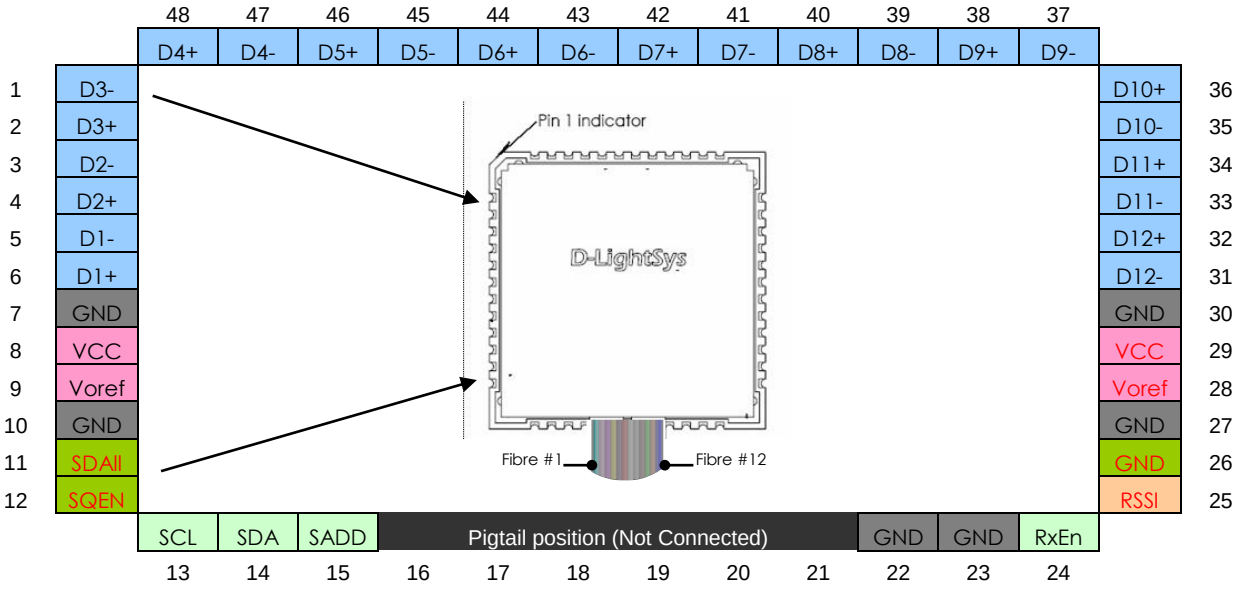
	1	2	3	4	5	6	7	8	9	10
A	D2-	GND	D3+	GND	D8+	D8-	GND	D10-	GND	D11+
B	D2+	GND	D3-	GND	GND	GND	GND	D10+	GND	D11-
C	GND	GND	GND	GND	D7+	D7-	GND	GND	GND	GND
D	D1-	GND	D4+	GND	GND	GND	GND	D9-	GND	D12+
E	D1+	GND	D4-	GND	D6+	D6-	GND	D9+	GND	D12-
F	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
G	VCC	VCC	Voref	GND	D5+	D5-	GND	Voref	VCC	VCC
H	SADD	SD6	Voref	GND	GND	GND	GND	Voref	NC	nTest
J	SDA	RSSI	SDAll	NC	TDI	TDO	NC	NC	NC	nPOR
K	SCL	SQEn	LEG	NC	TCK	TMS	TRST	NC	SEL12	RxEn

(View from top or from the application board)

HSLink
Power Supply
Analog monitors/controls
Digital monitors/controls
Ground pins
JTAG Interface
Serial interface
Non Connected

Note that the module pin numbering is independent from the Meg-Array numbering, in order to allow module keying by rotating the Meg-Array by 90° steps. Contact sales or technical support for module keying options.

LCC Package Pin Layout (DLR-xx-251-IL-Pyz-Lvv Option)



DATASHEET

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Package mechanical drawings

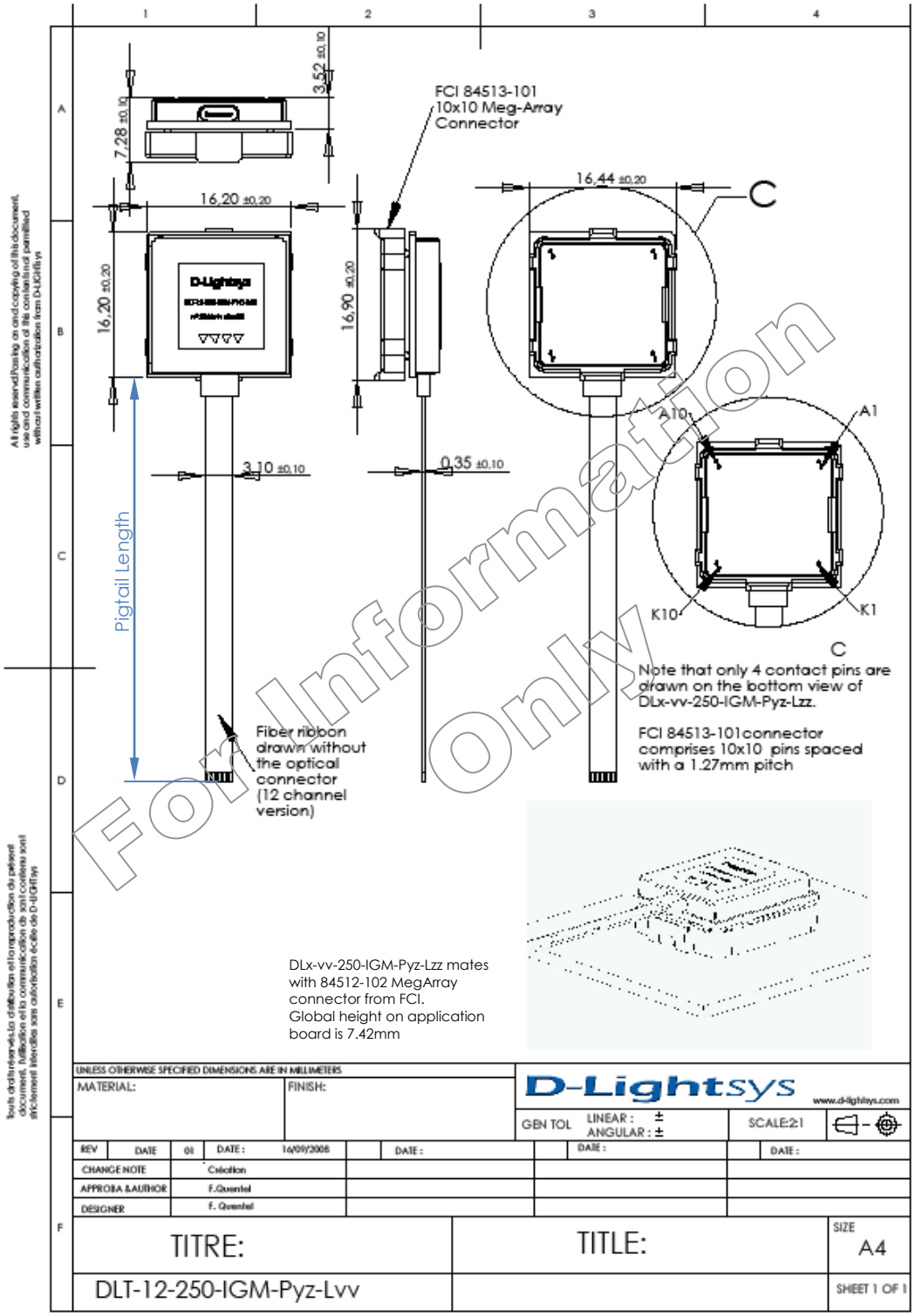

Figure 12 - DLx-xx-25x-IGM-Pyz-Lvv mechanical drawing

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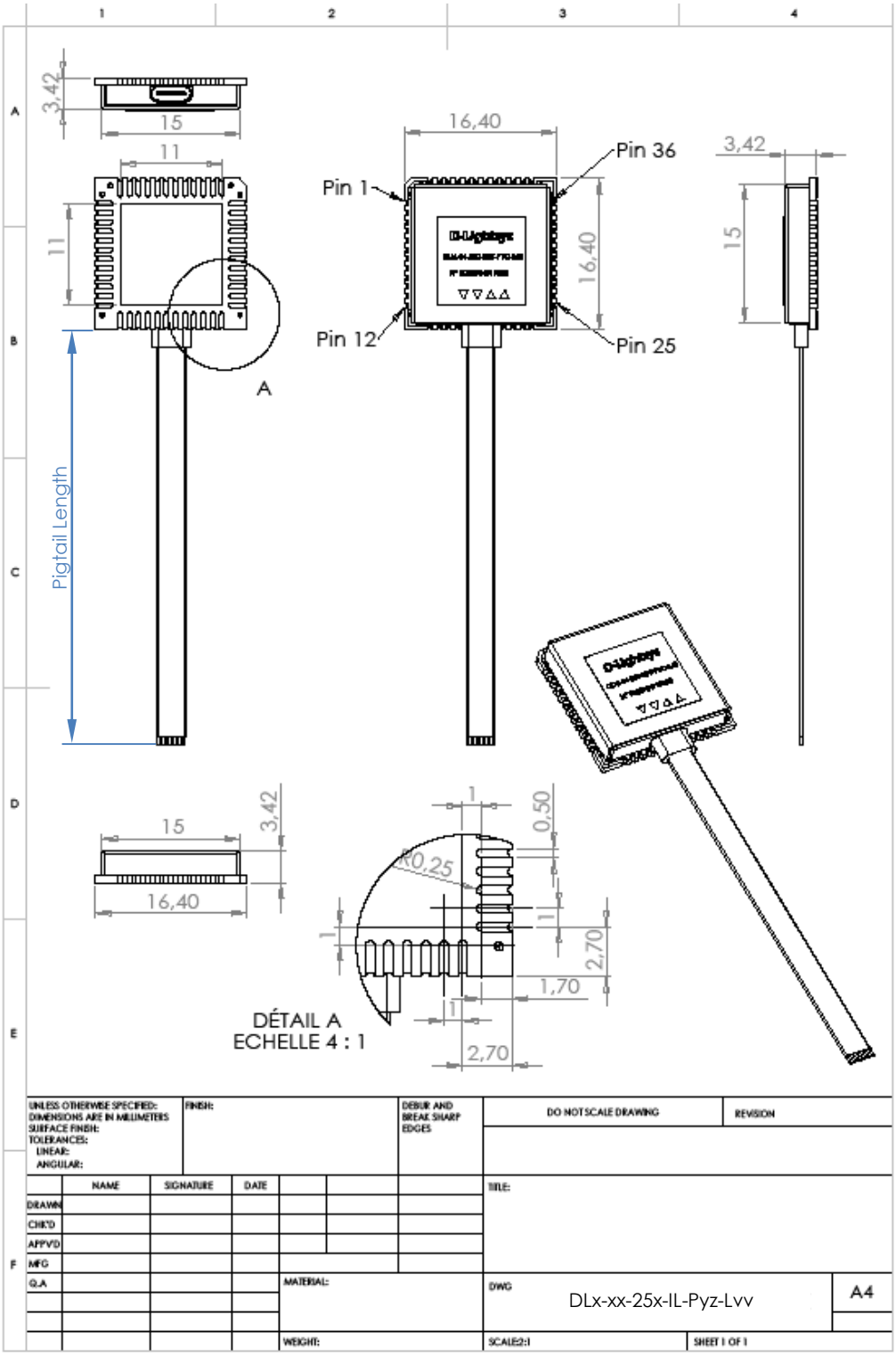

Figure 13 - DLx-xx-25x-IL-Pyz-Lvv mechanical drawing

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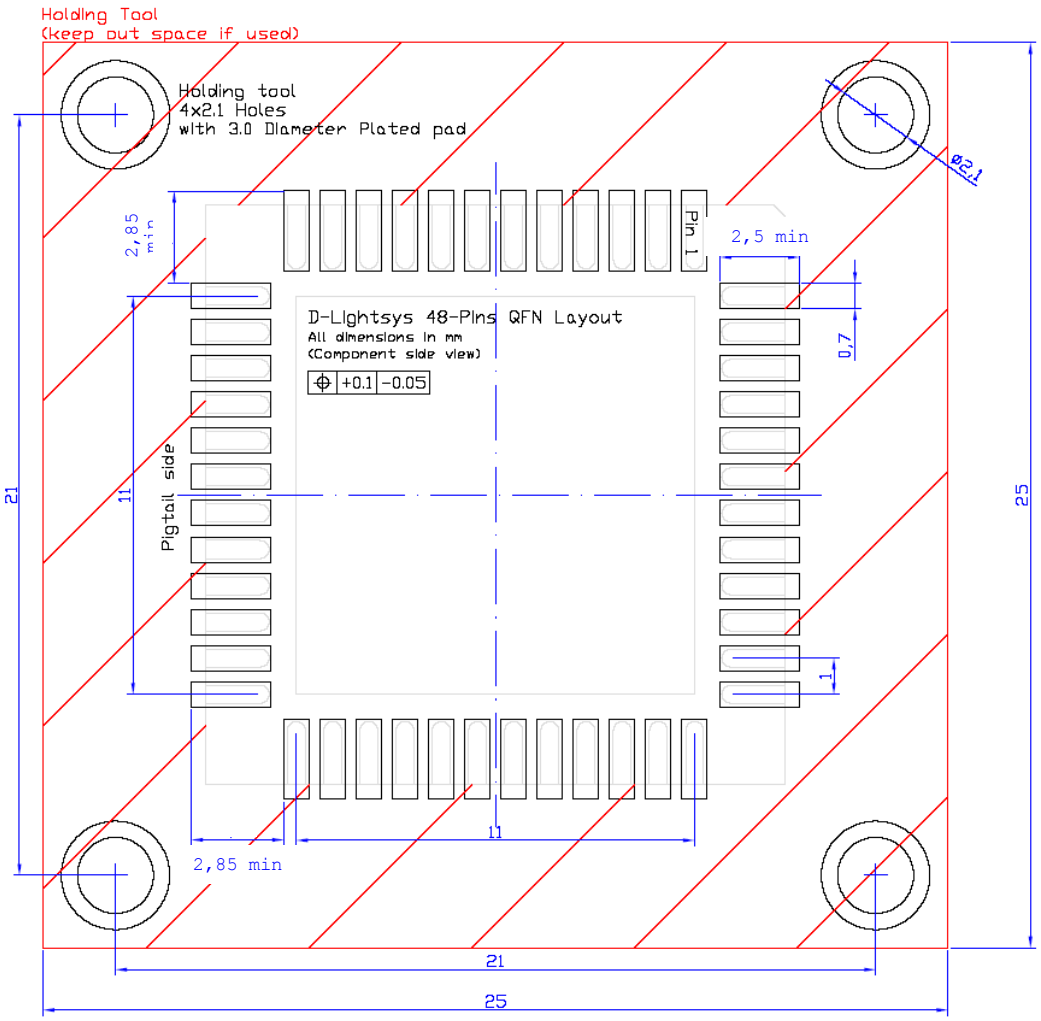
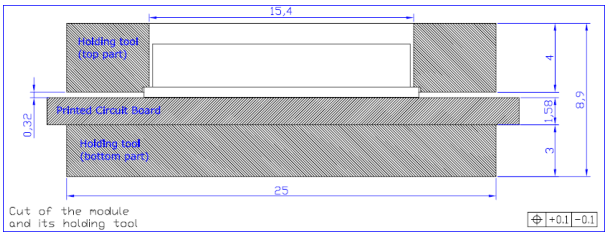
Module holding tool option:
If the module is intended to be used with the holding tool (Ref: HT-DLM-v1.0), The 4xØ2.1mm diameter holes and the the keep out space (Both sides) presented in the previous figure should be used. If the module is directly soldered on board, 4xØ2.1mm Holes and keep out space could be omitted.

LCC package PCB Layout drawings

A typical PCB footprint is shown on the following figure (dimension are in mm).



Note:
If the module is intended to be used with the holding tool (Ref: HT-DLM-v1.0), The 4xØ2.1mm diameter holes and the the keep out space (Both sides) presented in the previous figure should be used. If the module is directly soldered on board, 4xØ2.1mm Holes and keep out space could be omitted.



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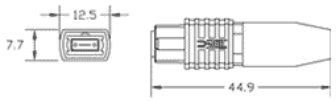
Pigtail information

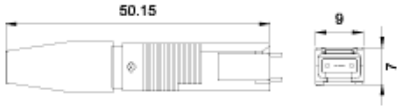
The DLT-xx-251-Iw-Pyz-Lvv optical pigtail consists of a standard fiber ribbon optical cable terminated by an MT-compatible connector. Pigtail length can be adjusted to fit the customer's requirements.

The following pigtail connectors are available.

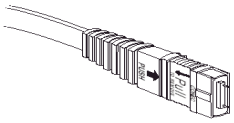
- **O option :** MPO connector (based on MT ferrule).



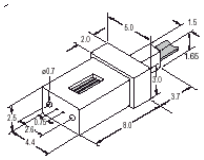
- **X option :** MPX connector (based on MT ferrule).



- **T option :** MTP connector (based on MT ferrule).



- **N option :** No connector Pigtail mount with MT ferrule.



Related literature (distributed under Non-Disclosure Agreement)

Application Notes:

Ref: AN-SLM/01 *"S-Light Transceiver Usage"* Version 1.1
Ref: AN-SLM/02 *"S-Light and D-Light 2 wire serial interface usage"* Version 1.0
Ref: AN-SLM/03 *"D-Light and S-Light Input/Output Stage modeling"* Version 1.0
Ref: AN-SLM/04 *"S-Light Reliability Data"* Version 0.1
Ref: AN-SLM/05 *"S-Light and D-Light surface mount process"* Version 0.3
Ref: AN-SLM/06 *"S-Light and D-Light surface mount bonding process"* Version 1.0
Ref: AN-SLM/07 *"D-Light thermal modeling"* Version 0.1
Ref: AN-SLM/08 *"Hand soldering process for D-Lightsys QFN package"* Version 1.0
Ref: AN-SLM/09 *"10Gbps operation of EVM-SLM/02 FR-4 evaluation board analysis"* Version 1.0

Evaluation board & Software materials:

Ref: EVM-DLx/01 "*DLx-www-xy-Pz* Evaluation board documentations" Version 1.0
Ref: SOF-DLM/01 "Windows Based D-Light family module programming software user's guide"

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