



3.3V CMOS 1-TO-10 CLOCK DRIVER

IDT74FCT3807D/E

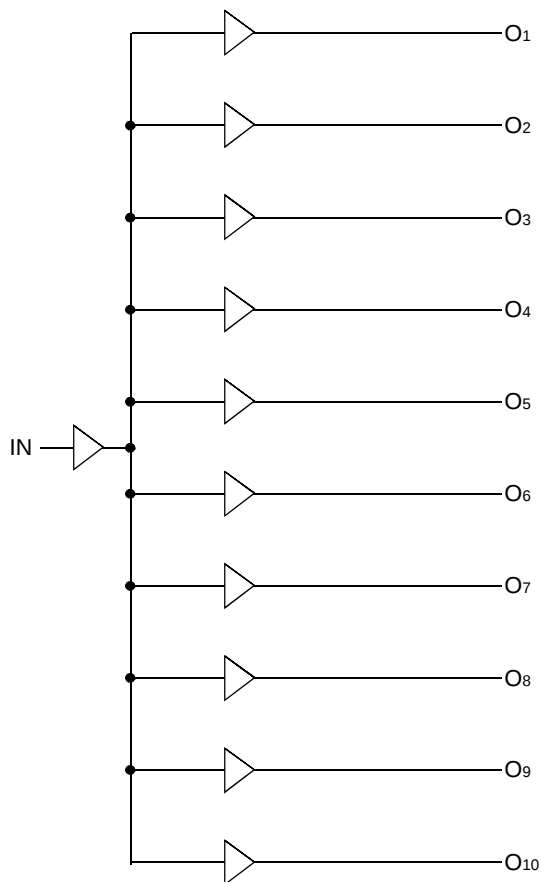
FEATURES:

- Advanced CMOS Technology
- Guaranteed low skew < 100ps (max.)
- Very low duty cycle distortion < 250ps (max.)
- High speed propagation delay < 2ns (max.)
- Very low CMOS power levels
- TTL compatible inputs and outputs
- 1:10 fanout
- Maximum output rise and fall time < 1ns (max.)
- Low input capacitance: 3pF typical
- $V_{CC} = 3.3V \pm 0.3V$
- Inputs can be driven from 3.3V or 5V components
- Operating frequency up to 166MHz
- Available in SSOP, QSOP, and TSSOP packages

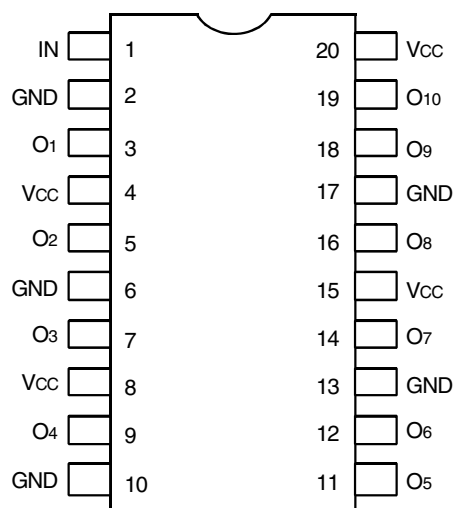
DESCRIPTION:

The FCT3807 is a 3.3V clock driver built using advanced CMOS technology. This low skew clock driver offers 1:10 fanout. The large fanout from a single input reduces loading on the preceding driver and provides an efficient clock distribution network. Multiple power and grounds reduce noise. Typical applications are clock and signal distribution.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP/ QSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{CC}	Input Power Supply Voltage	−0.5 to +4.6	V
V _I	Input Voltage	−0.5 to +5.5	V
V _O	Output Voltage	−0.5 to V _{CC} +0.5	V
T _J	Junction Temperature	150	°C
T _{STG}	Storage Temperature	−65 to +165	°C

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3	4	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	—	6	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
I _N	Input
O _x	Outputs

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CCQ}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}	—	0.1	30	μA
ΔI _{CC}	Power Supply Current per Input HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V	—	45	300	μA
I _{CCD}	Dynamic Power Supply Current per Output ⁽³⁾	V _{CC} = Max. C _L = 15pF All Outputs Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	80	120	μA/MHz
I _C	Total Power Supply Current ⁽⁴⁾	V _{CC} = Max. C _L = 15pF All Outputs Toggling f _i = 133MHz	V _{IN} = V _{CC} V _{IN} = GND		125	150	mA
			V _{IN} = V _{CC} - 0.6V V _{IN} = GND		125	150	
		V _{CC} = Max. C _L = 15pF All Outputs Toggling f _i = 166MHz	V _{IN} = V _{CC} V _{IN} = GND	—	155	195	
			V _{IN} = V _{CC} - 0.6V V _{IN} = GND	—	160	195	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i)$$

I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} - 0.6V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_i = Input Frequency

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level			2	—	5.5	V
V_{IL}	Input LOW Level			-0.5	—	0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_I = 5.5\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}$	$V_I = \text{GND}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{ODH}	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3,4)}$		-45	-75	-180	mA
I_{ODL}	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3,4)}$		50	92	200	mA
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3,4)}$		-60	-135	-240	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -12\text{mA}$	2.4 ⁽⁵⁾	3	—	V
			$I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$	—	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 12\text{mA}$	—	0.3	0.5	V
			$I_{OL} = 100\mu\text{A}$	—	—	0.2	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3$, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. $V_{OH} = V_{CC} - 0.6\text{V}$ at rated current.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - 3807D (3,4)

Symbol	Parameter	Conditions ⁽¹⁾	Min. ⁽²⁾	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay	$C_L = 15\text{pF}$ $f \leq 133\text{MHz}$	1	2.5	ns
t_R	Output Rise Time (0.8V to 2V)		—	1	ns
t_F	Output Fall Time (2V to 0.8V)		—	1	ns
$tsk(O)$	Same device output pin-to-pin skew ⁽⁵⁾		—	250	ps
$tsk(P)$	Pulse skew ⁽⁶⁾		—	250	ps
$tsk(PP)$	Part to part skew ⁽⁷⁾		—	550	ps
f_{MAX}	Input Frequency		—	133	MHz

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - 3807E (3,4)

Symbol	Parameter	Conditions ^(1,8)	Min. ⁽²⁾	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay	$C_L = 15\text{pF}$ $f \leq 166\text{MHz}$	0.5	2	ns
t_R	Output Rise Time (0.8V to 2V)		—	1	ns
t_F	Output Fall Time (2V to 0.8V)		—	1	ns
$tsk(O)$	Same device output pin-to-pin skew ⁽⁵⁾		—	100	ps
$tsk(P)$	Pulse skew ⁽⁶⁾		—	250	ps
$tsk(PP)$	Part to part skew ⁽⁷⁾		—	550	ps
f_{MAX}	Input Frequency		—	166	MHz

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH} , t_{PHL} , $tsk(P)$, and $tsk(O)$ are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC} , operating temperature and process parameters. These propagation delay limits do not imply skew.
5. Skew measured between all outputs under identical transitions and load conditions.
6. Skew measured is difference between propagation delay times t_{PHL} and t_{PLH} of same output under identical load conditions.
7. Part to part skew for all outputs given identical transitions and load conditions at identical V_{CC} levels and temperature.
8. Airflow of 1m/s is recommended for frequencies above 133MHz.

TEST CIRCUITS

TEST CONDITIONS

Symbol	Vcc = 3.3V ±0.3V	Unit
CL	15	pF
RT	Z _{OUT} of pulse generator	Ω
t _R / t _F	1 (0V to 3V or 3V to 0V)	ns

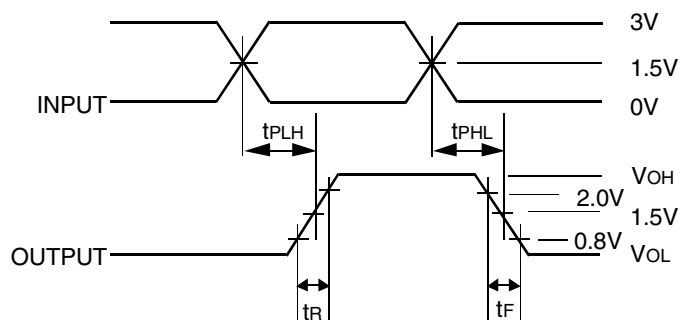
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

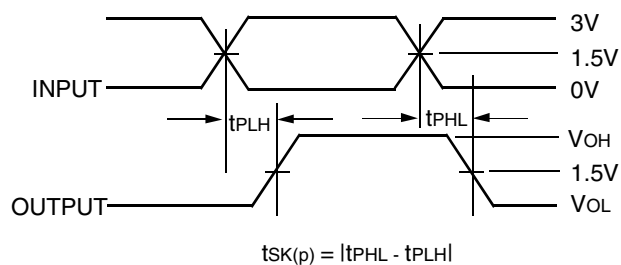
RT = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

t_R / t_F = Rise/Fall time of the input stimulus from the Pulse Generator.

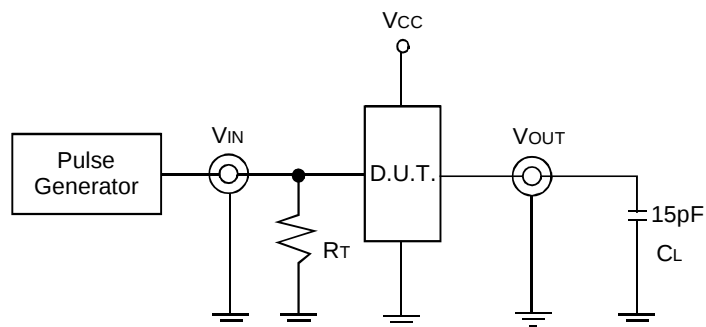
TEST WAVEFORMS



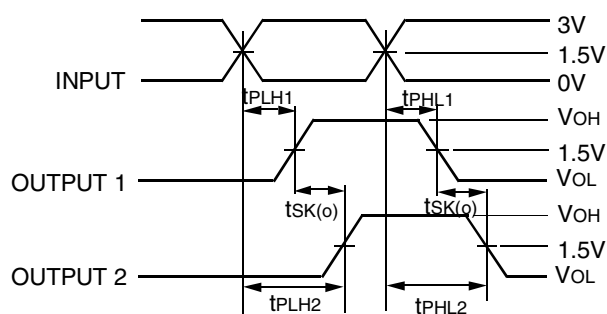
Propagation Delay



Pulse Skew - tSK(P)

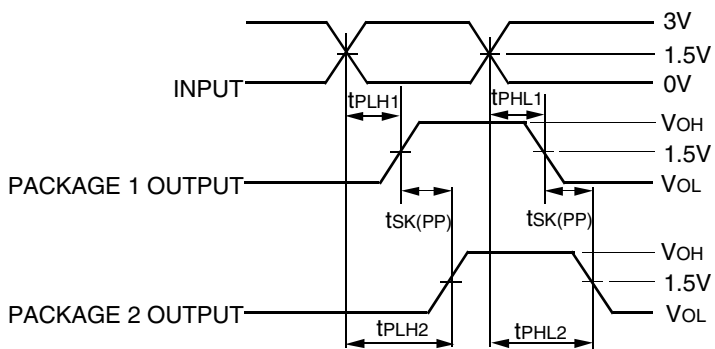


CL = 15pF Circuit



$$t_{SK(O)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

Output Skew - tSK(O)



$$t_{SK(PP)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

Part-to-Part Skew - tSK(PP)

Part-to-Part Skew is for the same package and speed grade.

ORDERING INFORMATION

74FCT	XXXX	X	X		
	Device Type	Package	Process		
				I	-40°C to +85°C (Industrial)
				PYG	SSOP - Green
				QG	QSOP - Green
				PGG	TSSOP - Green
				3807D 3807E	3.3V CMOS 1-to-10 Clock Driver



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