512K X28HT512 64K x 8 Bit

High Temperature, 5 Volt, Byte Alterable E²PROM

FEATURES

- **175°C Full Functionality**
- **Simple Byte and Page Write**
  - **—Single 5V Supply**
  - **—Self-Timed**
    - **—No Erase Before Write**
    - **—No Complex Programming Algorithms**
    - **—No Overerase Problem**
- **Highly Reliable Direct Write™ Cell**
  - **—Endurance: 10,000 Write Cycles**
  - **—Data Retention: 100 Years**
  - **—Higher Temperature Functionality is Possible by Operating in the Byte Mode**

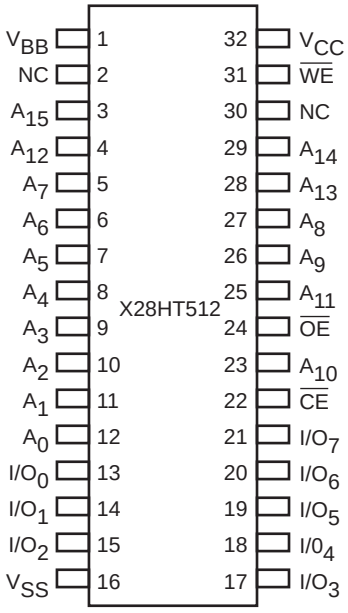
DESCRIPTION

The X28HT512 is an 64K x 8 CMOS E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology which provides Xicor products superior high temperature performance characteristics. Like all Xicor programmable nonvolatile memories the X28HT512 is a 5V only device. The X28HT512 features the JEDEC approved pinout for bytewide memories, compatible with industry standard EPROMS.

The X28HT512 supports a 128-byte page write operation, effectively providing a 39µs/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds.

PIN CONFIGURATION

FLAT PACK
CERDIP
SOIC (R)



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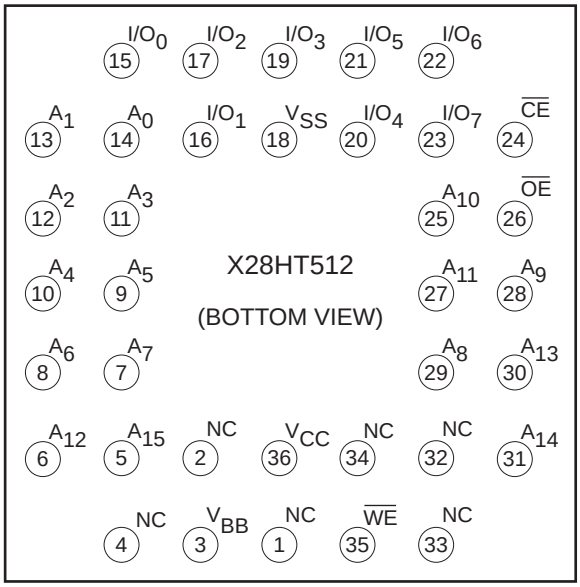
PGA



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PIN DESCRIPTIONS

Addresses (A_0–A_{15})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28HT512 through the I/O pins.

Back Bias Voltage (V_{BB})

It is required to provide -3V on pin 1. This negative voltage improves higher temperature functionality.

Write Enable ($\overline{WE}$)

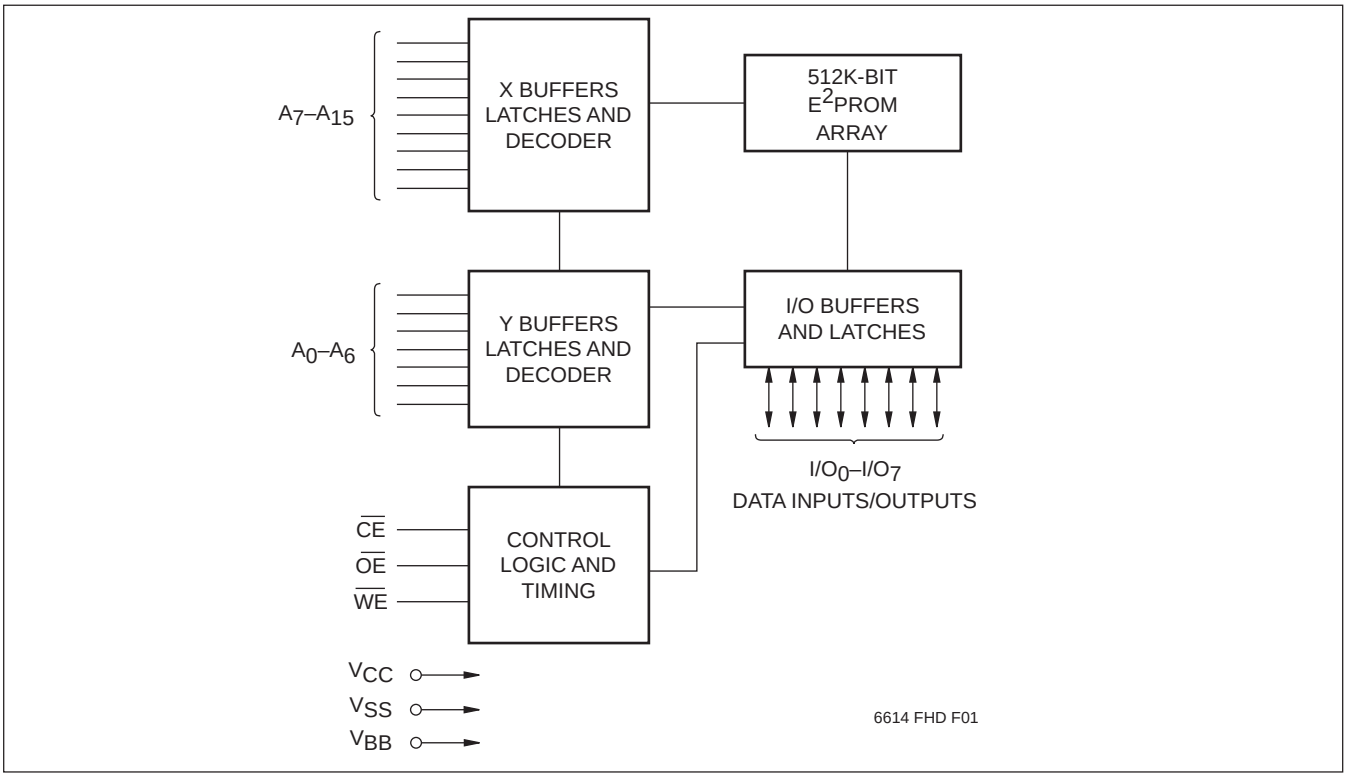
The Write Enable input controls the writing of data to the X28HT512.

PIN NAMES

Symbol	Description
A_0–A_{15}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{BB}	–3V
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

6614 PGM T01

FUNCTIONAL DIAGRAM



DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28HT512 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

The page write feature of the X28HT512 allows the entire memory to be written in 2.5 seconds. Page write allows two to one hundred twenty-eight bytes of data to be consecutively written to the X28HT512 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_7 through A_{15}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

HARDWARE DATA PROTECTION

The X28HT512 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse typically less than 10ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is ≤3.4V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity. Write cycle timing specifications must be observed concurrently.

SYSTEM CONSIDERATIONS

Because the X28HT512 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

It has been demonstrated that markedly higher temperature performance can be obtained from this device if $\overline{CE}$ is left enabled throughout the read and write operation.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28HT512 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
X28HT512 ..... –40°C to +175°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMEND OPERATING CONDITIONS

Temperature	Min.	Max.
High Temp	–40°C	+175°C

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Supply Voltage	Limits
X28HT512	5V ±5%
Back Bias Voltage (V_{BB})	–3V ±10%

6614 PGM T03.1

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified.)

		Limits			
Symbol	**Parameter**	**Min.**	**Max.**	**Units**	**Test Conditions**
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, Address Inputs = .4V/2.4V Levels @ f = 5MHz
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)		3	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		20	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		20	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(1)	Input LOW Voltage	–1	0.6	V	
V_{IH}(1)	Input HIGH Voltage	2.2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.5	V	I_{OL} = 1mA
V_{OH}	Output HIGH Voltage	2.6		V	I_{OH} = –400µA
V_{BB}	Back Bias Voltage		200	µA	V_{BB} = –3V±10%

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Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-up to Read Operation	100	µs
t_{PUW}(2)	Power-up to Write Operation	5	ms

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	10	pF	V_{IN} = 0V

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ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles per Byte
Data Retention	100		Years

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A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

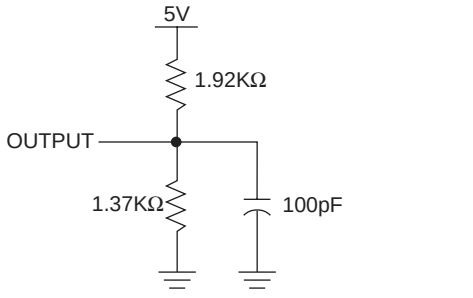
6614 PGM T07

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

6614 PGM T08

EQUIVALENT A.C. LOAD CIRCUIT



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SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (2) This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X28HT512-20		X28HT512-25		Units
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		ns
t_{CE}	Chip Enable Access Time		200		250	ns
t_{AA}	Address Access Time		200		250	ns
t_{OE}	Output Enable Access Time		80		80	ns
t_{LZ}(3)	$\overline{CE}$ LOW to Active Output	0		0		ns
t_{OLZ}(3)	$\overline{OE}$ LOW to Active Output	0		0		ns
t_{HZ}(3)	$\overline{CE}$ HIGH to High Z Output		80		80	ns
t_{OHZ}(3)	$\overline{OE}$ HIGH to High Z Output		80		80	ns
t_{OH}	Output Hold from Address Change	0		0		ns

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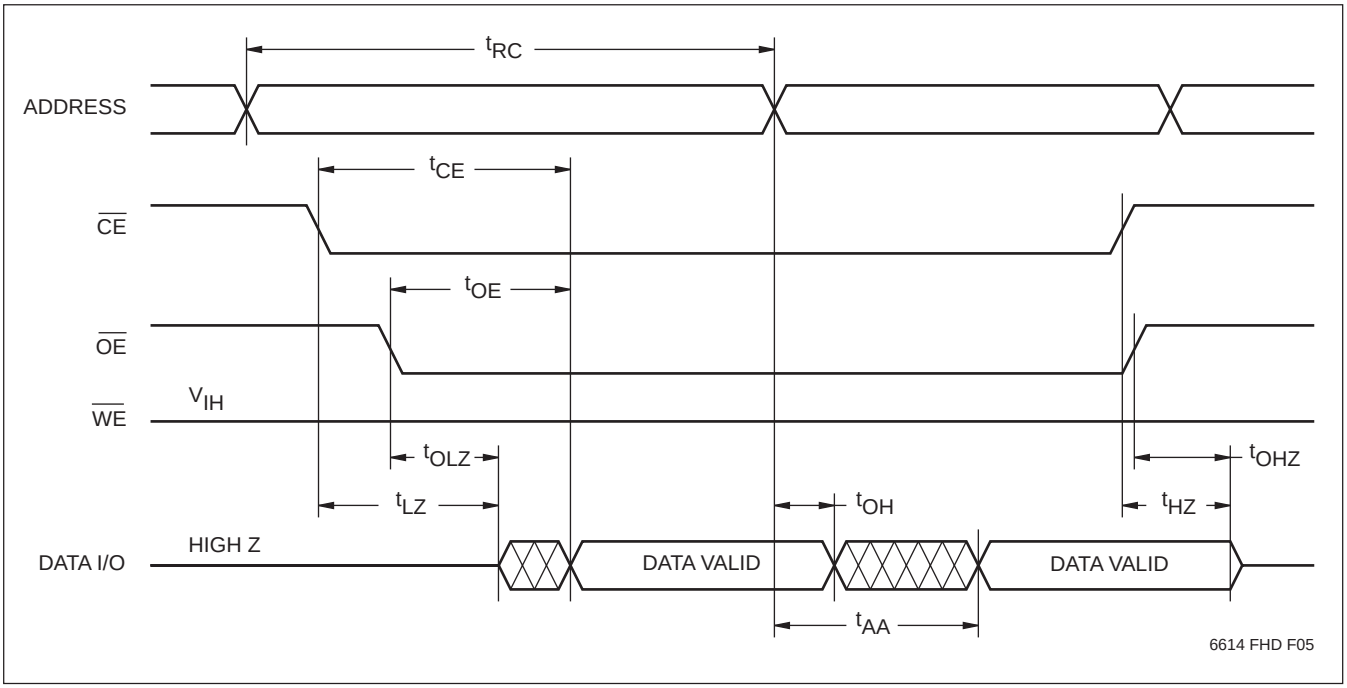
Read Cycle



Notes: (3) t_{LZ} min., t_{HZ}, t_{OLZ} min., and tOHZ are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Max.	Units
t_{WC}(4)	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	20		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	200		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	10		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	200		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery	200		ns
t_{DV}	Data Valid		1	µs
t_{DS}	Data Setup	100		ns
t_{DH}	Data Hold	25		ns
t_{DW}	Delay to Next Write	10		µs
t_{BLC}	Byte Load Cycle	0.4	100	µs

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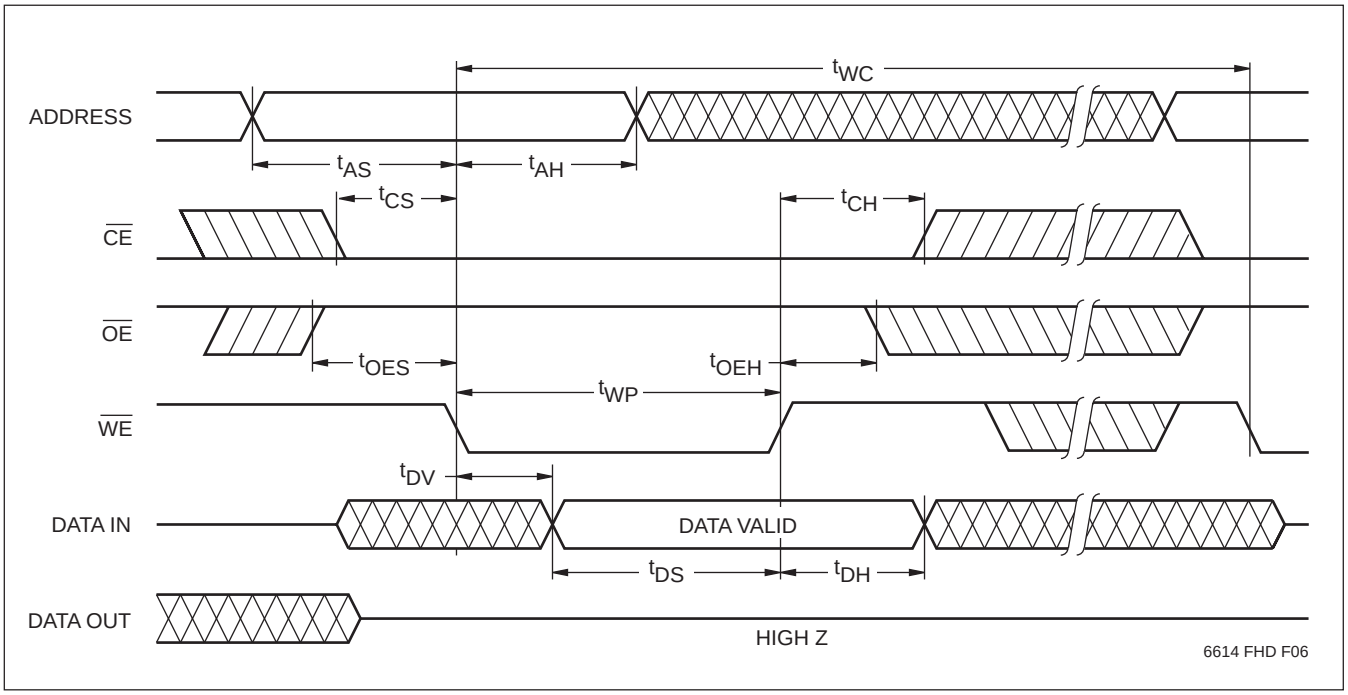
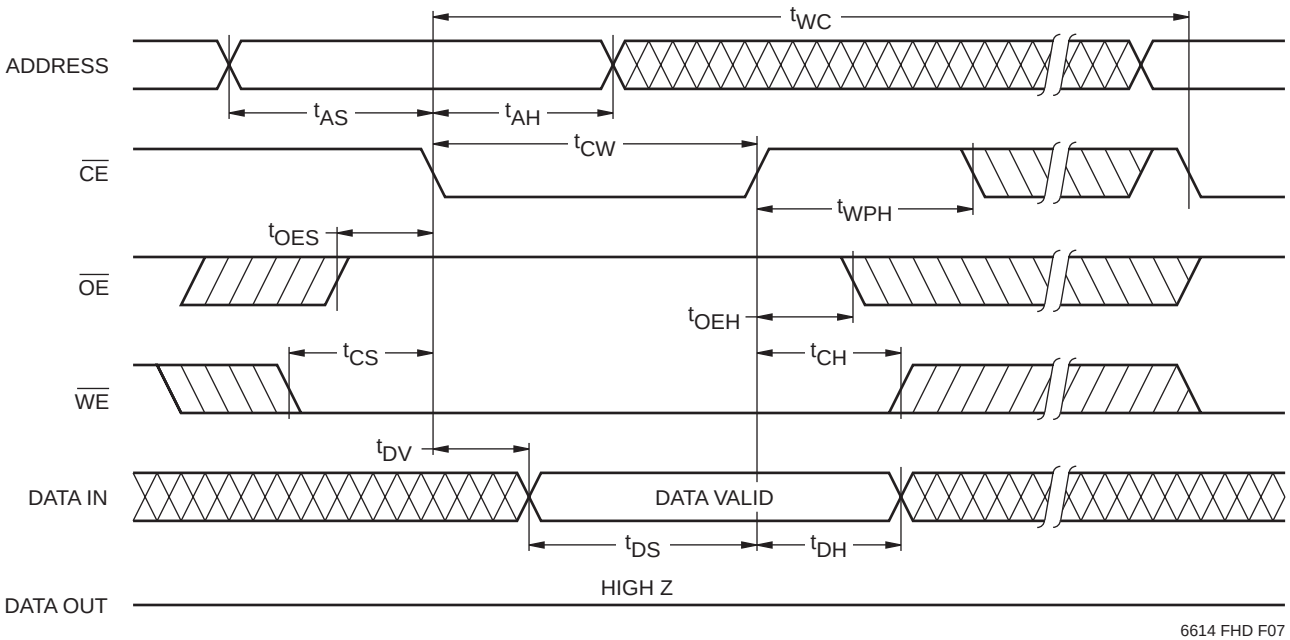
$\overline{WE}$ Controlled Write Cycle

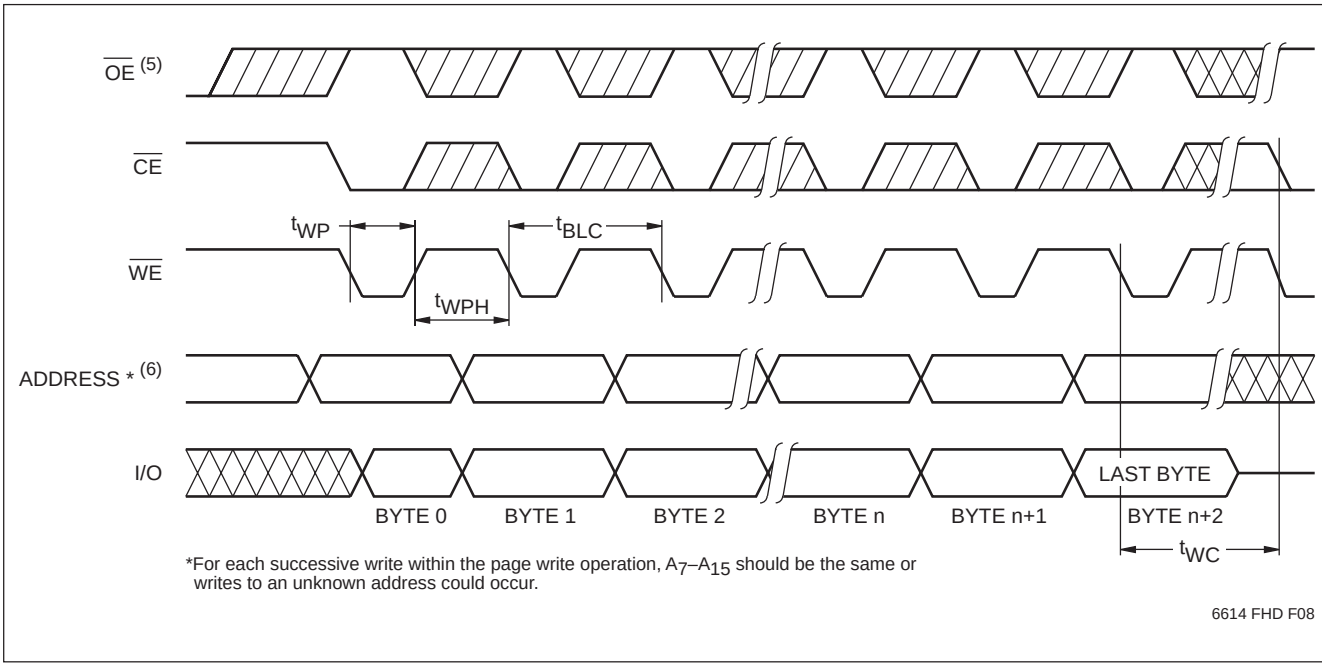


Notes: (4) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete the internal write operation.

$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

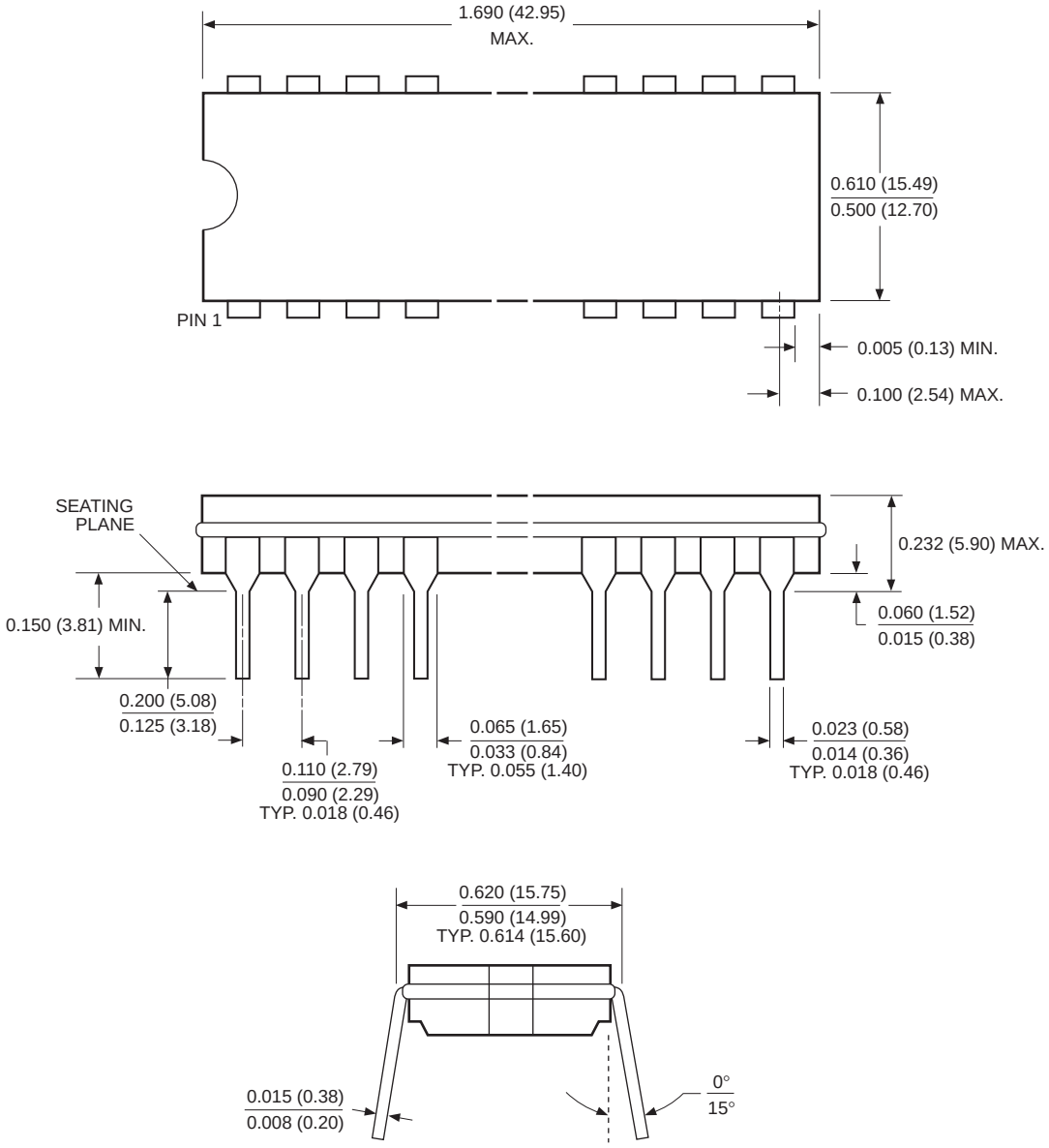


Notes: (5) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

PACKAGING INFORMATION

32-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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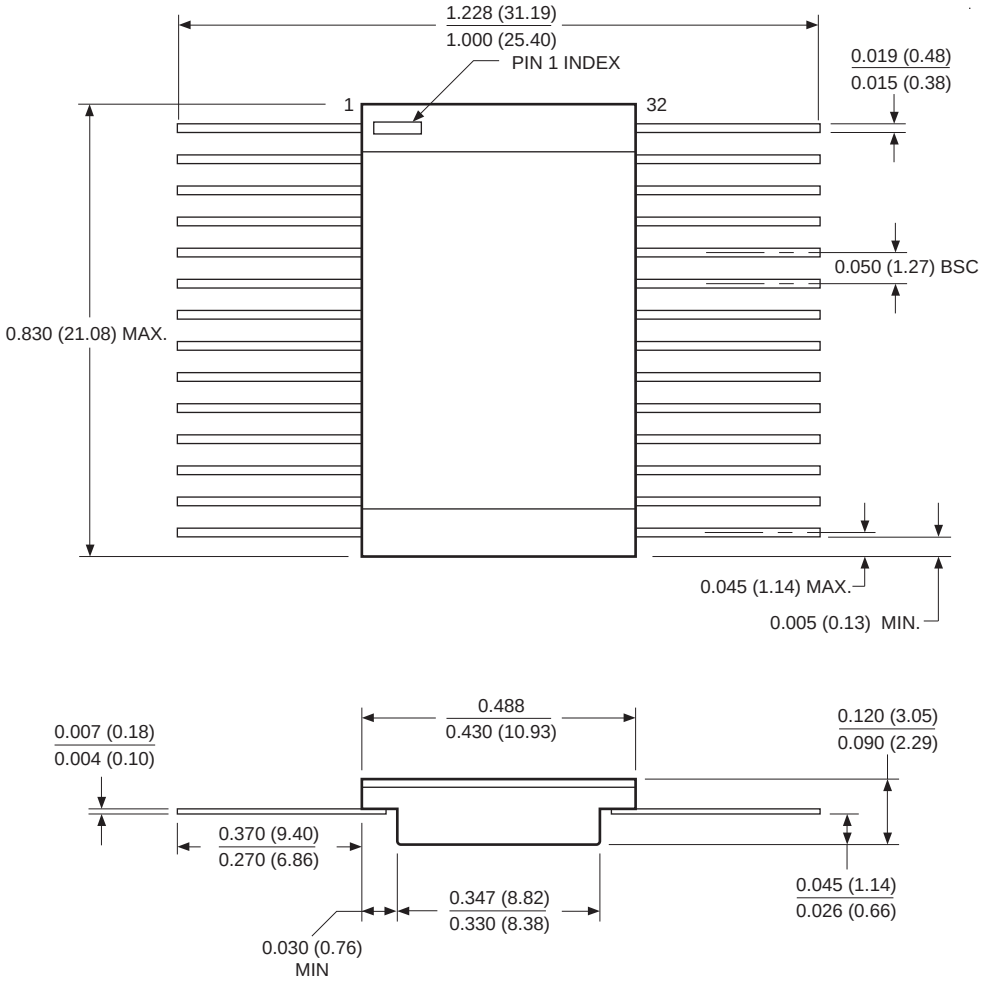
PACKAGING INFORMATION

32-LEAD CERAMIC FLAT PACK TYPE F

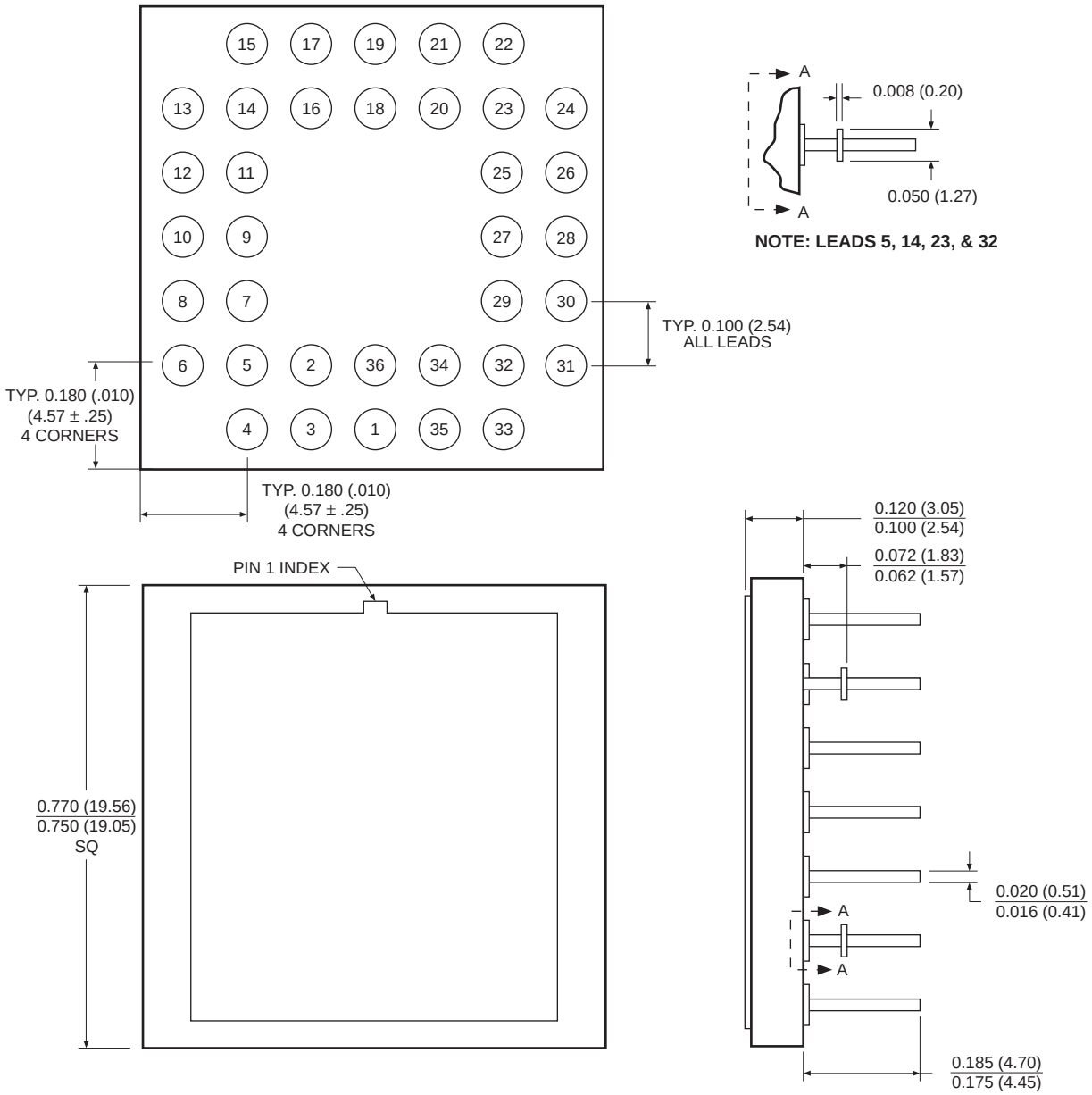


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F20

PACKAGING INFORMATION

36-LEAD CERAMIC PIN GRID ARRAY PACKAGE TYPE K



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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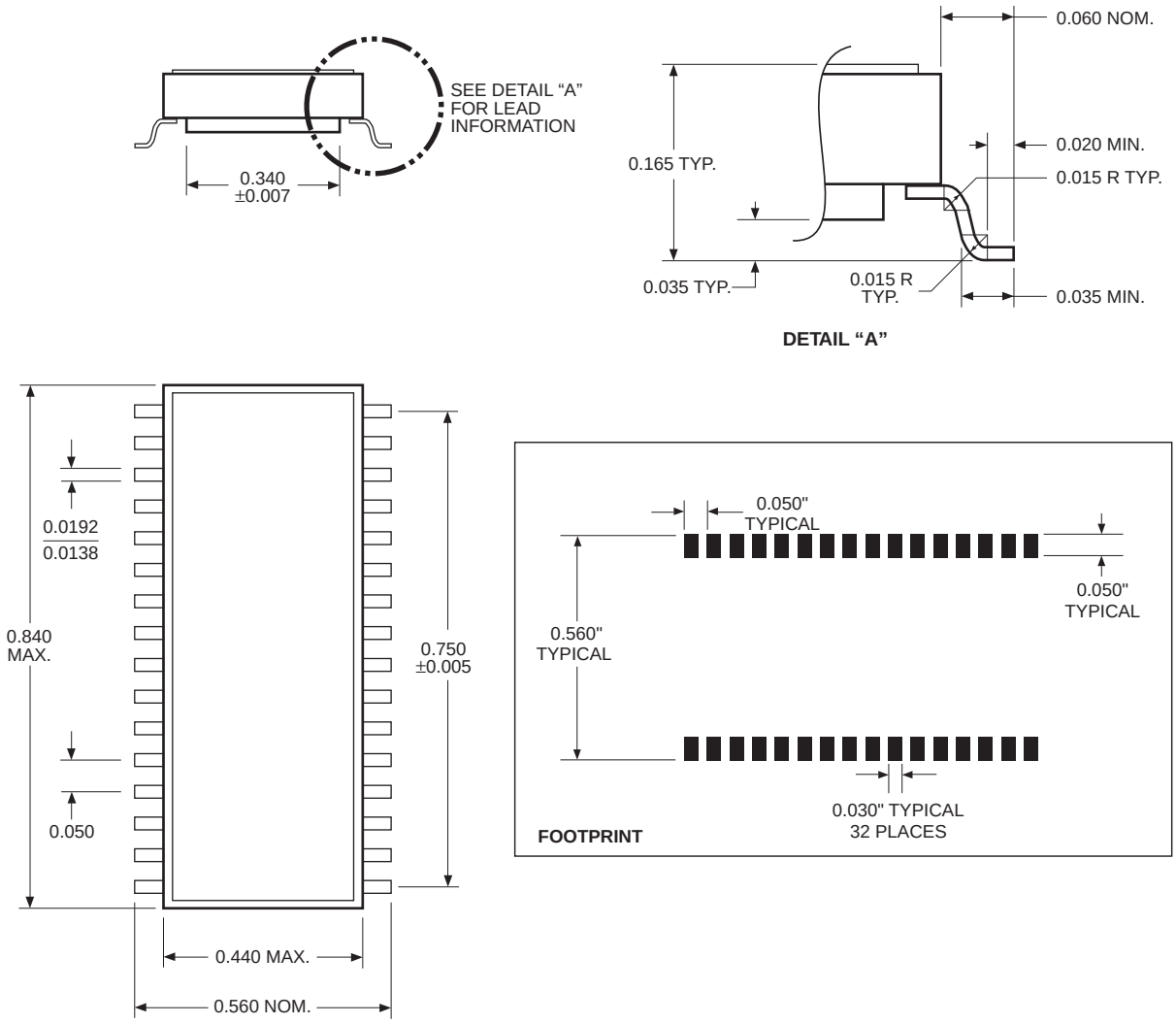
PACKAGING INFORMATION

32-LEAD CERAMIC SMALL OUTLINE GULL WING PACKAGE TYPE R



NOTES:

1. ALL DIMENSIONS IN INCHES

2. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCHES

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ORDERING INFORMATION