Low Voltage SPDT 0.8Ω Analog Switch

Features

- CMOS Technology for Bus and Analog Applications
- Low On-Resistance: 0.8Ω at 3.0V
- Wide V_{CC} Range: 1.65V to 5.5V
- Rail-to-Rail Signal Range
- Control Input Overvoltage Tolerance: 5.5V(Min)
- Fast Transition Speed: 12ns at 5.0V
- High Bandwidth: 150 MHz
- Extended Industrial Temperature Range: -40°C to 85°C
- Packaging (Pb-free & Green):
  -12-Pin TDFN 1mm×3mm

Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Battery powered Communications
- Computer Peripherals

Description

The PI5A4158 is a dual high-bandwidth, fast single-pole double-throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. The device features ultra low RON of 0.8Ω typical at 3.0V VCC and will operate over the wide VCC range of 1.65V to 5.5V.

The PI5A4158 features very low quiescent current even when the control voltage is lower than the VCC supply. This feature services the mobile handset applications very well by allowing direct interface with baseband processor general purpose I/Os.

Break-before-make switching prevents both switches being enabled simultaneously. This eliminates signal disruption during switching.

The control input, S, is independent of supply voltage.

Pin Description

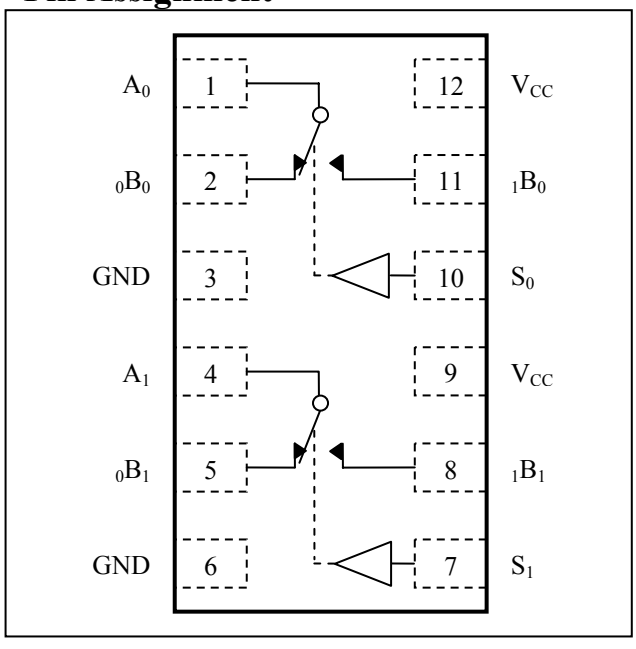
Pin No	Name	Description
8, 11	$_1B_x$	Data Port (Normally open)
3, 6	GND	Ground
2, 5	$_0B_x$	Data Port (Normally closed)
1, 4	A_X	Common Output / Data Port
9, 12	V_{CC}	Positive Power Supply
7, 10	S_X	Logic Control

Logic Function Table

Logic Input (S_X)	Function
0	$_0B_x$ Connected to A_X
1	$_1B_x$ Connected to A_X

Note: X= 0 or 1

Pin Assignment



Maximum Ratings

Storage Temperature……..-65℃ to +150℃
Ambient Temperature with Power Applied.....-40℃ to +85℃
Supply Voltage V_{CC} ……..-0.5V to +7.0V
DC Switch Voltage V_S ……-0.5V to V_{CC}+0.5V
DC Input Voltage V_{IN} … ……...-0.5V to +7.0V
DC Output Current V_{OUT}……..….128mA
DC V_{CC} or Ground Current I_{CC} /I_{GND} … ……..….±100mA
Junction Temperature under Bias (T_J) .....150°C
Junction Lead Temperature (T_L)
(Soldering, 10 seconds) .....260°C
ESD（HBM） 5KV
Power Dissipation (P_D) @ +85°C TDFN1x3 350mW

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage	-	1.65	-	5.5	V
V_{IN}	Control Input Voltage	-	0	-	V_{CC}	V
V_S	Switch Input Voltage	-	0	-	V_{CC}	V
V_{OUT}	Output Voltage	-	0	-	V_{CC}	V
T_A	Operating Temperature	-	-40	25	85	°C
t_r, t_f	Input Rise and Fall Time	Control Input V_{CC} = 2.7V to 3.6V	0	-	10	ns/V
		Control Input V_{CC} = 4.5V to 5.5V	0	-	5	ns/V

Note: Control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

(T_A = –40°C to 85°C, Typical values are at 3V and +25°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Supply Voltage	Min.	Typ.	Max.	Units
V_{IAR}	Analog Input Signal Range	-	V_{CC}	0	-	V_{CC}	V
R_{ON}	ON Resistance (1)	I_{Ax}=100mA, V_{nBx} =0V	V_{CC}=4.5V	-	0.7	1.0	Ω
		I_{Ax}=100mA, V_{nBx} =2.4V		-	0.6	0.9	
		I_{Ax}=100mA, V_{nBx} =4.5V		-	0.8	1.1	
		I_{Ax}=100mA, V_{nBx} =0V	V_{CC}=3.0V	-	0.8	1.2	Ω
		I_{Ax}=100mA, V_{nBx} =3.0V		-	0.9	1.8	
		I_{Ax}=100mA, V_{nBx} =0V	V_{CC}=2.3V	-	1.0	1.3	Ω
		I_{Ax}=100mA, V_{nBx} =2.3V		-	1.2	1.7	
		I_{Ax}=100mA, V_{nBx} =0V	V_{CC}=1.65V	-	1.3	1.8	Ω
		I_{Ax}=100mA, V_{nBx} =1.65V		-	2.0	2.6	
ΔR_{ON}	ON Resistance Match Between Channels (1,2,3)	I_{Ax}=100mA, V_{nBx} =3.15V	V_{CC}=4.5V	-	0.01	0.03	Ω
		I_{Ax}=100mA, V_{nBx} =2.1V	V_{CC}=3.0V	-	0.02	0.04	
		I_{Ax}=100mA, V_{nBx} =1.6V	V_{CC}=2.3V	-	0.03	0.06	
		I_{Ax}=100mA, V_{nBx} =1.15V	V_{CC}=1.65V	-	0.03	0.06	
R_{ONF}	ON Resistance Flatness (1,2,4)	I_{Ax}=100mA, V_{nBx} =0V,2.4V,4.5V	V_{CC}=4.5V	-	0.2	0.4	Ω
		I_{Ax}=100mA, V_{nBx} =0V,1.5V,3.3V	V_{CC}=3.3V	-	0.2	0.4	
		I_{Ax}=100mA, V_{nBx} =0V,1.1V,2.5V	V_{CC}=2.5V	-	0.4	0.6	
		I_{Ax}=100mA, V_{nBx} =0V, 0.7V,1.8V	V_{CC}=1.8V	-	1.0	1.4	
V_{IH}	Input High Voltage	Logic High Level	V_{CC}=1.65V	-	0.9	-	V
			V_{CC}=2.3V	-	1.0	-	
			V_{CC}=3.0V	-	1.1	-	
			V_{CC}=4.2V	-	1.2	-	
			V_{CC}=5.5V	-	1.3	-	
V_{IL}	Input Low Voltage	Logic Low Level	V_{CC}=1.65V	-	-	0.6	V
			V_{CC}=2.3V	-	-	0.6	
			V_{CC}=3.0V	-	-	0.6	
			V_{CC}=4.2V	-	-	0.8	
			V_{CC}=5.5V	-	-	0.8	
$I_{OFF(Bn)}$	Source Off Leakage Current	V_{Ax}=1V/4.5V, V_{nBx}=1V/4.5V	V_{CC}=3.0V	-20	-	+20	nA
$I_{ON(A, Bn)}$	Channel On Leakage Current	-	V_{CC}=1.65V to 5.5V	-40	-	+40	nA
I_{CC}	Quiescent Supply Current	All Channels ON or OFF, V_{nBx}=V_{CC} and GND, I_{OUT}=0A	V_{CC}=3.6V	-	0.004	0.2	µA
			V_{CC}=5.5V	-	0.004	0.2	
I_{CCT}	Increase in I_{CC} per Input	Channel Input at 2.7V	V_{CC}=4.3V	-	0.2	10.0	µA

Notes:

1. Measured by voltage drop between A and B pins at the indicated current through the device. ON resistance is determined by the lower of the voltages on two ports (Ax or nBx) x= 0 or 1, n= 0 or 1.
2. Parameter is characterized but not tested in production.
3. $\Delta R_{ON} = R_{ON}$ max – R_{ON} min. measured at identical V_{CC}, temperature and voltage levels.
4. Flatness is defined as difference between maximum and minimum value of ON resistance over the specified range of conditions.

Capacitance(1)

Symbol	Parameter	Test Conditions	Supply Voltage	Temp (°C)	Min.	Typ.	Max.	Units
C_{IN}	Control Input	f = 1 MHz	V_{CC} = 5.0V	T_A = 25°C	-	3.5	-	pF
C_{IO-B}	For Bn Port, Switch OFF				-	15.0	-	
C_{IOA-ON}	For An Port, Switch ON				-	34.0	-	

Notes:

1. Capacitance is characterized but not tested in production

Switch and AC Characteristics (1)

Parameter	Description	Test Conditions	Supply Voltage	Min	Typ	Max	Units
t_{BBM}	Break Before Make Time	See Figure 2	V_{CC} = 2.7V to 3.6V	-	10	20	ns
			V_{CC} = 4.5V to 5.5V	-	6	12	
t_{ON}	Turn on Time	See Figure 1	V_{CC} = 2.7V to 3.6V	-	12	25	
			V_{CC} = 4.5V to 5.5V	-	9	18	
t_{OFF}	Turn off Time	See Figure 1	V_{CC} = 2.7V to 3.6V	-	17	35	
			V_{CC} = 4.5V to 5.5V	-	10	20	
Q	Charge Injection	C_L = 1nF, V_{GEN} = 0V, R_{GEN}=0Ω. See Figure 3	V_{CC} = 5.0V	-	35	-	pC
			V_{CC} = 3.3V	-	25	-	
OIRR	Off Isolation	R_L=50Ω, V_{GEN}=0V, R_{GEN} =0Ω, f =1MHz. See Figure 4 (2)	V_{CC} =1.65V to 5.5V	-	-70	-	dB
X_{TALK}	Crosstalk Isolation	f=1MHz, See Figure 5	V_{CC} =1.65V to 5.5V	-	-70	-	
f_{3dB}	–3dB Bandwidth	See Figure 8	V_{CC} =1.65V to 5.5V	-	150	-	MHz
T_{HD}	Total Harmonic Distortion	R_L=600Ω, V_{IN}=0.5Vpp, f=20Hz to 20kHz See Figure 9	V_{CC} =2.7V to 4.2V	-	0.015	-	%

Notes:
1. Guaranteed by design.
2. Off Isolation = 20 Log_{10} [V_{nBx} /V_{Ax}] and is measured in dB.

Test Circuits and Timing Diagrams

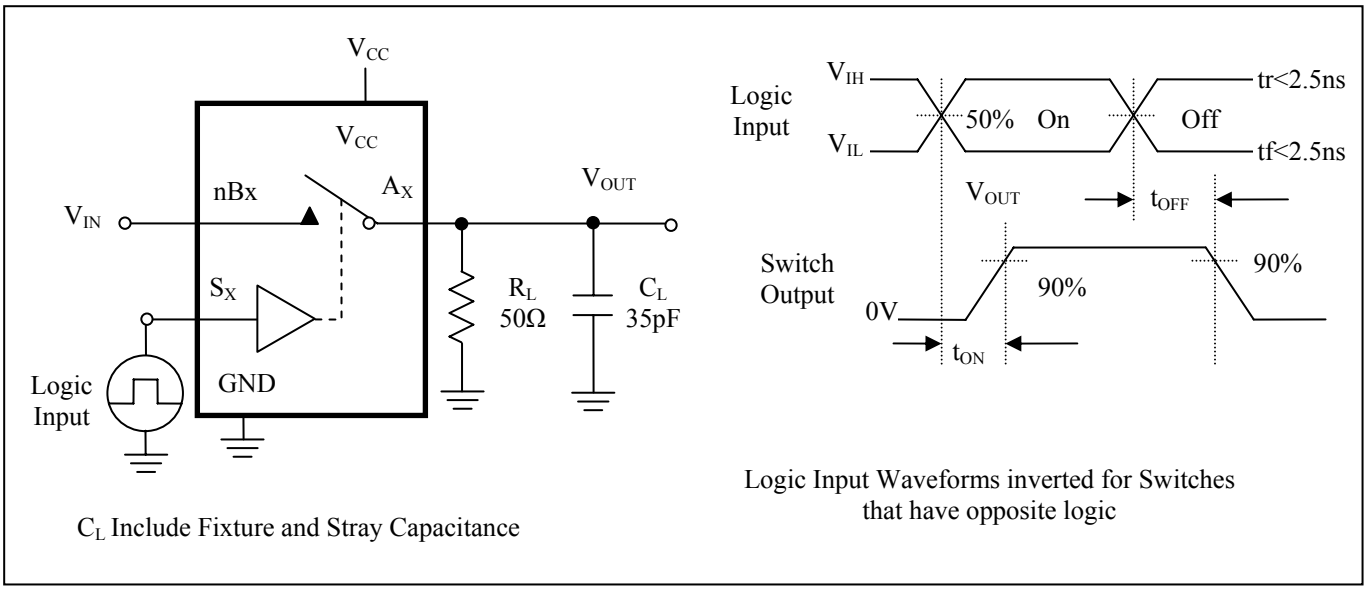


Figure 1. Turn ON/OFF Timing

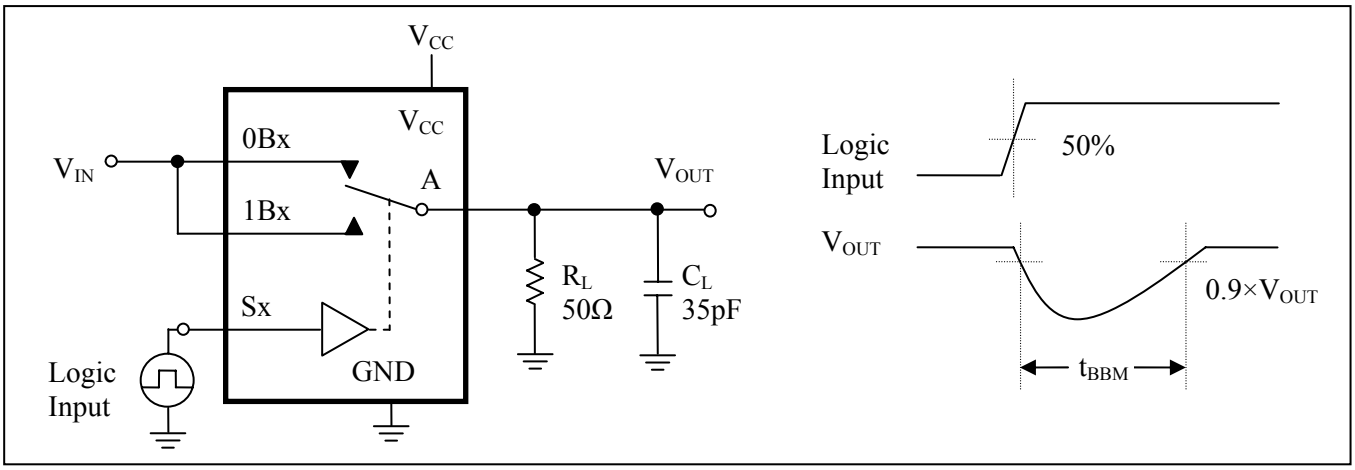


Figure 2. Break Before Make Interval Timing

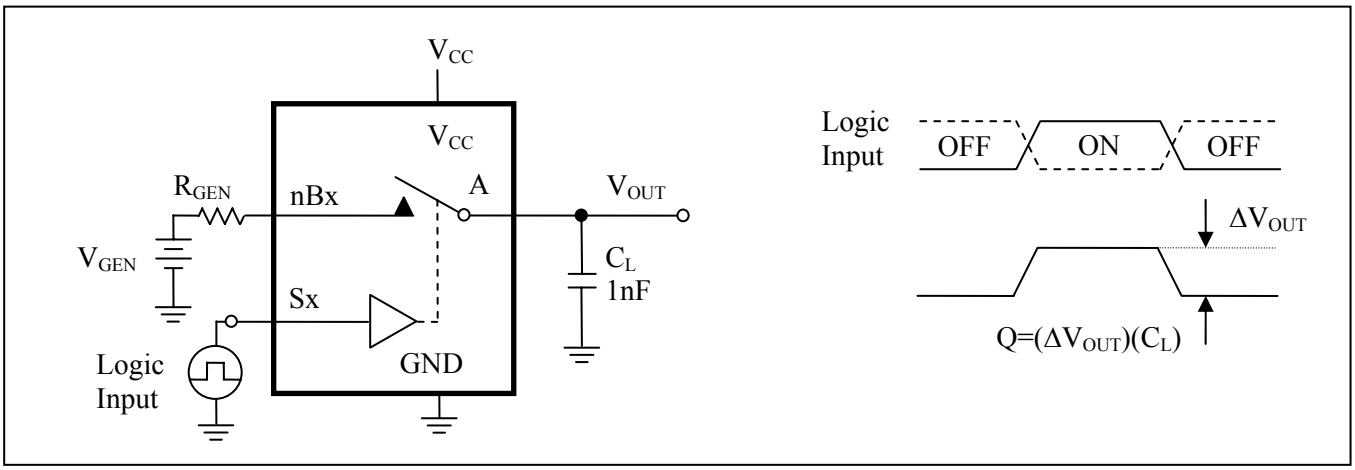


Figure 3. Charge Injection Test

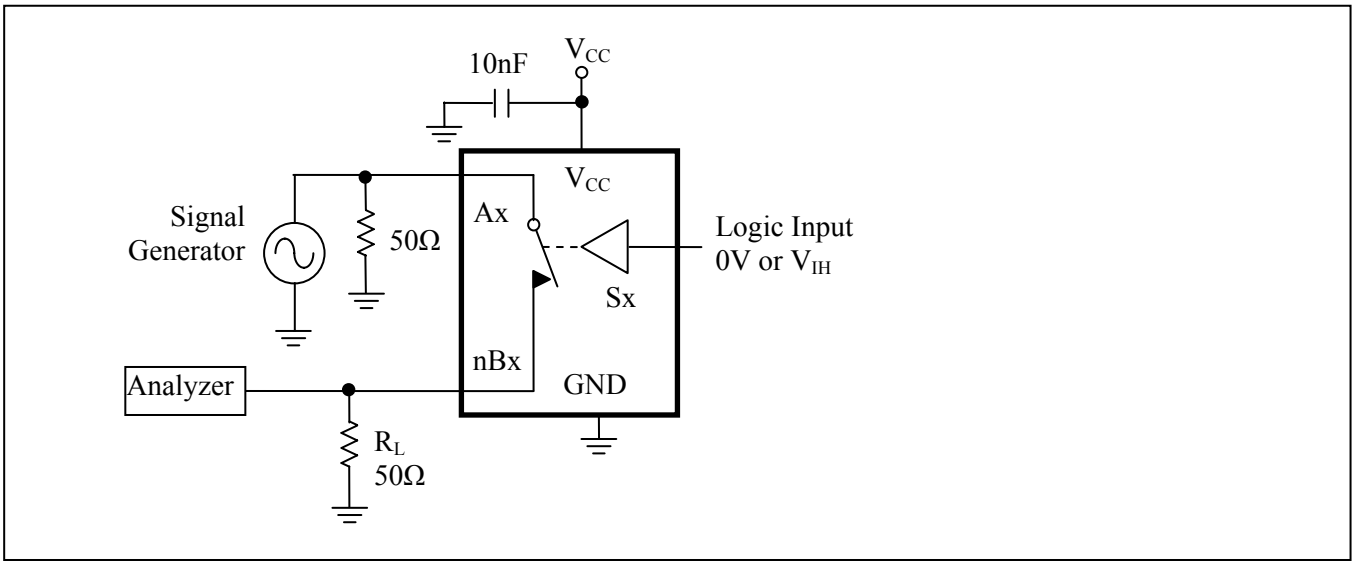


Figure 4. Off Isolation

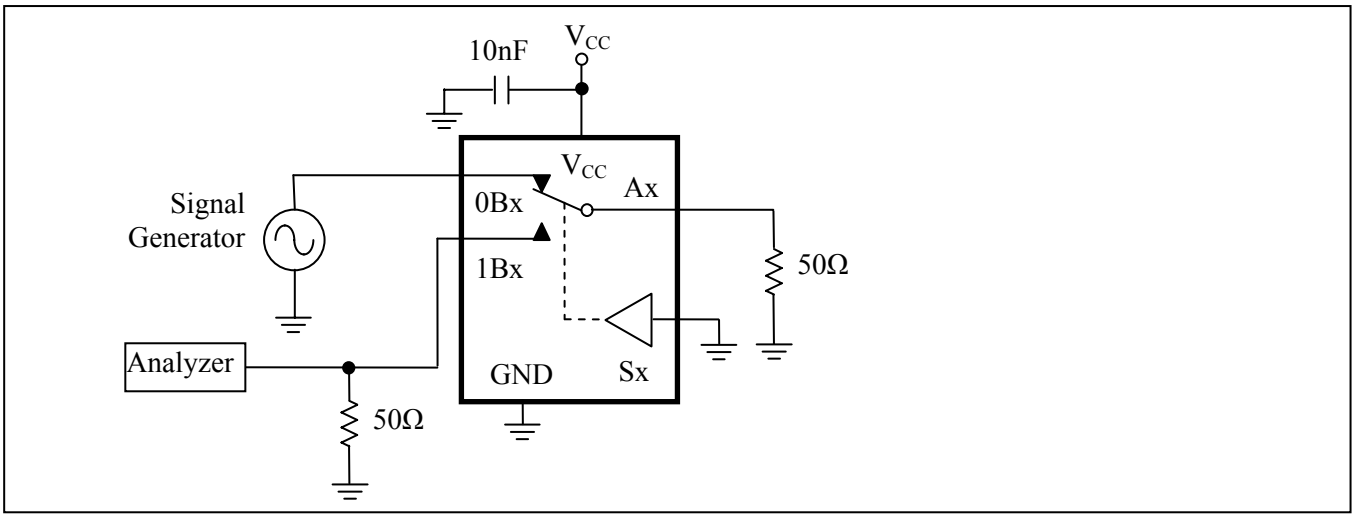


Figure 5. Crosstalk

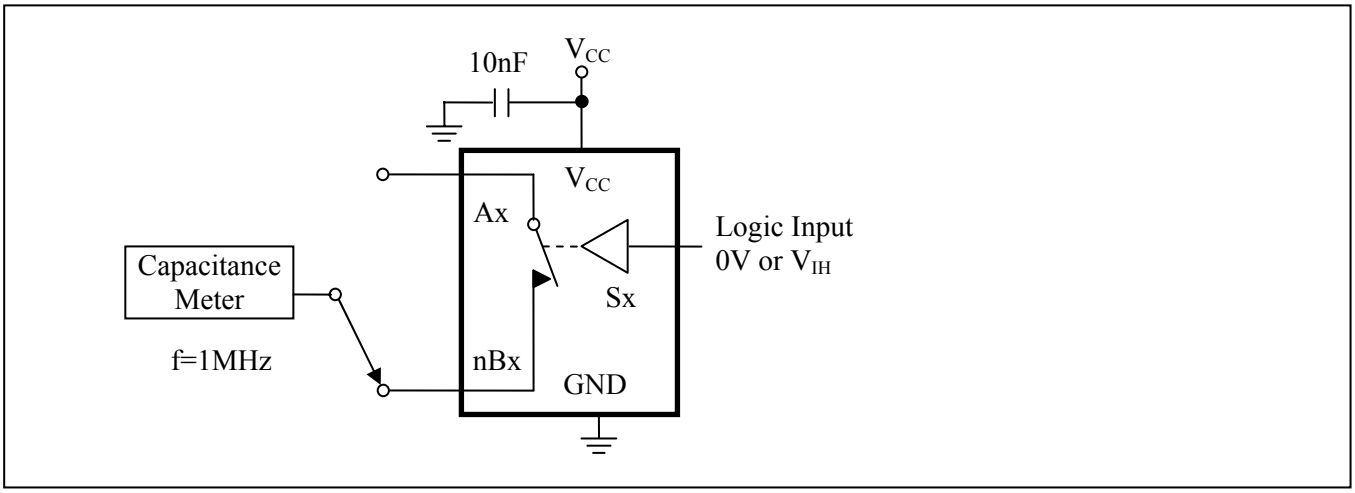


Figure 6. Channel Off Capacitance

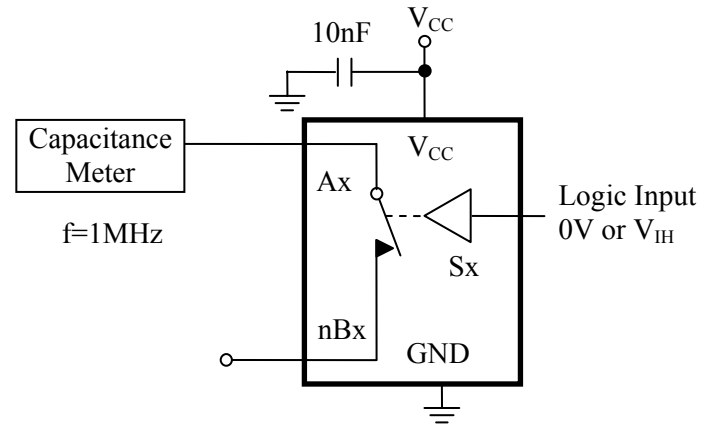


Figure 7. Channel On Capacitance

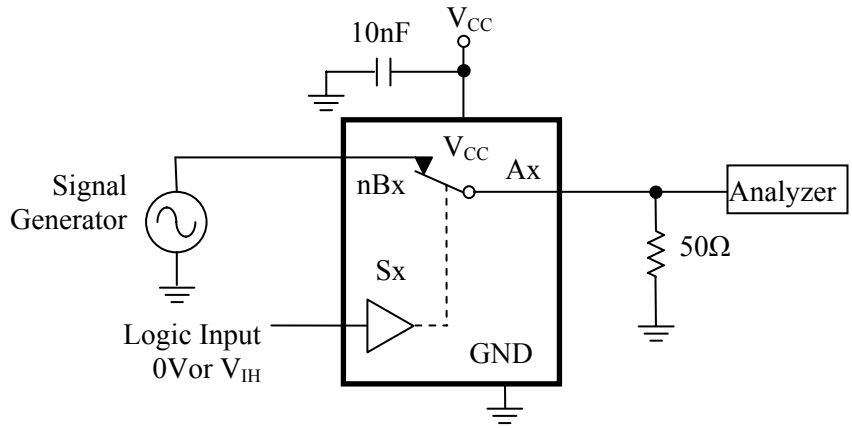


Figure 8. Bandwidth

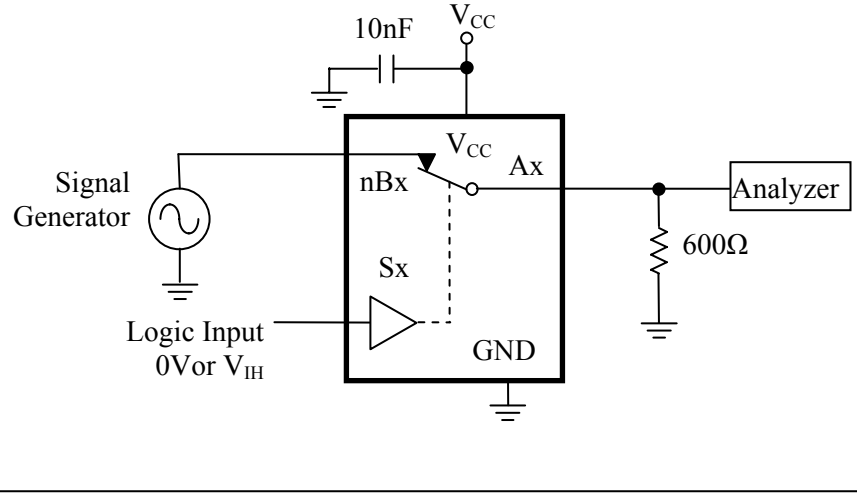
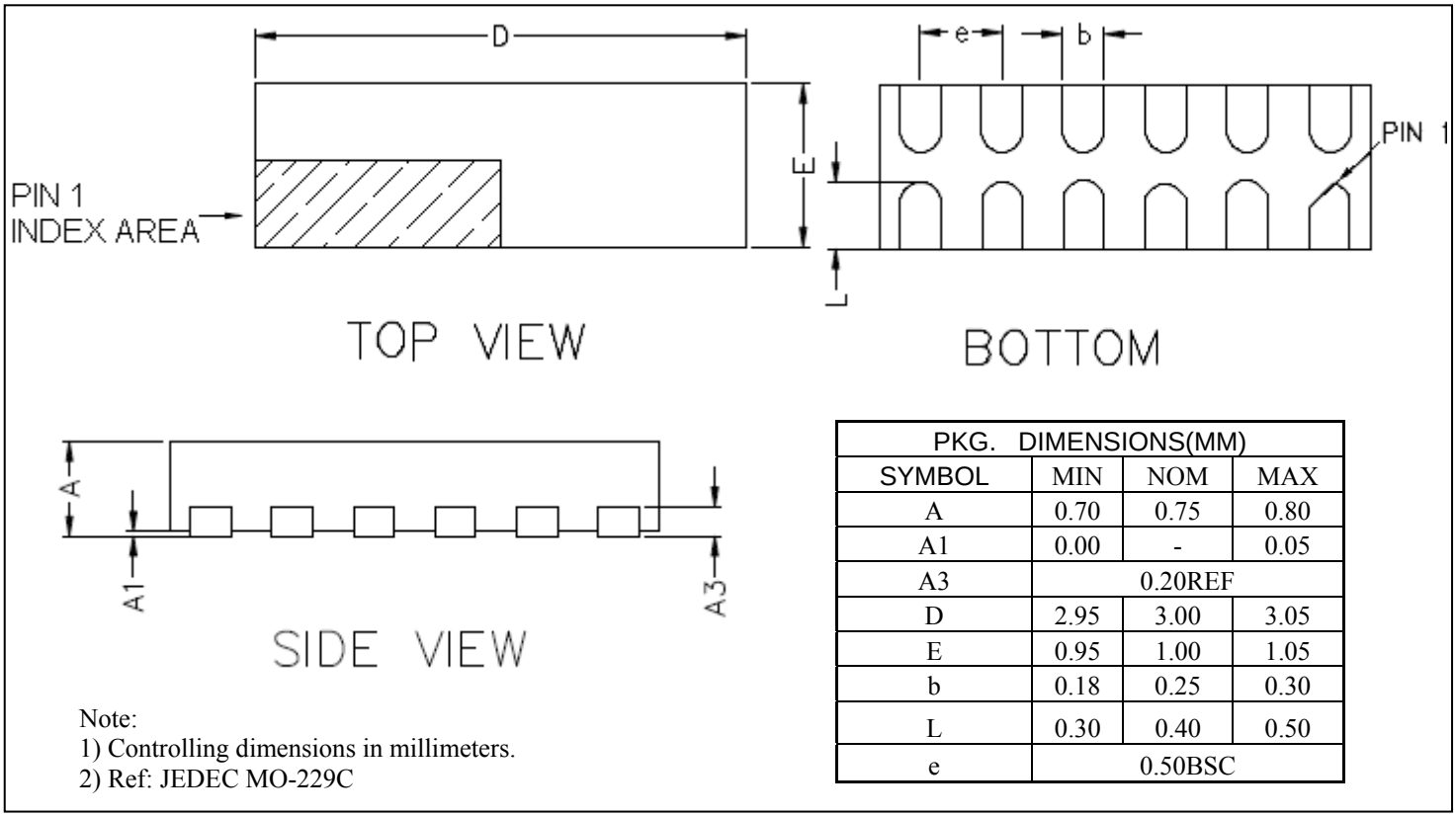


Figure 9. Harmonic Distortion

Mechanical Information

ZA (12-pin TDFN 1×3)



PKG. DIMENSIONS(MM)			
SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.20REF	
D	2.95	3.00	3.05
E	0.95	1.00	1.05
b	0.18	0.25	0.30
L	0.30	0.40	0.50
e		0.50BSC	

Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC MO-229C

Ordering Information

Part Number	Package Code	Package	Top Marking
PI5A4158ZAE	ZA	Lead Free and Green TDFN-12 1×3 (ZA)	nP

Notes:
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel