# THAT Corporation

**Audio Preamplifier**
**Digital Controller IC**

## THAT 5173

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## FEATURES

- Wide gain range: 0 to 60dB in 3dB steps
- Wide supply range: ±5V to ±17V
- Wide output swing:+27dBu (±17V sup.)
- Wide input swing: +27dBu (±17V sup.)
- Low THD+N: <0.001% @1kHz, up to 42dB gain
- Integrated differential servo minimizes output offset
- Zero-crossing detector minimizes switching noise
- Daisy Chainable SPI interface
- Four general-purpose digital outputs
- Small 5mm x 5mm QFN24 package

## APPLICATIONS

- Digitally controlled microphone preamplifiers
- Digitally-controlled instrumentation amplifiers
- Digitally-controlled differential amplifiers
- Audio mixing consoles
- PC audio breakout boxes
- Audio distribution systems
- Digital audio snakes
- Portable audio recorders

## Description

The THAT5173 is a digital gain controller for low-noise, analog, differential, current-feedback audio preamplifiers such as the THAT 1570. When used in conjunction with an appropriate analog gain block, the 5173 supports digitally control gain from 0dB to 60dB in 3dB steps, while preserving low noise and distortion. It operates from ±5V to ±17V analog supplies, supporting input signal levels as high as +27 dBu (at 0dB gain and ±17V supplies) in combination with the 1570 -- without an input pad. The 5173 includes a differential servo and zero-crossing detector to minimize dc offsets and glitches (zipper noise) during gain adjustments.

The 5173 is controlled via an industry standard serial-peripheral interface (SPI) port. Four General Purpose Outputs (GPOs) can be controlled via this interface. The GPOs may be used to control auxiliary functions such as input selectors, filters, mutes, LEDs, relays, etc.

The 5173 was designed to mate perfectly with the THAT 1570 Differential Audio Preamplifier IC. Together, these combinations provide a high performance solution for digitally-controllable audio preamplifier applications. However, the 5173 may also be used to control a discrete preamplifier.

Fabricated in a high-voltage CMOS process, the 5173 integrates an astonishing amount of circuitry within a very small package. It comes in a small (5x5 mm) 24-pin QFN package, making it suitable for small portable devices.
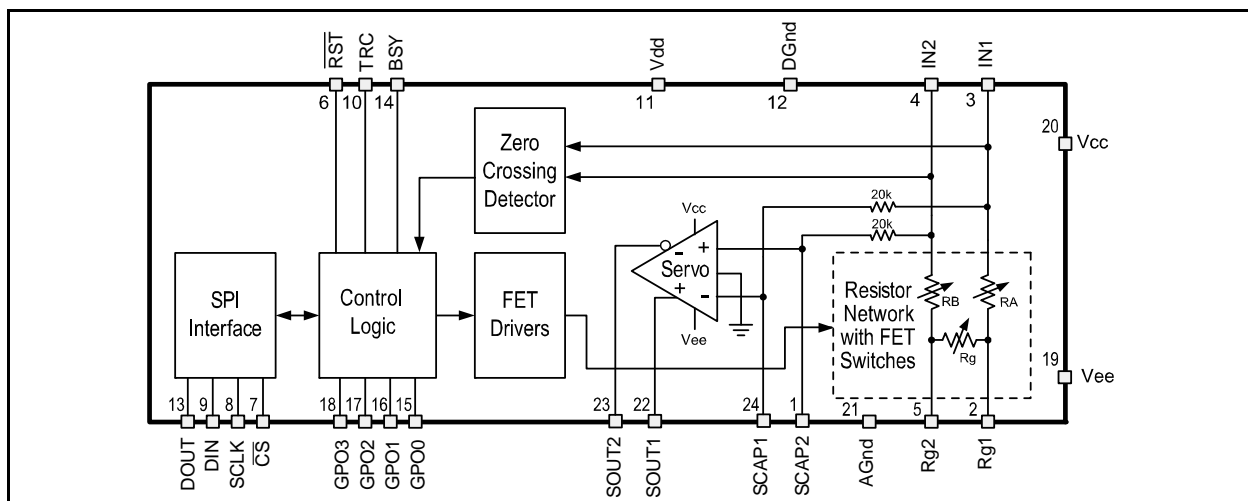


Figure 1. THAT 5173 Block Diagram

| Pin Number | Pin Name | Pin Description |
|---|---|---|
| 1 | SCAP2 | DC Servo Capacitor Input 2 |
| 2 | RG1 | Attenuator Network Output 1 [Connects to preamplifier feedback 1 (RG1)] |
| 3 | IN1 | Attenuator Network Input 1 [Connects to preamplifier output 1] |
| 4 | IN2 | Attenuator Network Input 2 [Connects to preamplifier Output 2] |
| 5 | RG2 | Attenuator Network Output 2 [Connects to preamplifier feedback Input 2 (RG2)] |
| 6 | RST' | Reset Input (Active Low) |
| 7 | CS' | Chip Select Input (Active Low) |
| 8 | SCLK | Serial Clock Input |
| 9 | DIN | Serial Data Input |
| 10 | TRC | R/C Timeout or External Clock Input |
| 11 | VDD | Logic Positive Power Supply |
| 12 | DGND | Logic Ground Reference |
| 13 | DOUT | Serial Data Output |
| 14 | BSY | Busy Output (Active High) |
| 15 | GPO0 | General Purpose Output 0 |
| 16 | GPO1 | General Purpose Output 1 |
| 17 | GPO2 | General Purpose Output 2 |
| 18 | GPO3 | General Purpose Output 3 |
| 19 | VEE | Negative Analog Supply Voltage |
| 20 | VCC | Positive Analog Supply Voltage |
| 21 | AGND | Analog Ground Reference |
| 22 | SOUT1 | DC Servo Output 1 |
| 23 | SOUT2 | DC Servo Output 2 |
| 24 | SCAP1 | DC Servo Capacitor Input 1 |
| Thermal Pad | PAD | Connected internally to VEE. Solder to PCB (optionally connect to VEE) for optimal performance. |

Table 1. Pin Assignments

## SPECIFICATIONS[1]

### Absolute Maximum Ratings[2,3]

| | | | |
|---|---|---|---|
| Total Analog Supply Voltage ($V_{CC}$-$V_{EE}$) | 36 V | Minimum Analog Voltage at IN1, IN2 ($V_{IAMin}$) | $V_{EE}$ |
| Positive Analog Supply Voltage ($V_{CC}$-$A_{GND}$) | 18 V | Maximum Digital Input Voltage ($V_{IDMax}$) | $V_{DD}$ + 0.3 V |
| Negative Analog Supply Voltage ($V_{EE}$-$A_{GND}$) | -18 V | Minimum Digital Input Voltage ($V_{IDMin}$) | $D_{GND}$ - 0.3 V |
| Digital Supply Voltage ($V_{DD}$-$D_{GND}$) | 4.5 V | Storage Temperature Range ($T_{STG}$) | -40 to +125 ºC |
| Analog and Digital Ground Difference ($D_{GND}$-$A_{GND}$) | ±0.3 V | Operating Temperature Range ($T_{OP}$) | -40 to +85 ºC |
| Maximum Analog Voltage at IN1, IN2 ($V_{IAMax}$) | $V_{CC}$ | Junction Temperature ($T_{JMAX}$) | +125 ºC |
| Maximum Current Through $V_{DD}$, $D_{GND}$ | 100 mA | | |

### Electrical Characteristics[2,4]

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Analog Supply Voltage | $V_{CC}$; -$V_{EE}$ | Referenced to $A_{GND}$ | 4.75 | — | 17 | V |
| Digital Supply Voltage | $V_{DD}$ | Referenced to $D_{GND}$ | 3.0 | — | 3.6 | V |
| Analog Supply Current | $I_{CC}$; -$I_{EE}$ | No Signal | — | 7.6 | 10 | mA |
| Digital Supply Current | $I_{DD}$ | No Signal | — | 2 | 11 | µA |
| **Resistor Ladder Characteristics (DC)** | | | | | | |
| Gain Range [-20log ($V_{IN1}$-$V_{IN2}$)/($V_{RG}1$-$V_{RG2}$)] | | $V_{CC}$ -1.6 > $V_{IN1}$ >$V_{EE}$+1.6  $V_{CC}$ -1.6 > $V_{IN2}$ >$V_{EE}$ +1.6 | 0 | — | 60 | dB |
| Gain Step Size | | 0dB ≤ Gain ≤ 60dB | — | 3 | — | dB |
| Gain Error | | All gain settings | -0.5 | ±0.2 | 0.5 | dB |
| $R_G$ Range (Resistance from $IN_1$ to $IN_2$) | | All gain settings | 13.7 | 17.1~12.1k | open | Ω |
| $R_A$, $R_B$ Range (Resistance from $IN_1$ to $Rg_1$)  (Resistance from $IN_2$ to $Rg_2$) | | All gain settings | 2.0 | 2.5~8.6 | 10.3 | kΩ |
| **Servo Amp Characteristics (DC)** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | Includes bias current effects | -1.75 | — | +1.75 | mV |
| Power Supply Rejection Ratio | PSRR | $V_{CC}$ = -$V_{EE}$; ±5V to ±15V | 100 | 115 | — | dB |
| Maximum Output Voltage | $V_{OMax}$ | | $V_{CC}$-4.5 | — | — | V |
| Minimum Output Voltage | $V_{OMin}$ | | — | — | $V_{EE}$+4.5 | V |
| Maximum Output Current | $I_{OMax}$ | | 0.70 | 1.0 | — | mA |

1. All specifications are subject to change without notice.

2. Unless otherwise noted, $T_A$=25ºC, $V_{CC}$=+15V, $V_{EE}$= -15V, $V_{DD}$= +3.3V

3. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not impli ed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4. 0 dBu = 0.775 Vrms

## Electrical Characteristics (con't)[1,3,4]

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Zero-Crossing Detector Characteristics (DC)** | | | | | | |
| Zero-Crossing Detector Threshold | | | — | ±12.5 | — | mV |
| ZCD Timeout | $t_{ZTO}$ | $R_T = 22M\Omega$, $C_T = 1$ nF | — | 22 | — | ms |
| ZCD Timing Capacitor | $C_T$ | | | 1 | 2 | nF |
| ZCD Timing Resistor | $R_T$ | | 1k | 22M | 100M | $\Omega$ |
| **AC Characteristics** | | | | | | |
| THD+N (Differential signal applied to f = 1 kHz, Gain = 21 dB, $IN_1$, $IN_2$, measured at $RG_1$, $RG_2$) $V_{IN1} - V_{IN2} < = +22$ dBu | | | — | 0.001 | — | % |
| Maximum Signal Voltage at $IN_1$, $IN_2$ | | | — | $V_{CC} - 2.5$ | — | V |
| Minimum Signal Voltage at $IN_1$, $IN_2$ | | | — | $V_{EE} + 2.5$ | — | V |
| Maximum Signal Voltage at $RG_1$, $RG_2$ | | | — | $V_{CC} - 2.5$ | — | V |
| Minimum Signal Voltage at $RG_1$, $RG_2$ | | | — | $V_{EE} + 1.5$ | — | V |

| Electrical Characteristics (con't)[1,3,4] | | | | | |
|---|---|---|---|---|---|
| Parameter | Symbol | Min | Typ | Max | Units |
| **Digital I/O and Switching Characteristics** | | | | | |
| High-Level Input Voltage | $V_{IH}$ | 0.7 x $V_{DD}$ | – | – | V |
| Low-Level Input Voltage | $V_{IL}$ | – | – | 0.3 x $V_{DD}$ | V |
| High-Level Output Voltage at Io = 4 mA | $V_{OH}$ | 0.8 x $V_{DD}$ | – | – | V |
| Low-Level Output Voltage at Io = - 4 mA | $V_{OL}$ | – | – | 0.4 | V |
| Input Leakage Current | $I_{in}$ | – | 2 | – | $\mu$A |
| Input Capacitance | | – | 3.5 | – | pF |
| SCLK Frequency | $f_{SCK}$ | – | – | 10 | MHz |
| SCLK Low Time | $t_{SCL}$ | 40 | – | – | ns |
| SCLK High Time | $t_{SCH}$ | 40 | – | – | ns |
| DIN to SCLK Rising Setup | $t_{DSU}$ | 15 | – | – | ns |
| SCLK Rising to DIN Hold Time | $t_{DH}$ | 15 | – | – | ns |
| $\overline{CS}$ Enabled to SCLK High | $t_{CSCR}$ | 50 | – | – | ns |
| $\overline{RST}$ Release to CS Active | $t_{SRS}$ | 100 | – | – | ns |
| $\overline{CS}$ Enabled to DOUT Active | $t_{CSDA}$ | 100 | – | – | ns |
| $\overline{CS}$ Release to DOUT Tristate | $t_{CSDH}$ | 5 | – | 20 | ns |
| SCLK Falling to DOUT Valid | $t_{CFDO}$ | – | – | 15 | ns |
| $\overline{CS}$ High Time Between Transmissions | $t_{CSH}$ | 25 | – | – | $\mu$s |
| $\overline{CS}$ Release to SCLK Rising | $t_{CSRCR}$ | 100 | – | – | ns |
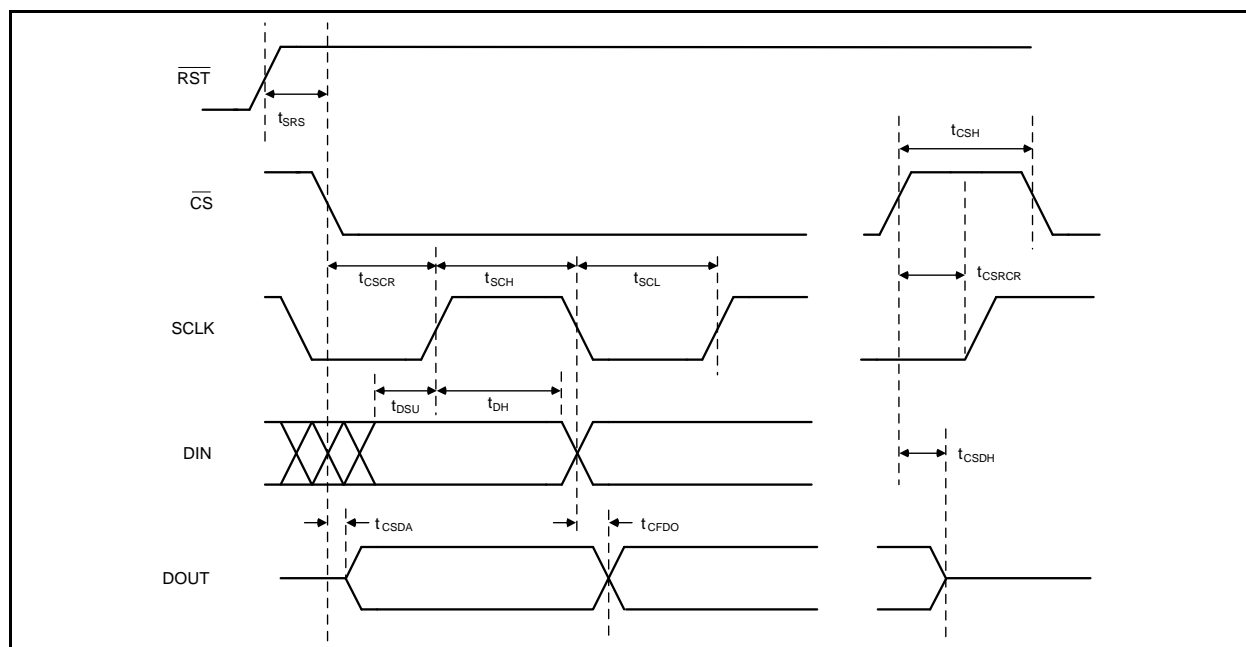


Figure 2. SPI Timing.

# Theory of Operation

The THAT 5173 contains a set of precision resistors, switched by a set of CMOS FET switches, configured to create a variable, switched, differential attenuation network. The network's impedances are ideal for controlling gain in low-voltage-noise, current-feed- back instrumentation amplifiers, and are optimized for low source impedance applications.

## Using the 5173

The attenuator is intended primarily for use in the feedback loop of differential current-feedback gain stages, such as the THAT 1570. Designed specifically for use in high-performance microphone preamplifiers, THAT's engineers paid careful attention to precision, stability, and control over the resistors and their switches, in order to maintain excellent audio performance over a wide range of gains and signal levels.

Figure 3 shows the analog portion of the 5173 connected to a 1570. Resistors $R_A$, $R_B$, and $R_G$ form a differential attenuator ("U-pad"). The amplifier's dif-
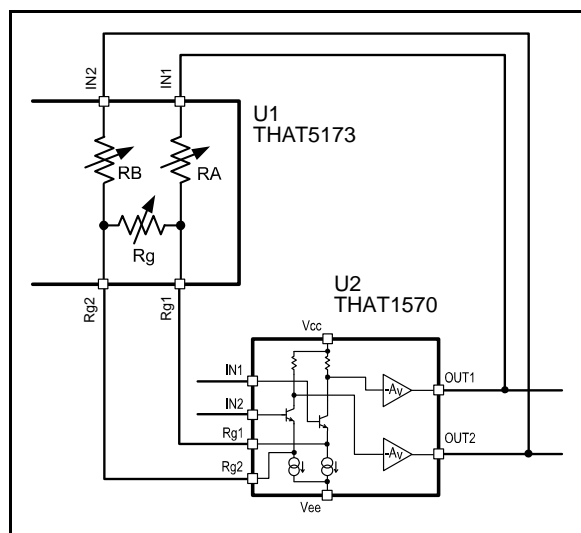


Figure 3. 5173 analog connections to a 1570.

ferential output is applied to $R_A$ and $R_B$. The output of the attenuator, appearing across $R_G$, is connected to the inverting differential input of the dual current-feedback amplifiers (the $R_{G1}$ and $R_{G2}$ pins). The voltage divider ratio thus controls the differential gain of the circuit.

The 5173 changes the attenuator settings based on the gain command provided via the SPI control interface. At 0dB gain $R_G$ is an open circuit and $R_A = R_B = 2.5k\Omega$. At +3dB gain, $R_G$ is ~12.12k$\Omega$, while $R_A = R_B = $ ~2.5k$\Omega$. To achieve other gains, all three resistors are varied by CMOS switches in order to produce 3dB gain steps from 0 to +60dB. At all gains, the impedance levels are chosen to minimize noise and distortion within the circuit as a whole.

Table 2 lists the typical internal attenuator resistor values for each gain setting.

| Gain Setting | Rg (Ohms) | Ra, Rb (Ohms) | "Gain" Register |
|---|---|---|---|
| 0 | Inf | 2,500 | 0 |
| 3 | 12,120.2 | 2,500 | 1 |
| 6 | 8,580.5 | 4,269.9 | 2 |
| 9 | 3,044.5 | 2,768 | 3 |
| 12 | 3,044.5 | 4,537.9 | 4 |
| 15 | 3,044.5 | 7,037.9 | 5 |
| 18 | 1,080.2 | 3,750.1 | 6 |
| 21 | 1,080.2 | 5,520 | 7 |
| 24 | 1,080.2 | 8,020 | 8 |
| 27 | 383.3 | 4,098.6 | 9 |
| 30 | 383.3 | 5,868.5 | 10 |
| 33 | 383.3 | 8,368.5 | 11 |
| 36 | 136 | 4,222.2 | 12 |
| 39 | 136 | 5,992.1 | 13 |
| 42 | 136 | 8,492.1 | 14 |
| 45 | 48.3 | 4,266.1 | 15 |
| 48 | 48.3 | 6,036 | 16 |
| 51 | 48.3 | 8,536 | 17 |
| 54 | 17.1 | 4,281.7 | 18 |
| 57 | 17.1 | 6,051.6 | 19 |
| 60 | 17.1 | 8,551.6 | 20 |

Table 2. Internal attenuator resistor values.

## Accommodating High Signal Levels

One key objective of the 5173 design was to accommodate full professional-audio signal levels. Accordingly, it is fabricated in a high-voltage CMOS process which allows operation from up to ±17V analog power supplies. Along with proprietary (and patent-pending) drive circuitry to the switching FETs, this permits low-distortion operation at signal levels up to over +27dBu in, and +27dBu out. See also DN140 for more discussion and ideas.

## Switching Noise

The 5173 includes several features which minimize switching noise during gain changes. Special (patent pending) circuitry slows down the FET gate drive to minimize charge injection. This helps suppress clicks when changing gain. As well, the FET switches are implemented in a balanced fashion so as to maintain equal perturbation to the positive and negative sides of the balanced signal path.

A built-in zero-crossing detector can be used to restrict gain changes to times when the analog signal is very close to zero. The detector monitors the differential signal present between the $IN_1$ and $IN_2$ pins

of the 5173. When enabled, it permits gain changes to take place only when the signal is within ±12.5mV. A timeout (set by external components $R_T$ and $C_T$ in Figures 8~11) ensures that a gain change will always occur at the expiration of the timeout, in case the signal has not gotten within the voltage window by that time.

The period of a 20Hz waveform is 50ms and thus zero-crossings will occur every 25ms. Accordingly, THAT recommends that the timeout be set to less than or equal to 25ms in order to ensure that gain changes will be made at zero-crossings unless there is some unusual low-frequency signal present. 22mS is the time constant shown in the application schematics. Of course, for special applications, the designer may choose to disable the zero-crossing detection and force immediate gain changes without regard to the signal condition.

With the zero-crossing feature enabled, gain changes are very quiet – barely audible when performed in the absence of program, and all but inaudible with program material present.

## Servo and DC Offsets

The 5173 also includes an integrated differential servo amplifier which minimizes dc offset at the output. Practically, it is impossible to ensure that the input offset voltage of the analog gain stage is low enough to maintain low output dc offset at high gains. (For <10mV output offset, the input offset at ~60dB gain would have to be under 10μV!) On the other hand, it is not too difficult to make amplifiers with under 1.75mV input offset. By using such an amplifier in feedback around the analog gain stage, it is possible to generate a correction voltage that maintains low output offset from the circuit as a whole.

The integrated differential servo amplifier has under 1.75mV input offset voltage. It requires two large non-polar capacitors in feedback around each half of the amp to form an integrator. The integrator's input is connected to the gain stage's output, and the integrator's output is applied to the gain stage's input. As the loop settles, the gain stage's output will be driven to the input offset voltage of the servo. The loop time constant must be set long enough so as not to interfere with low audio-frequency signals.

The combination of the input coupling capacitors ($C_4$ and $C_5$ in Figures 8~11), the bias resistors ($R_1$ and $R_2$ – which form a load for $C_4$ and $C_5$), and the servo, form a 2nd order highpass filter whose characteristics change with the gain setting. The Q of this filter is highest at the highest gain setting. (At low gains, the behavior is governed almost entirely by the input coupling network and bias resistors, since the poles split and the one related to the servo moves very low.) Assuming 1.2kΩ for $R_1$ and $R_2$, and 1.2MΩ for $R_7$ and $R_8$, we can set the highest Q to be about .77 (for approximately Butterworth response) if we choose $C_{12}$ and $C_{13}$ to be 1/10 the values of $C_4$ and $C_5$.

We recommend a 1000:1 ratio between servo feed resistors ($R_7$ and $R_8$) to the analog gain stage bias resistors ($R_1$ and $R_2$) to minimize any noise contribution from the servo amp. Reducing $R_7$ and $R_8$ will lower the Q, while increasing them will raise the Q, proportional to the square-root of resistance.

Mathematically, we can express the cutoff frequency, $f_o$, and the Q as:

$$f_o = \frac{1}{2\pi\sqrt{\frac{1}{G}\,R_7\,20\text{k}\Omega\,C_4 C_{13}}}, \text{ and}$$

$$Q = \frac{1}{2\pi f_0 \frac{1}{G} 20\text{k}\Omega\,C_{13}\,K}, \text{ where G is the}$$

preamp gain, $K=1+(R_7/R_1)$, $R_1=R_2$, $R_7=R_8$, $C_4=C_5$, $C_{12}=C_{13}$, and the source impedance is less than 1kΩ.

While the servo is effective at minimizing dc offset at the outputs, it does require time to react. When gain is changed, particularly if a sudden large increase in gain is initiated (e.g. 0dB to 60dB), the servo output will not change instantaneously with the gain change. Immediately after the gain increase, the servo will be supplying a dc offset appropriate for the lower gain, and the dc at the output will thus change, on a transient basis, to a higher level. As the servo acquires the new required value, the dc offset will be driven down to under 1.75mV.

To minimize the sonic impact of the dc offset change, THAT recommends that gain be increased slowly by sending many commands to the 5173 that increase gain 3dB (one step) at a time, over a second or more of total time. This replaces the one big change in dc offset with a series of much smaller ones, allowing the servo some time to settle (at least partially) in between each step. Note that the problem is much less audible during stepwise decreases in gain, since the servo's output is not amplified as much at the new (lower) gain as it was at the previous one.

## SPI Control Interface

The 5173 provides a daisy chainable serial-peripheral interface (SPI) port for digital control of its internal parameters. The SPI port may be clocked at speeds up to 10MHz, and thus a 16-bit data word can be clocked into the chip in less than 2 us.

The SPI port consists of four signals: Chip Select (CS), Data In (DIN), Data Out (DOUT), and Serial Clock (SCLK). Figure 4 shows a single 5173 device connected to the SPI port of a typical host microcontroller. A command sequence is initiated when CS makes high to low transition. Data is clocked into DIN on rising edges of SCLK, through an internal 16-bit shift register which holds the 5173 configuration, and then out the DOUT pin on falling edges of SCLK. CS makes a low to high transition at the conclusion of a command sequence. The DOUT pin is tristated while CS is high so that multiple devices can be connected to a single SPI MISO port on a host processor.
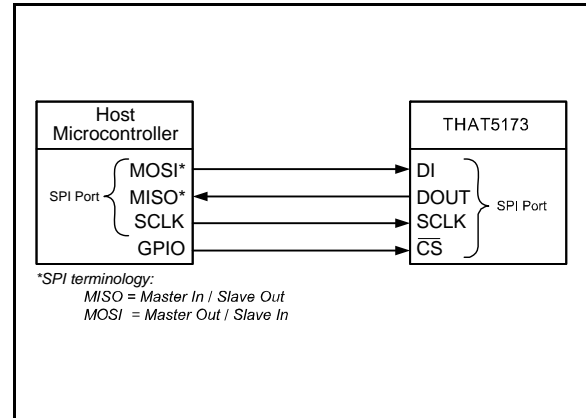


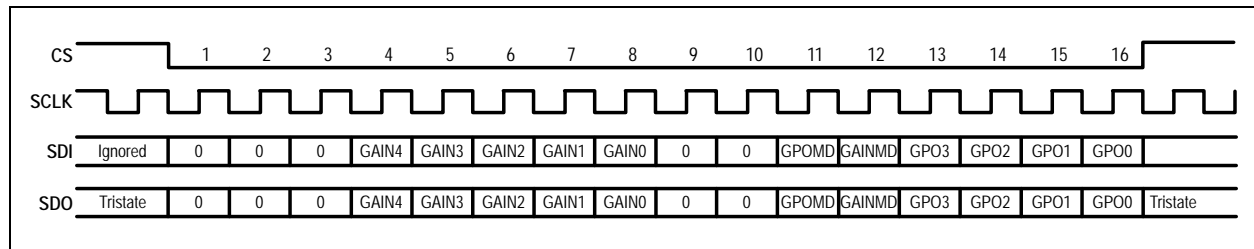Figure 4. Single 5173 connected to a host microcontroller.



Figure 5. SPI Command Format

| Signal | Pin | I/O | Function |
|--------|-----|-----|----------|
| $\overline{\text{CS}}$ | 16 | Input | Device chip select input, active low. An SPI transfer begins with a high-to-low CS transition and ends with a low-to-high CS transition. When CS is high, SCLK transitions are ignored. |
| SCLK | 17 | Input | SPI serial clock input. An SPI master supplies this clock with frequencies up to 10MHz. Data is clocked into the DIN pin on the rising edge of SCLK. Data is clocked out of DOUT pin on the falling edge of SCLK. |
| DIN | 18 | Input | SPI serial data input (Master-Out, Slave-In). |
| DOUT | 19 | Output/Tristate | SPI serial data output (Master-In, Slave-Out). DOUT is tristated when CS is high. |

Table 3. SPI signals.

## Parameters

The 5173 parameters that can be adjusted via SPI are:

### • GAIN (5 bits)

The GAIN[4:0] bits set the gain of the internal resistor ladder. Note that each increment of 1 in the GAIN value results in a 3dB increment in gain. See Table 4 for gain settings.

Reset default = 00000 (0dB)

### • GPO (4 bits)

Each of the GPO[3:0] bits controls the state of the respective GPO port as follows:

0 = GPO[n] "off" (0V)
1 = GPO[n] "on" (3.3V)

Reset default = 0000 (all ports off)

### • Zero Crossing Detector Enables (2 bits)

The zero crossing detector can be independently enabled for gain and GPO changes via the GAINMODE and GPOMODE config bits respectively. Table 5 shows the bit settings for each of the modes.

Reset default = 00 (ZC off)

| GPO MODE | GAIN MODE | | |
|---|---|---|---|
| : | : | | |
| : | 0 | = Immediate GAIN Updates |
| : | 1 | = GAIN updates on ZC |
| : | | | |
| 0 | | = Immediate GPO Updates |
| 1 | | = GPO Updates on ZC |

Table 5. Zero Crossing Detector Enables

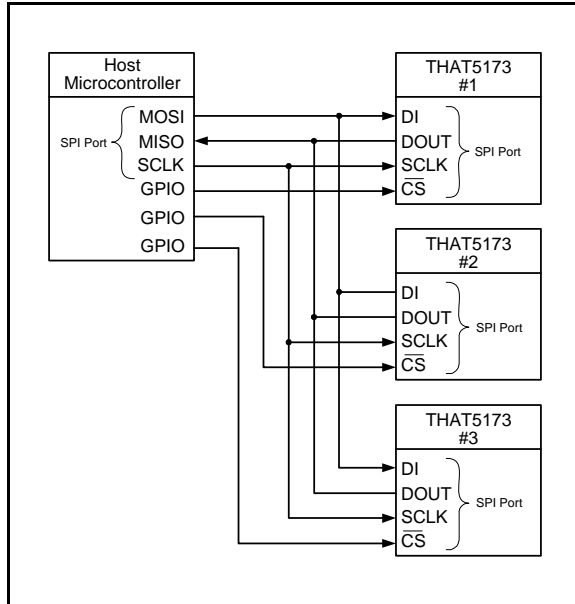| GAIN [4:0] | | | | | Decimal Value | 5173 Gain |
|---|---|---|---|---|---|---|
| G4 | G3 | G2 | G1 | G0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| 0 | 0 | 0 | 1 | 0 | 2 | 6 |
| 0 | 0 | 0 | 1 | 1 | 3 | 9 |
| 0 | 0 | 1 | 0 | 0 | 4 | 12 |
| 0 | 0 | 1 | 0 | 1 | 5 | 15 |
| 0 | 0 | 1 | 1 | 0 | 6 | 18 |
| 0 | 0 | 1 | 1 | 1 | 7 | 21 |
| 0 | 1 | 0 | 0 | 0 | 8 | 24 |
| 0 | 1 | 0 | 0 | 1 | 9 | 27 |
| 0 | 1 | 0 | 1 | 0 | 10 | 30 |
| 0 | 1 | 0 | 1 | 1 | 11 | 33 |
| 0 | 1 | 1 | 0 | 0 | 12 | 36 |
| 0 | 1 | 1 | 0 | 1 | 13 | 39 |
| 0 | 1 | 1 | 1 | 0 | 14 | 42 |
| 0 | 1 | 1 | 1 | 1 | 15 | 45 |
| 1 | 0 | 0 | 0 | 0 | 16 | 48 |
| 1 | 0 | 0 | 0 | 1 | 17 | 51 |
| 1 | 0 | 0 | 1 | 0 | 18 | 54 |
| 1 | 0 | 0 | 1 | 1 | 19 | 57 |
| 1 | 0 | 1 | 0 | 0 | 20 | 60 |
| 1 | 0 | 1 | 0 | 1 | 21 | 60 |
| 1 | 0 | 1 | 1 | 0 | 22 | 60 |
| | | : | | | : | : |
| 1 | 1 | 1 | 1 | 1 | 31 | 60 |

Table 4. Gain Settings

Figure 6. Multiple 5173 ICs connected in parallel to a host microcontroller, with independent chip selects.

## Multiple Devices with Separate Chip Selects

The SPI port can be operated with multiple devices by using separate chip selects as shown in Figure 6. The advantage of this method over daisy chaining is that any of the N 5173 devices may be updated with a single 16-bit SPI operation (as opposed to the long Nx16 bit data stream required when N devices are daisy chained). The disadvantage of this method is N different chip selects must be supplied to the individual devices.
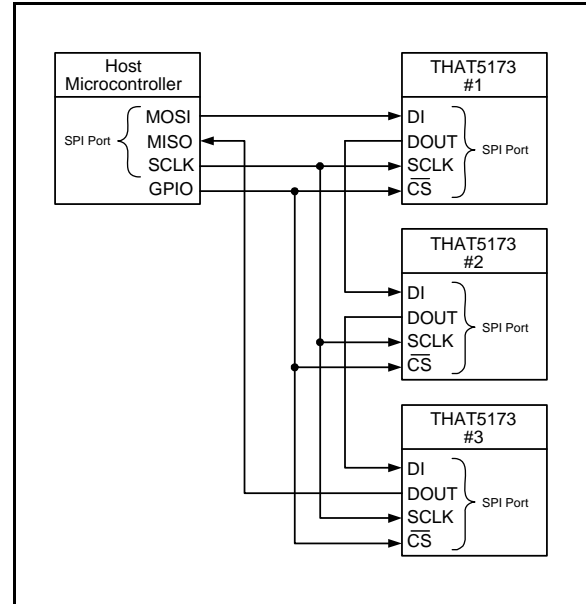


Figure 7. Multiple 5173 ICs connected in a daisy-chained mode to a host microcontroller.

## Daisy Chaining

Multiple devices can be daisy-chained by connecting the DOUT of device n to the DIN pin of device n+1, as shown in Figure 7. Data is loaded by holding the common CS low for 16 x N SCLK pulses, where N = total number of devices in the daisychain. All devices are simultaneously updated on the rising edge of CS, particularly useful in applications where updates to a large number of channels must be synchronized. Another advantage of this method is one chip select can be shared by all devices, simplifying the digital control circuitry on the PCB. The disadvantage is all N devices must be updated as a group, thereby slowing down the rate of control to each individual device.

# Applications

While the 5173 is perfectly suitable for application to virtually any discrete current-feedback differential preamplifier, the applications discussed herein are exclusively based on use with the companion THAT1570 IC. The circuit of Figure 8 shows the most basic application of the 5173 and 1570 to form a complete low-noise digitally-controlled microphone preamplifier.

## Gain Ranges in Basic Configurations

The circuit of Figure 8 offers differential gain that varies from 0 to 60dB in 3dB steps. For single-ended analog outputs, the circuit of Figure 8 can be followed by a differential-to-single-ended converter, as shown in Figure 9.

At minimum gain (0dB) and with ±15V supply rails, the maximum (differential) input signal level is +26.8dBu, and the maximum (differential) output signal level is +26.6dBu. At maximum gain (+60dB), the maximum input signal level is -33dBu, and the maximum output signal level remains +26.6dBu. All these figures increase by a little over 1dB if the circuit is run from ±17V supplies.

When converting to single-ended signals, take care to select a low-noise opamp, and pay attention to the noise generated by the impedances. The component values shown in Figure 9 will largely preserve

the dynamic range of the 1570 and 5173 combination.

For many applications, the output of the microphone preamplifier must drive an analog-to-digital converter. Most high-performance A/D converters have differential inputs, and cannot accept differential signals greater than ~+8dBu. For such applications, the output of the mic preamp must be attenuated to prevent overload of the A/D converter. The circuit of Figure 10 shows one typical circuit, using a simple resistive attenuator ($R_9$ through $R_{11}$). The impedance levels of the attenuator are chosen to minimize their self-generated voltage noise, and to stay within the load limits of the amplifier which drives them. Figure 10 assumes that the maximum differential input to the A/D converter is +8dBu. For higher (or lower) maximum input levels, or for different supply voltages to the 1570 and 5173, scale the attenuator accordingly, keeping its total impedance ($R_9 + R_{10} + R_{11}$) the same. Please note that the noise contribution of the U-pad can compromise the theoretical noise performance of the 1570/5173 combination at minimum gain. Moreover, the non-zero impedance drive to the converter may increase distortion with high-performance converters. The impact of this impedance depends on the ADC.

Note that one drawback of the circuit shown in Figure 10 is that it offers no attenuation of common-signals. The 1570 has unity common-mode gain
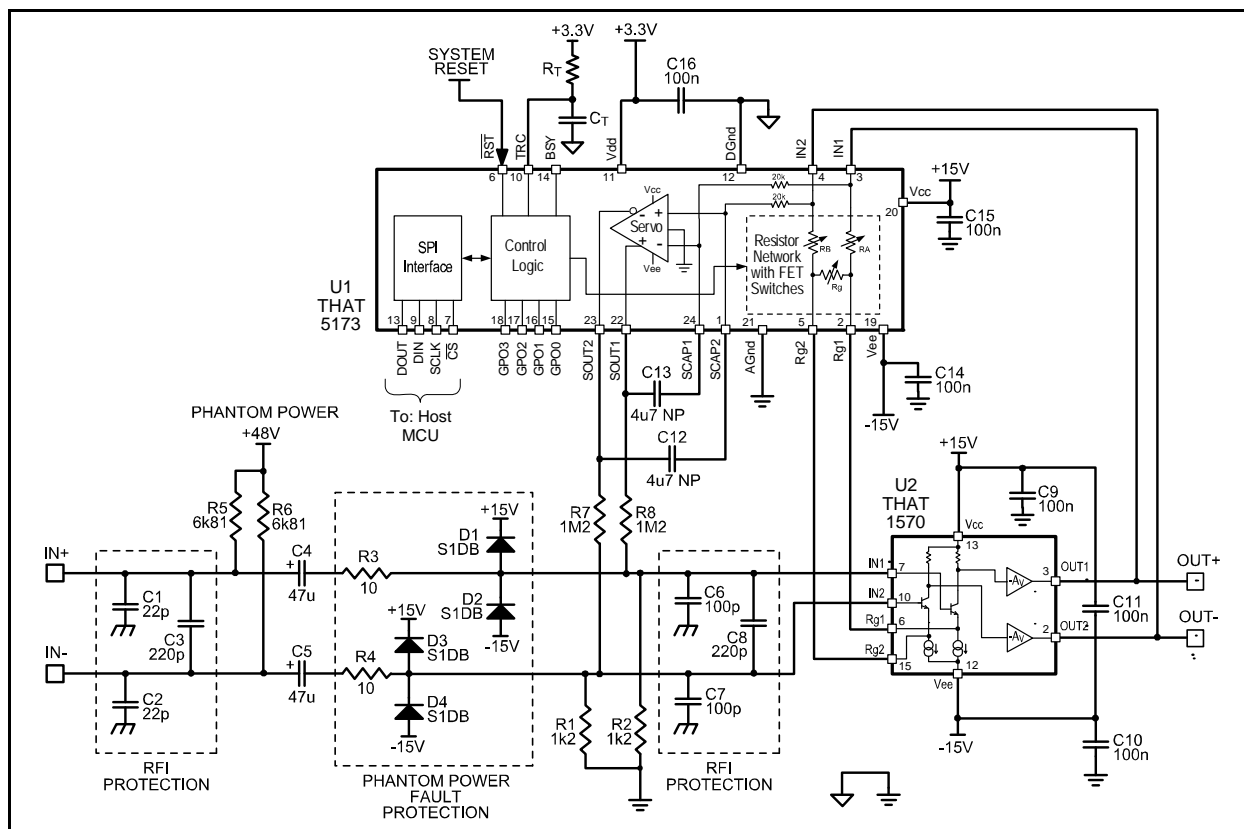


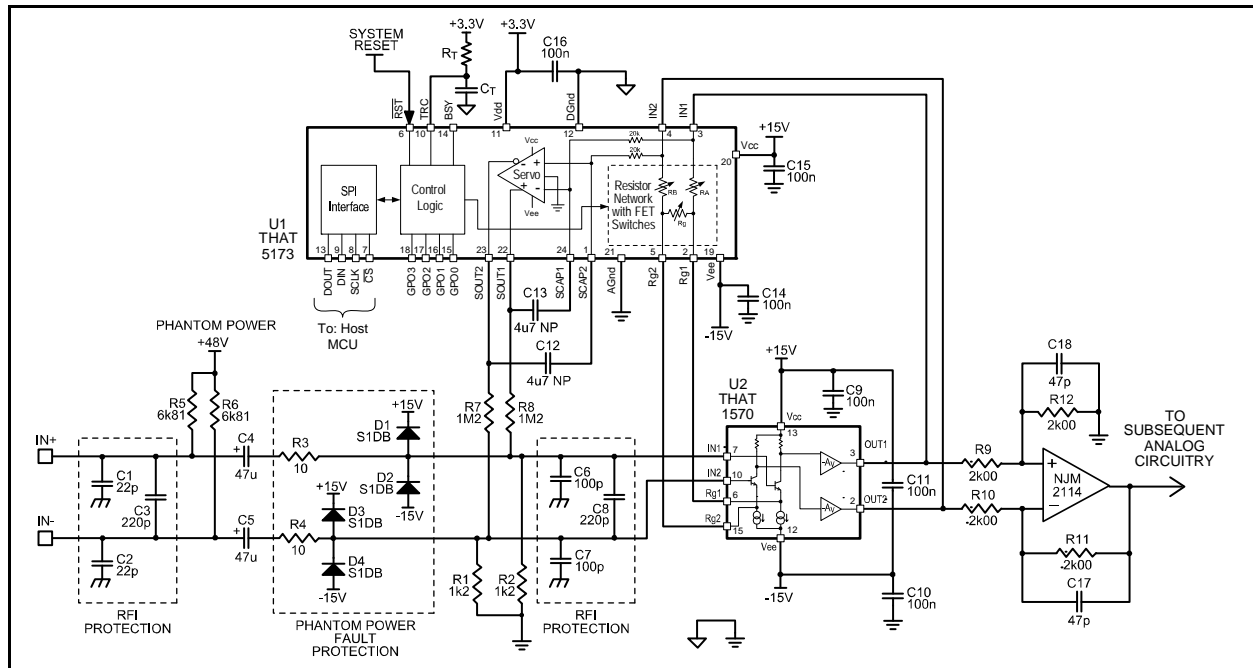Figure 8. 5173 and 1570 basic application circuit.

Figure 9. 5173 and 1570 typical application with single-ended output.

regardless of its differential gain. When set to unity gain, the circuit of Figure 8 has 0 dB CMRR. The U-pad attenuator formed by R9~R11 attenuates differential signals but not common-mode signals, so the CMRR of this circuit is actually -9 dB at minimum gain: when the 5173 is set for 0 dB gain, differential input signals are attenuated by 9 dB, but common-mode signals are passed without any attenuation.

Differential-input A/D converters generally provide high common-mode rejection, so the system CMR including converter may well be acceptable, but consider what happens if a large common-mode signal is present along with a large differential input
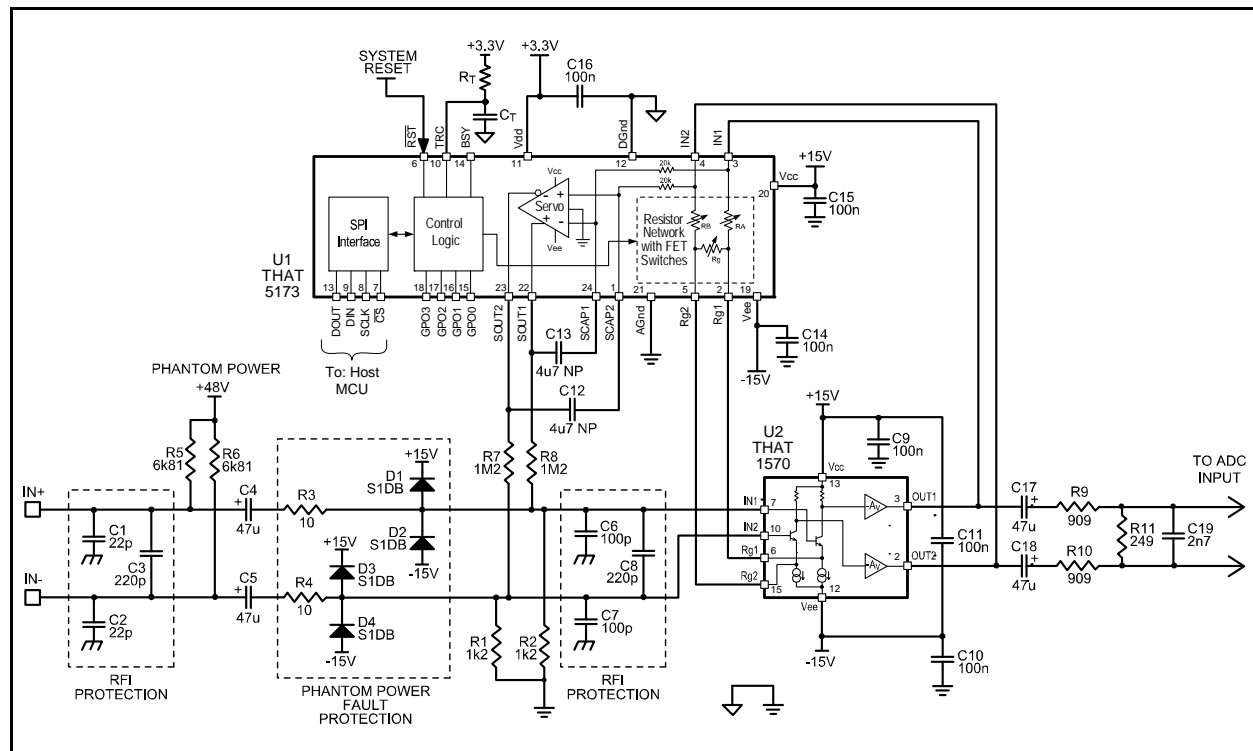


Figure 10. 5173 and 1570 low-cost application for output to an A/D convertor.

signal. (This is most likely the case when using the preamp as a line input.) The output of Figure 10 ("To ADC Input") will see that large common-mode input signal, along with a 9 dB attenuated version of the differential input signal. If sufficiently large, the common-mode signal can cause the converter to clip prematurely, modulating the differential audio with the common-mode signal. While this may only occur in extreme use conditions, it may well be of concern.

In such cases, consider the circuit of Figure 11, which removes the common-mode signal (depending on the matching of resistors R9 & R10, R11 & R13, and R14 & R16) before it reaches the A/D converter input. This circuit also provides a low-impedance drive for the converter, recommended by many converter makers for best distortion performance. The novel configuration (after Brit) minimizes the noise contribution of the second (lower) inverter, since it's noise appears in common mode and not differentially at the output.

Note that in this case, at low gains the CMRR of the system will be determined by the matching of resistors R9~R16, with some contribution at high frequencies from the matching of C17 and C18. At high gains, the CMRR of the output stage will be boosted by the gain of the 1570/5173 circuitry that precedes it.

## RFI Protection (and Common-Mode Rejection)

The circuits of Fig 8 through 11 include RFI protection in two sections. Small capacitors ($C_1$ and $C_2$) are used from the positive and negative signal inputs

to chassis ground, along with a larger capacitor ($C_3$) across the two inputs. These components should be located as close as possible to the input signal connector, and are intended to prevent RF from entering the chassis of the device.

A second RF protection network is located close to the amplifier, and is intended to prevent any RF picked up inside the unit from reaching the amplifier input, where it might be rectified and cause audio-band interference. This network consists of a pair of larger capacitors ($C_6$ and $C_7$) to ground and one more capacitor ($C_8$) across the two input lines. If RF is prevented from entering the unit, and none is generated inside the unit, then these capacitors may be omitted or reduced in value.

The design of these networks was arrived at after some consideration for common-mode rejection. Unbalanced capacitance from either input line (IN+ or IN-) to ground can unbalance common-mode signals, converting them to differential signals, which will be amplified along with the desired (differential) signal. The differential amplifier in the above circuits offers gain only to differential signals: common-mode signal gain is always 0dB. Therefore, its common-mode rejection is equal to the differential gain.

So long as common-mode signals are not converted to differential ones, this common-mode rejection will prevail. Because they are relatively small, differences in the values of $C_1$ and $C_2$ are less likely to cause imbalance than the larger capacitors at $C_6$ and $C_7$. For this reason, we recommend that capacitors $C_6$ and $C_7$ should be at least 5% types, in order to ensure matching between their values. Note that $C_3$
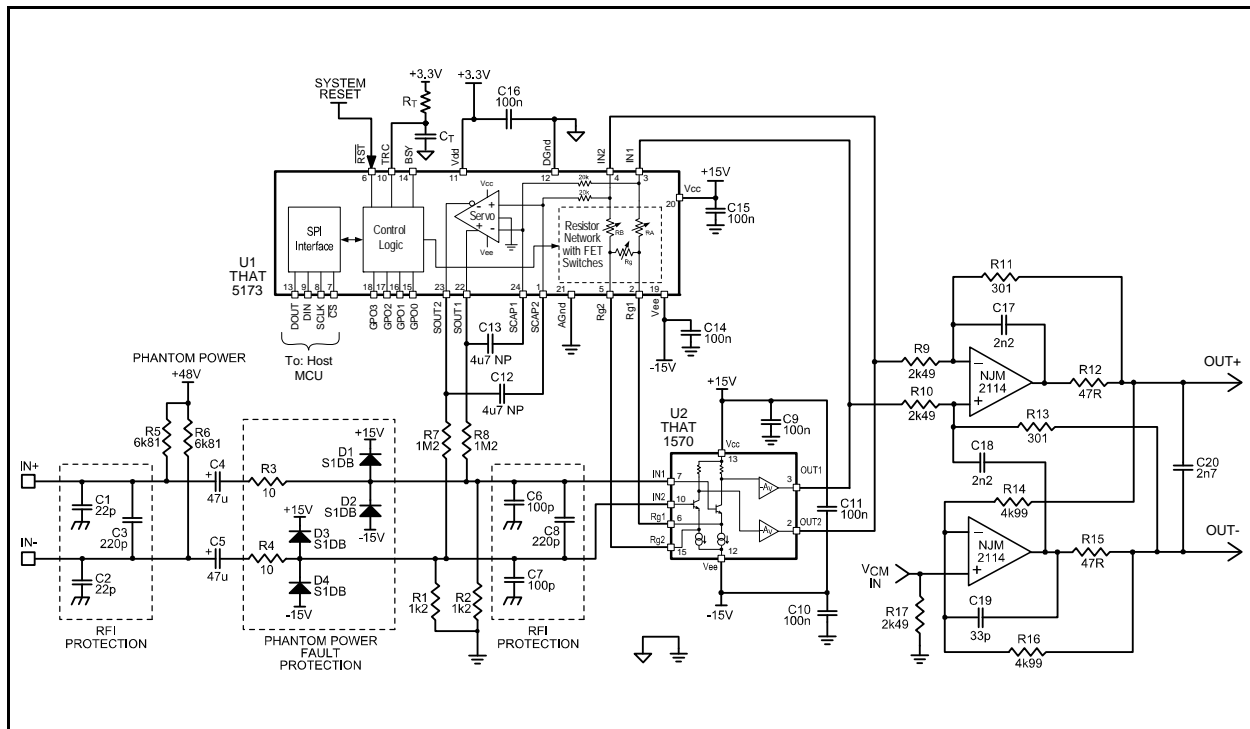


Figure 11. 5173 and 1570 high-performance application for output to an A/D convertor.

and $C_8$ affect only differential signals, and thus do not affect common-mode rejection.

## Power Supply Decoupling

Power supply decoupling is required for stability of the 1570, the servo in the 5173, and to minimize digital switching noise from propagating on the power supplies. The $V_{CC}$ and $V_{EE}$ pins should be connected to the same analog supply which powers the analog gain stage, while the $V_{DD}$ pin may be powered in common with other logic circuitry (microprocessors, etc.) in the unit.

THAT recommends one decoupling capacitor ($C_{16}$) for the digital power supply, placed close to pins 12 ($D_{GND}$) and 11 ($V_{DD}$), as these pins connect to the digital output driver bus.

$A_{GND}$ and $D_{GND}$ should be connected together directly under the 5173. Note that the part includes back-to-back diodes limiting the maximum voltage difference between these nodes. If even on a transient basis (e.g., supply spikes) a voltage difference of over 0.5 V exists between $A_{GND}$ and $D_{GND}$, large currents will flow which may damage the part.

Care should be taken to ensure that the power supply voltages never exceed the absolute maximum ratings even under transient conditions.

As described above (in the Theory section), the integrated differential servo is required for proper operation of the system as shown in the application schematics. By using the servo amplifier in feedback, output offset can be controlled over a wide range of gains.

In order to optimize settling behavior, THAT recommends that $C_{12}$ and $C_{13}$ be approximately one-half the size of $C_4$ and $C_5$. As well, to avoid the servo from contributing noise to the preamplifier, we recommend that the servo's output be divided down by approximately 1000:1 by the combination of $R_7/R_1$ and $R_8/R_2$.

## Reset (RST pin)

Asserting the RST pin low forces all internal registers to their default state (see Parameter definitions register definitions in SPI Port section for default values after reset). This pin is typically connected to system reset or to a port on the host microcontroller.

## Zero Crossing Detector  (and TRC pin)

The integrated zero-crossing detector may be enabled or disabled for the GAIN and GPO parameters independently (see Table 5). When enabled, it prevents gain and/or GPO changes from occurring until the differential output signal waveform is within ±12.5 mV of zero.

When the GAINMODE or GPOMODE bits are logic low (Table 5), Gain and GPO updates are made immediately following a rising edge on the /CS pin. When GAINMODE and GPOMODE are logic high, updates are made on the next output signal zero-crossing after a rising edge on the /CS pin.

When no signal is present, the zero-crossing detector may unacceptably delay a gain or GPO change from taking place. A timeout, set by $R_T$ and $C_T$, is provided to force a change to occur within $R_T C_T$mS if a zero crossing is not detected. The zero-crossing time-out function operates as follows:

A) $C_T$ is discharged when /CS goes low (the beginning of an SPI command sequence), and is allowed to start charging when /CS goes high (the end of an SPI command sequence).

B) Gain and/or GPOs are updated on the next zero-crossing or when the voltage on the TRC pin charges to $0.7*V_{DD}$ -- whichever event occurs first.

The recommended time constant for $R_T C_T$ is ~22mS (e.g. $C_T$ = 1nF and $R_T$ = 22MΩ ).

The choice between "immediate" vs "zero crossing" mode depends on the application. Immediate mode has the advantage of providing gain updates with short deterministic latency, whereas zero crossing mode has the advantage of minimizing glitches and zipper noise.

## Busy (BSY pin)

The BSY pin is asserted high when a gain update or GPO update is pending a zero-crossing. This pin may be monitored by the host microcontroller (e.g. connected to an external interrupt pin) in order to hold off a new gain command until the previous gain command has been executed.

If finer gain steps (e.g. 1dB) are implemented in external processing (typically a DSP) the BUSY signal can be employed to synchronize the external gain changes with those implemented by the 5173 (most importantly, when the interpolated gain "wraps" from maximum to minimum as each 5173 3dB step occurs). Note that latency in A/D conversion must be considered when attempting to synchronize digital with analog gain updates.
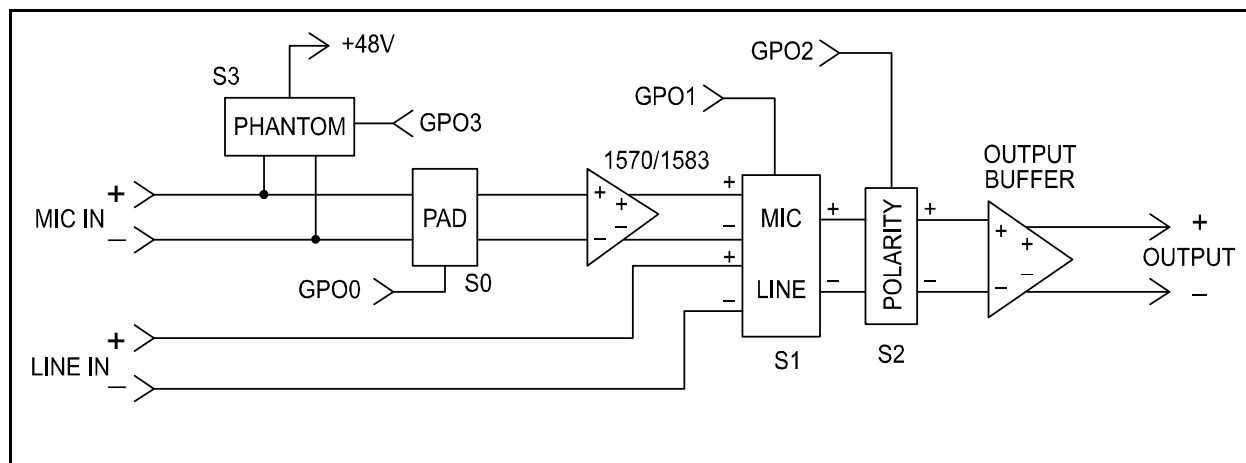
Figure 12. GPO outputs control preamp functions.

## Using the GPOs to Control Preamplifier Functions

While the General Purpose Outputs (GPOs) can be used to control any binary state functions, they are primarily intended to control analog functions associated with a preamplifier. Figure 12 is a block diagram showing THAT 5173 GPO outputs controlling typical preamp functions such as an input pad (GPO0), mic/line switching (GPO1), signal polarity (GPO2), and phantom power (GPO3). There are many ways to control each of these functions, each with its own tradeoffs. See Design Note 140 ("Input and Output Circuits for THAT Preamplifier ICs") for basic circuit ideas using relays.

# PCB Layout Information

The 5173 and 1570 are intended to lay out side-by-side, with pins 1 through 4 on the 1570 facing pins 1 through 6 on the 5173. See Figure 13 for a suggested layout.

Designers should take care to minimize capacitance on the Rg pins, and to ensure that power supply lines do not run close and/or parallel to either the input signal lines or the traces and pins connected to the Rg pins. For current feedback amplifiers such as the 1570, stray capacitance from the Rg pins (inverting input) to ground or power planes results in higher gains at high frequencies. As a result, mismatches in the capacitance on these two nodes will degrade common-mode performance at high frequencies.

Additionally, power supply lines, which often carry non-linear (e.g., half-wave rectified) versions of the signal can magnetically and capacitively couple



Figure 13. Recommended THAT1570/THAT5173 PCB Layout (mounted on same-side of PCB).

into the input and Rg lines. This can create distortion, particularly at high gains.

Therefore, THAT recommends avoiding ground plane under the $IN_1$ and $IN_2$ pins and associated traces. We also recomend a symmetrical PCB layout to match the capacitance on these nodes.

As is customary with QFN packages, we recommend that the metal "slug" on the bottom of the QFN package be soldered to provide physical attachment and improve thermal performance. It may be left unconnected electrically, or connected to $V_{EE}$.

When laying out the board, we recommend following advice offered by Henry W. Ott in his recent book Electromagnetic Compatibility Engineering, published in August 2009 by Wiley (ISBN: 978-0-470-18930-6). In it, Mr. Ott recommends laying out the digital and analog ground scheme using ground planes as if they were separate planes, but do not actually separate them in the final design. As noted earlier, all bypass capacitors should be located very close to their respective power and ground pins. In particular, for the digital supplies, C16 should connect close to pins 11 and 12.

A useful reference for PCB layout is the demonstration circuit board for the 5173/1570, available from THAT. While the board itself is of course useful to designers, the layout and schematic are published in the data sheet which covers the board, and is available for downloading from THAT's web site.
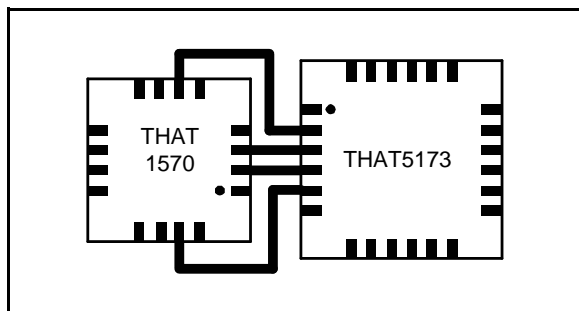
## Package and Soldering Information

| Package Characteristics | | | | |
|---|---|---|---|---|
| Parameter | Symbol | Conditions | | Units |
| Package Style | | See Fig. 14 for dimensions | 24 Pin QFN | |
| Thermal Resistance | $\theta_{JA}$ | QFN package soldered to board, Thermal pad not soldered to board | 70 | ºC/W |
| Environmental Regulation Compliance | | Complies with January 27, 2003 RoHS requirements | | |
| Soldering Reflow Profile | | JEDEC JESD22-A113-D (250 ºC) | | |
| Moisture Sensitivity Level | MSL | Above-referenced JEDEC soldering profile | 3 | |

The THAT 5173 is available in a 5mm x 5mm 24-pin QFN package. The package dimensions are shown in Figure 14. Pinouts are given in Table 1.

The 5173 is lead free and RoHS compliant. Material Declaration Data Sheets on the parts are available at our web site, www.thatcorp.com or upon request. For ordering information, see Table 6.
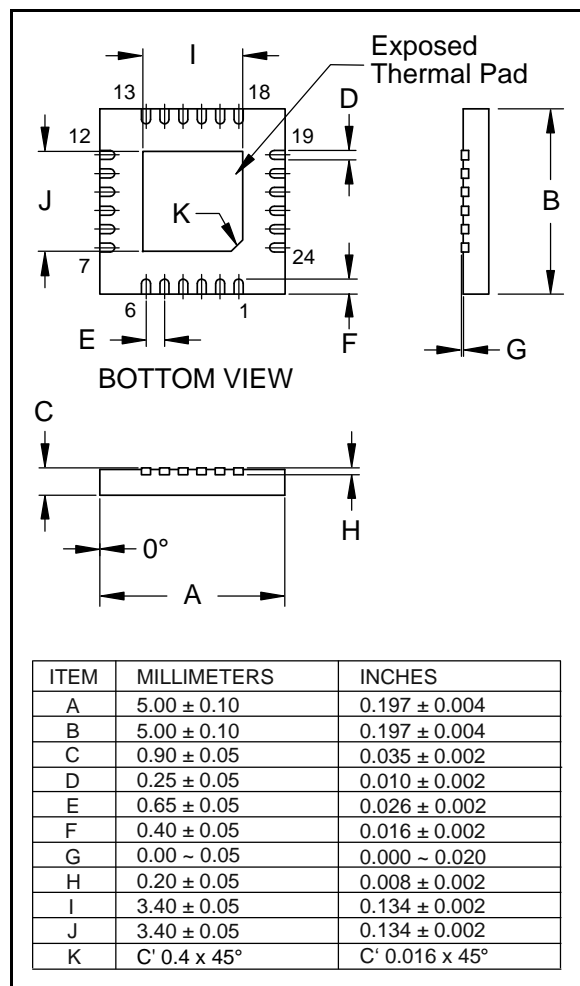
| Package | Order Number |
|---|---|
| 24 pin QFN | 5173N24-U |

Table 6. Ordering Information.



| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 5.00 ± 0.10 | 0.197 ± 0.004 |
| B | 5.00 ± 0.10 | 0.197 ± 0.004 |
| C | 0.90 ± 0.05 | 0.035 ± 0.002 |
| D | 0.25 ± 0.05 | 0.010 ± 0.002 |
| E | 0.65 ± 0.05 | 0.026 ± 0.002 |
| F | 0.40 ± 0.05 | 0.016 ± 0.002 |
| G | 0.00 ~ 0.05 | 0.000 ~ 0.020 |
| H | 0.20 ± 0.05 | 0.008 ± 0.002 |
| I | 3.40 ± 0.05 | 0.134 ± 0.002 |
| J | 3.40 ± 0.05 | 0.134 ± 0.002 |
| K | C' 0.4 x 45° | C' 0.016 x 45° |

Figure 14. 5 x 5mm QFN-24 Package Dimensions.

## Revision History

| Revision | ECO | Date | Changes | Page |
|:---:|:---:|:---:|:---|:---:|
| 00 | — | March 2012 | Release to production | — |
| 01 | 2737 | Nov 2012 | Correct typographical errors | 4, 16 |
| 02 | 2873 | May 2014 | Optimized capacitor values in application figures | — |
| 03 | 2883 | July 2014 | Corrected error in text regarding value of C12 & C13 | 7 |
|  |  |  |  |  |
|  |  |  |  |  |

# Notes

# **Notes**