

Z0109NA

4Q Triac

Rev. 05 — 21 March 2011

Product data sheet

1. Product profile

1.1 General description

Planar passivated sensitive gate four quadrant triac in a SOT54 (TO-92) plastic package intended for use in applications requiring direct interfacing to logic ICs and low power gate drivers.

1.2 Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate in four quadrants
- Triggering in all four quadrants

1.3 Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{J}(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; see Figure 4 ; see Figure 5	-	-	8	A
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{lead}} \leq 45\text{ }^{\circ}\text{C}$; see Figure 3 ; see Figure 1 ; see Figure 2	-	-	1	A

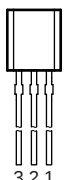
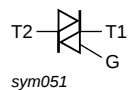


Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+G+; $T_j = 25\text{ }^\circ\text{C}$; see Figure 7	-	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+G-; $T_j = 25\text{ }^\circ\text{C}$; see Figure 7	-	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2-G-; $T_j = 25\text{ }^\circ\text{C}$; see Figure 7	-	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2-G+; $T_j = 25\text{ }^\circ\text{C}$; see Figure 7	-	-	10	mA

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2		 <i>sym051</i>
2	G	gate		
3	T1	main terminal 1		
SOT54 (TO-92)				

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
Z0109NA	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{lead}} \leq 45^\circ\text{C}$; see Figure 3 ; see Figure 1 ; see Figure 2	-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{J(init)}} = 25^\circ\text{C}$; $t_p = 20\text{ ms}$; see Figure 4 ; see Figure 5	-	8	A
		full sine wave; $T_{\text{J(init)}} = 25^\circ\text{C}$; $t_p = 16.7\text{ ms}$	-	8.5	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	0.32	A^2s
di_{T}/dt	rate of rise of on-state current	$I_{\text{T}} = 1\text{ A}$; $I_{\text{G}} = 20\text{ mA}$; $di_{\text{G}}/dt = 0.1\text{ A}/\mu\text{s}$; T2+ G+	-	50	$\text{A}/\mu\text{s}$
		$I_{\text{T}} = 1\text{ A}$; $I_{\text{G}} = 20\text{ mA}$; $di_{\text{G}}/dt = 0.1\text{ A}/\mu\text{s}$; T2+ G-	-	50	$\text{A}/\mu\text{s}$
		$I_{\text{T}} = 1\text{ A}$; $I_{\text{G}} = 20\text{ mA}$; $di_{\text{G}}/dt = 0.1\text{ A}/\mu\text{s}$; T2- G-	-	50	$\text{A}/\mu\text{s}$
		$I_{\text{T}} = 1\text{ A}$; $I_{\text{G}} = 20\text{ mA}$; $di_{\text{G}}/dt = 0.1\text{ A}/\mu\text{s}$; T2- G+	-	20	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	1	A
P_{GM}	peak gate power		-	2	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	$^\circ\text{C}$
T_{J}	junction temperature		-	125	$^\circ\text{C}$

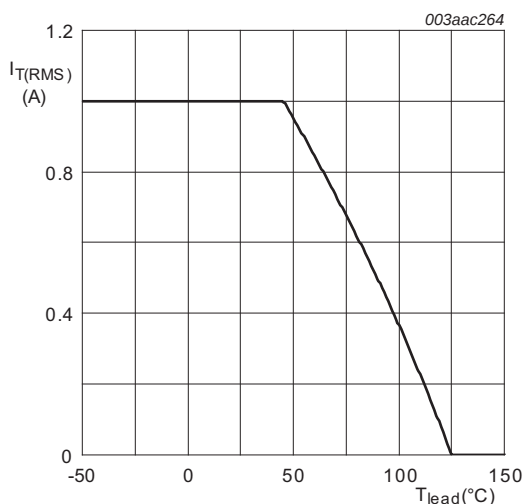
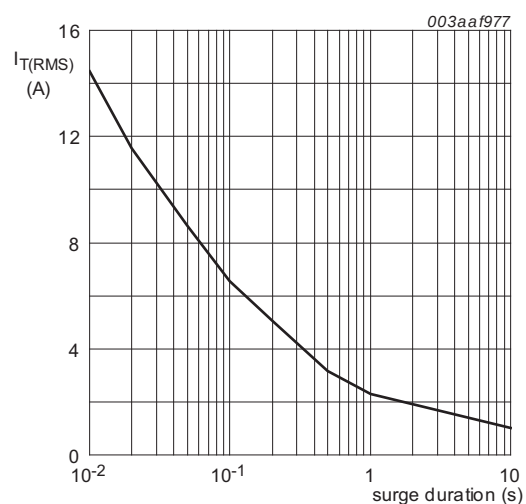
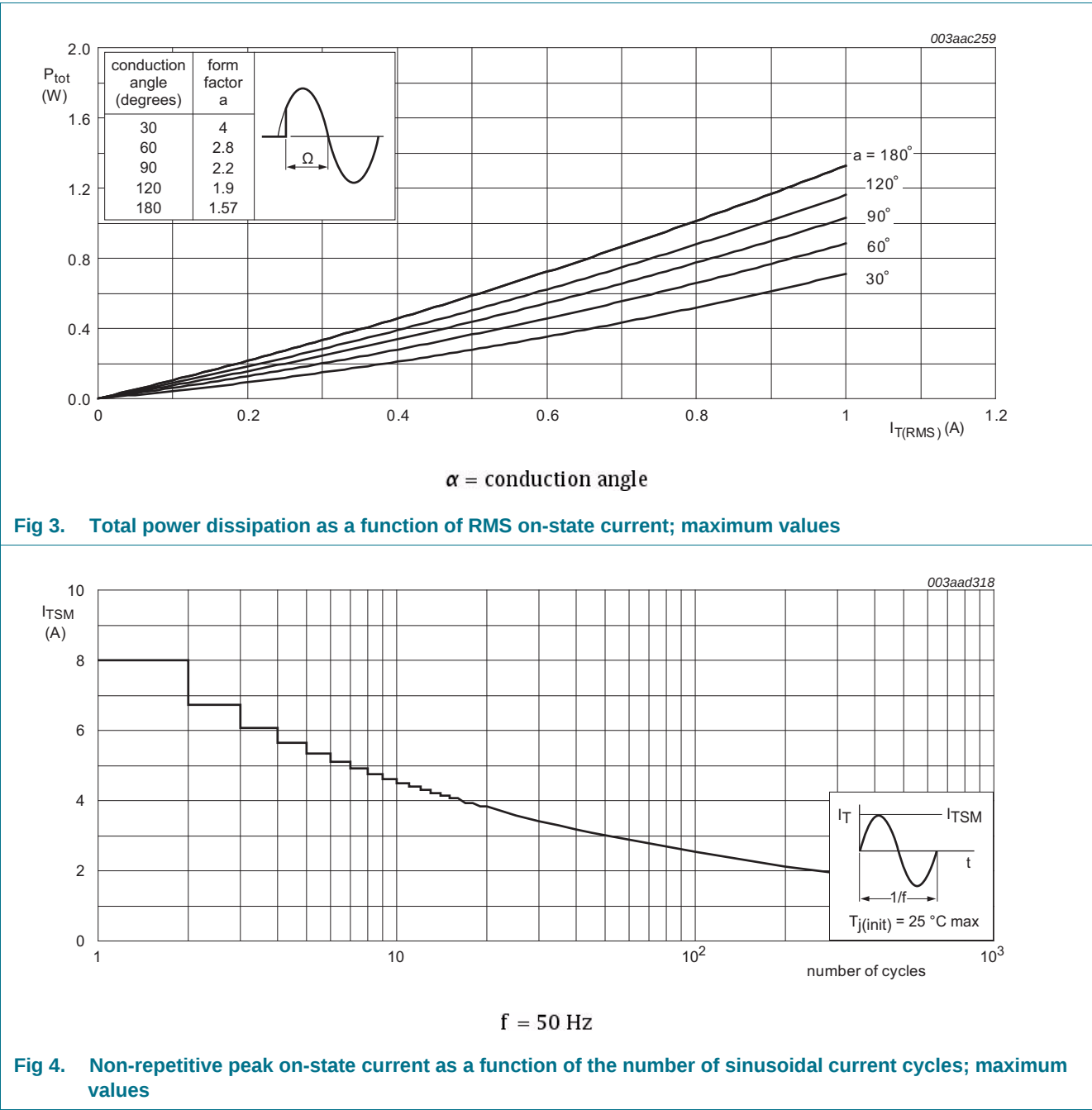


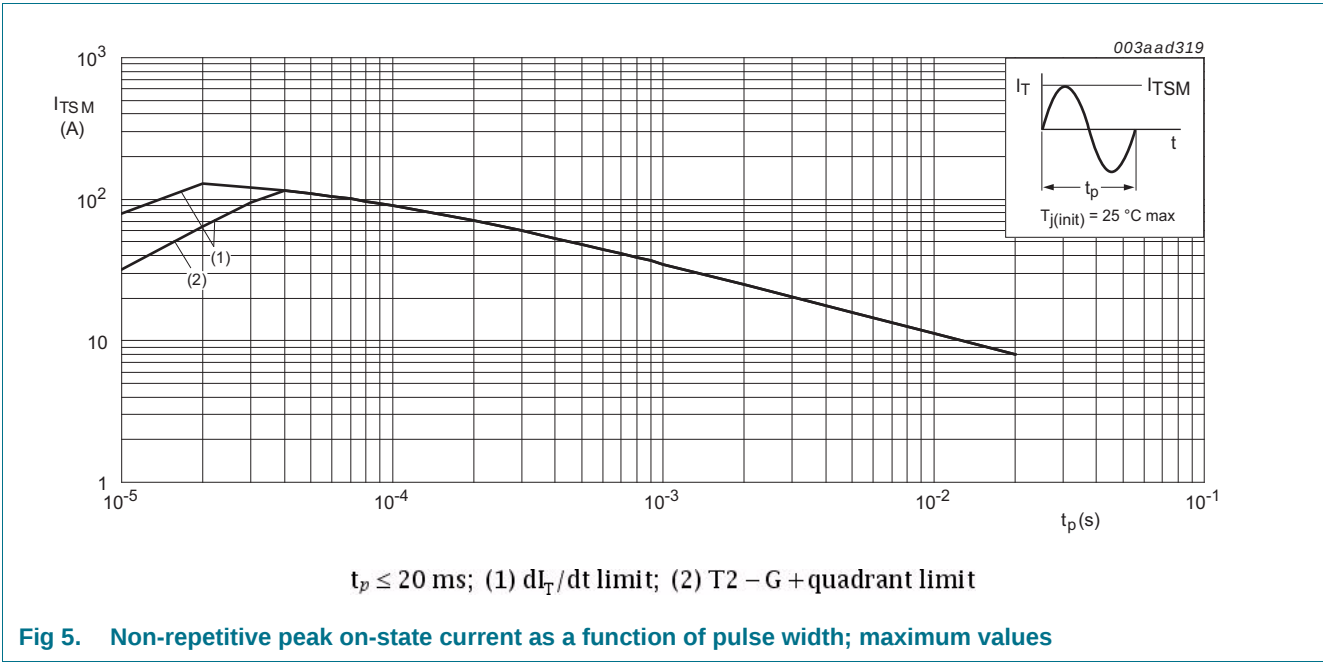
Fig 1. RMS on-state current as a function of lead temperature; maximum values



$$f = 50\text{ Hz}, T_{\text{lead}} = 45^\circ\text{C}$$

Fig 2. RMS on-state current as a function of surge duration; maximum values

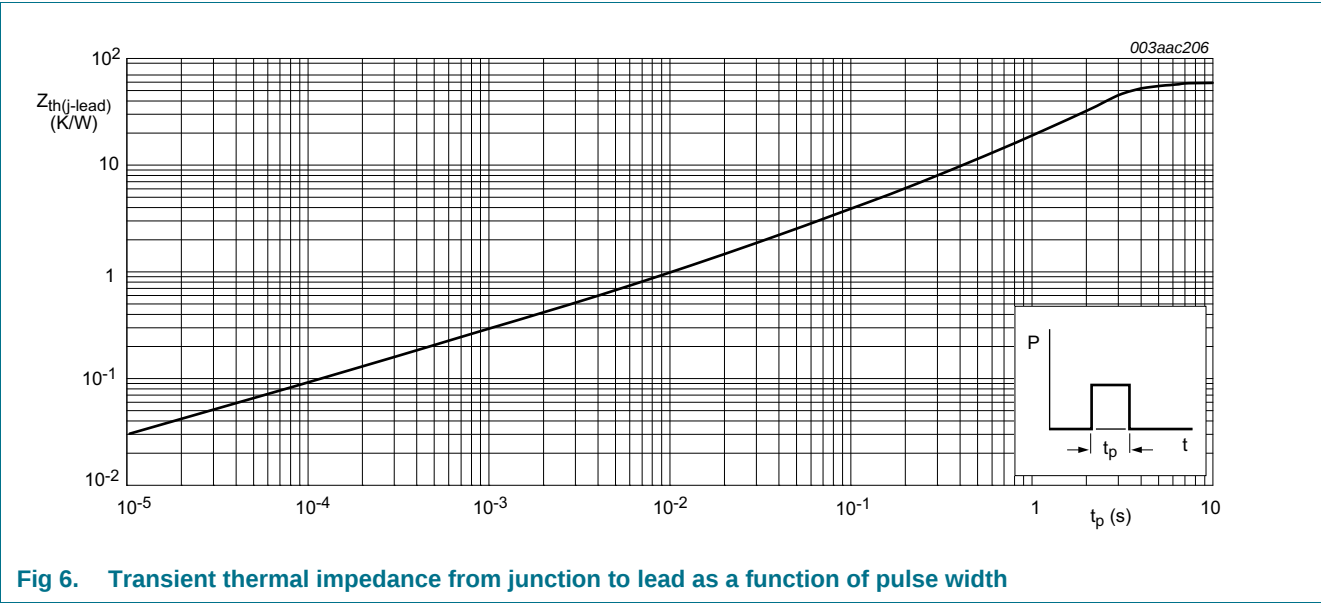




5. Thermal characteristics

Table 5. Thermal characteristics

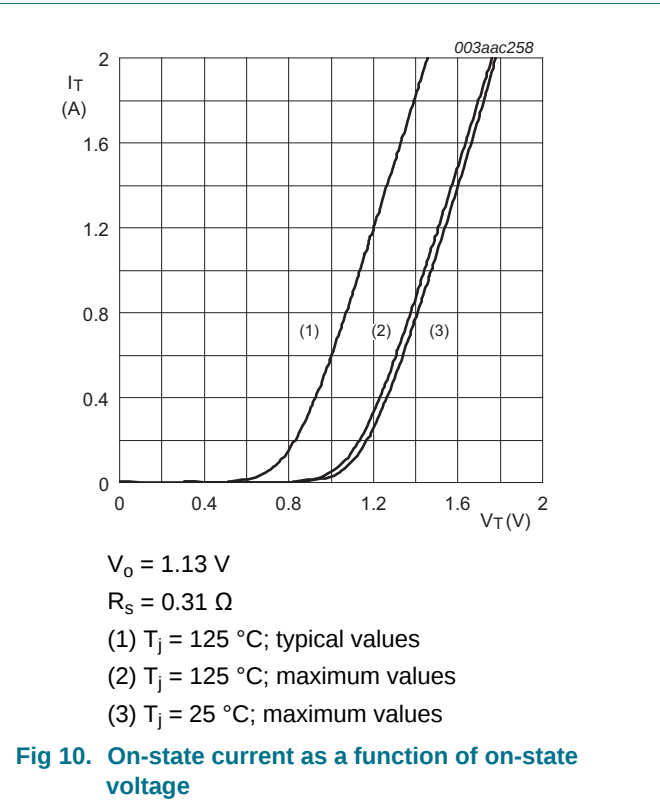
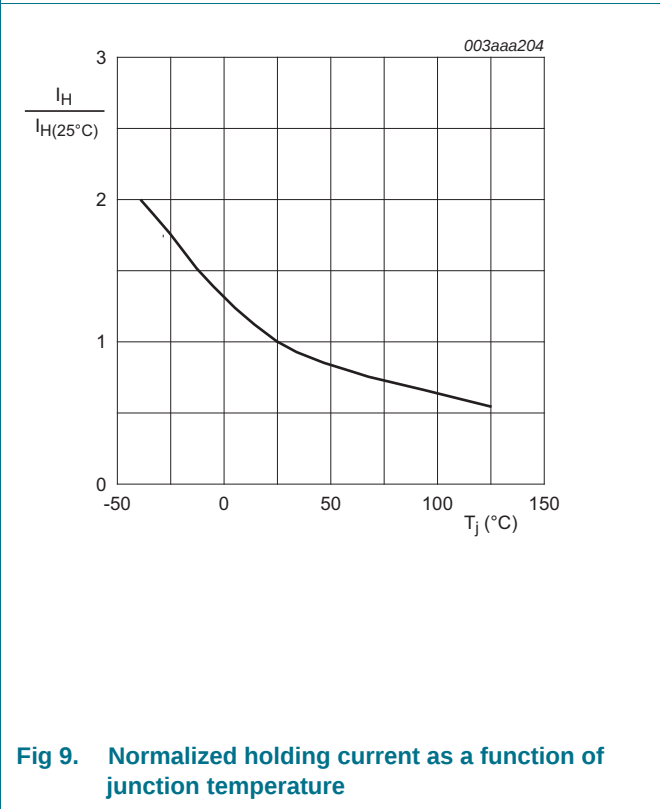
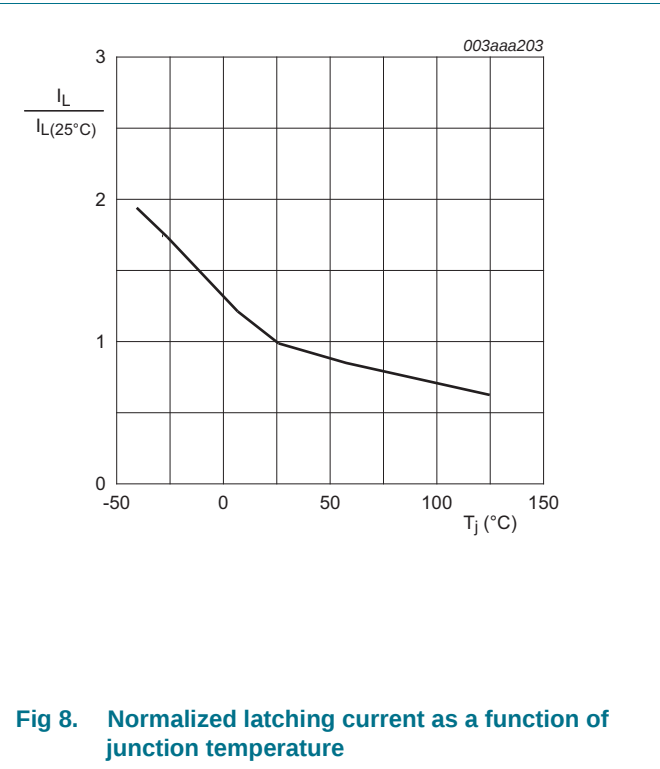
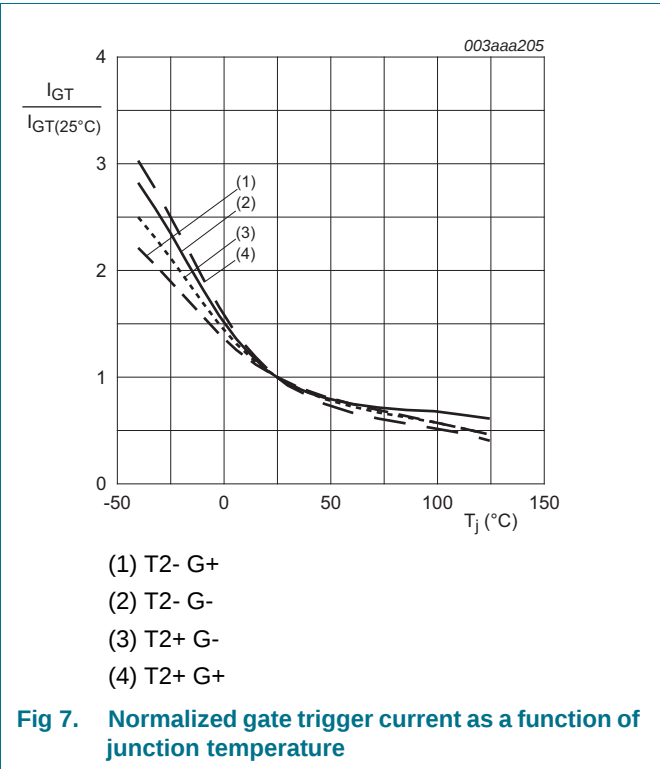
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle; see Figure 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	full cycle; printed circuit board mounted; lead length = 4 mm	-	150	-	K/W

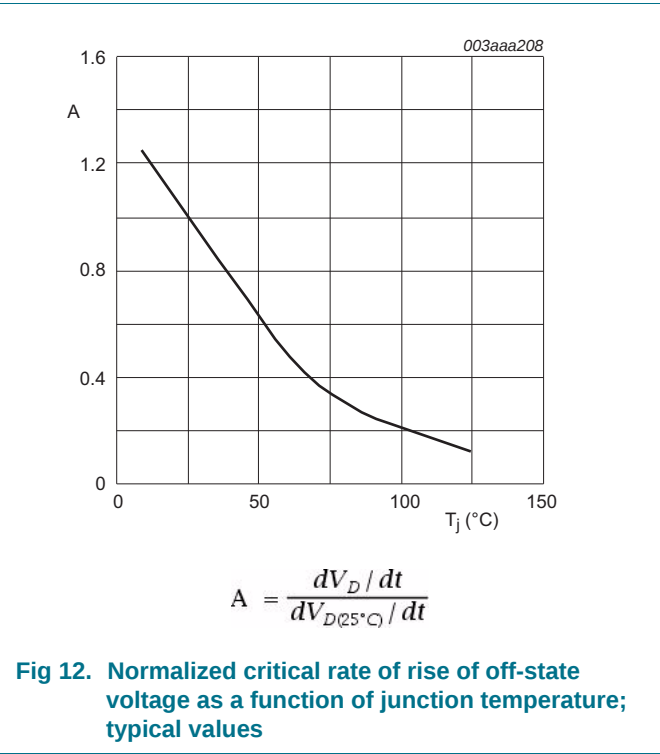
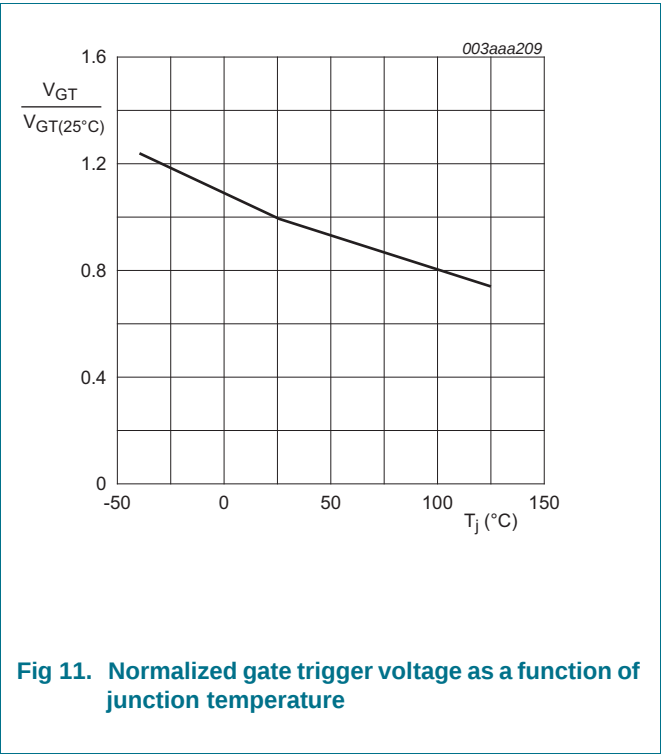


6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; see Figure 7	-	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; see Figure 7	-	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; see Figure 7	-	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; see Figure 7	-	-	10	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; see Figure 8	-	-	15	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; see Figure 8	-	-	25	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; see Figure 8	-	-	15	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; see Figure 8	-	-	15	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 9	-	-	10	mA
V_T	on-state voltage	$I_T = 1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 10	-	1.3	1.6	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 11	-	-	1.3	V
		$V_D = 800\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; see Figure 11	0.2	-	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$	-	-	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 110\text{ }^\circ\text{C}$; exponential waveform; gate open circuit; see Figure 12	50	-	-	V/ μs
dV_{com}/dt	rate of change of commutating voltage	$V_D = 400\text{ V}$; $T_j = 110\text{ }^\circ\text{C}$; $dI_{com}/dt = 0.44\text{ A/ms}$; $I_T = 1\text{ A}$; gate open circuit	2	-	-	V/ μs





7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

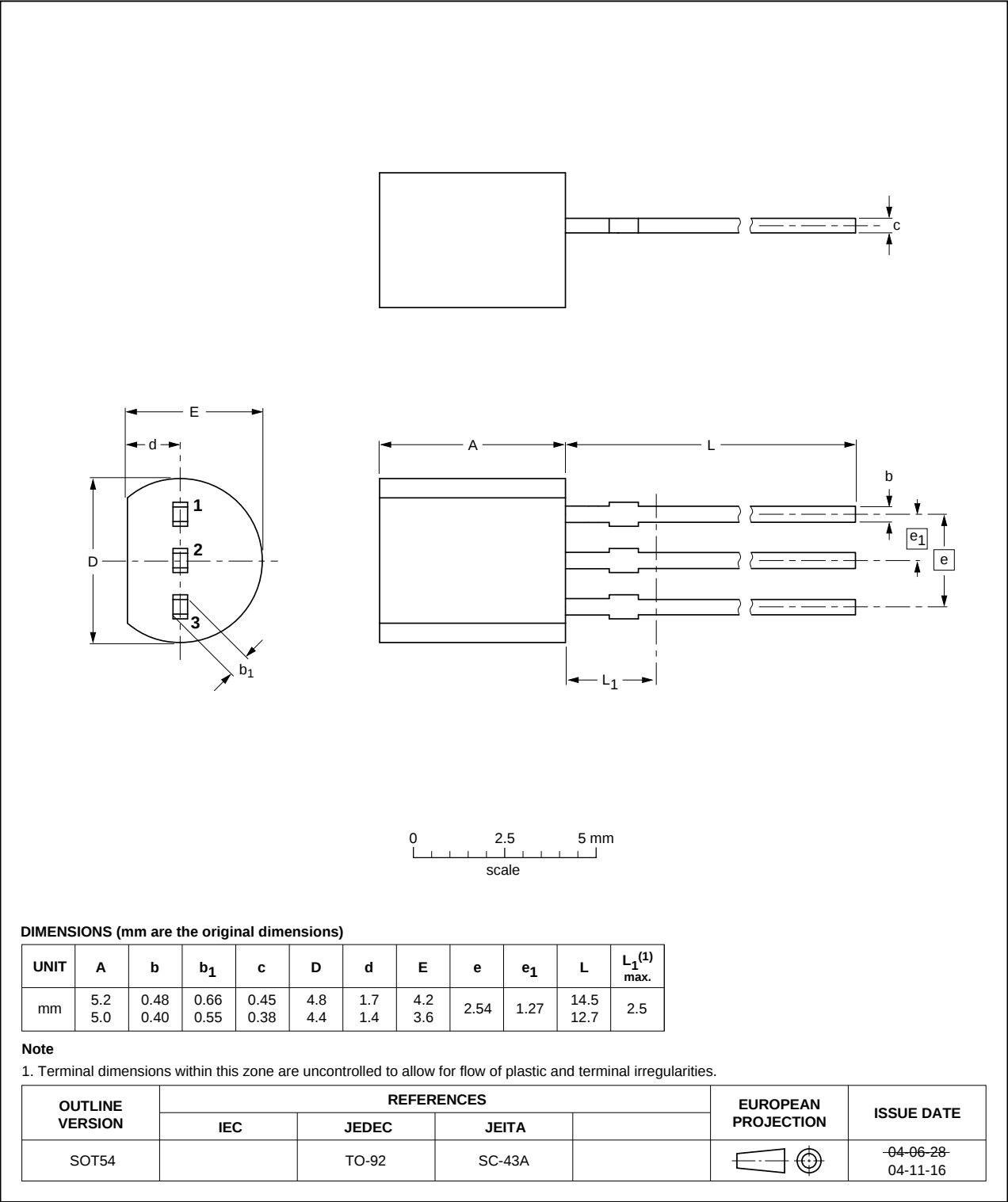


Fig 13. Package outline SOT54 (TO-92)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
Z0109NA v.5	20110321	Product data sheet	-	Z0109NA v.4
Modifications:	• Various changes to content.			
Z0109NA v.4	20090804	Product data sheet	-	Z0109NA v.3

9. Legal information

9.1 Data sheet status

Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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