

# 74ALVCH16374

2.5 V/3.3 V 16-bit edge-triggered D-type flip-flop; 3-state

Rev. 5 — 9 July 2012

Product data sheet

## 1. General description

---

The 74ALVCH16374 is 16-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications.

Incorporates bus hold data inputs which eliminate the need for external pull-up or pull-down resistors to hold unused inputs.

The 74ALVCH16374 consists of 2 sections of eight edge-triggered flip-flops. A clock (CP) input and an output enable ( $\overline{OE}$ ) are provided per 8-bit section.

The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When  $\overline{OE}$  is LOW, the contents of the flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go the high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## 2. Features and benefits

---

- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standard JESD8-B
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold
- Output drive capability 50  $\Omega$  transmission lines at 85 °C
- Current drive  $\pm 24$  mA at  $V_{CC} = 3.0$  V



3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74ALVCH16374DL	−40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVCH16374DGG	−40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram

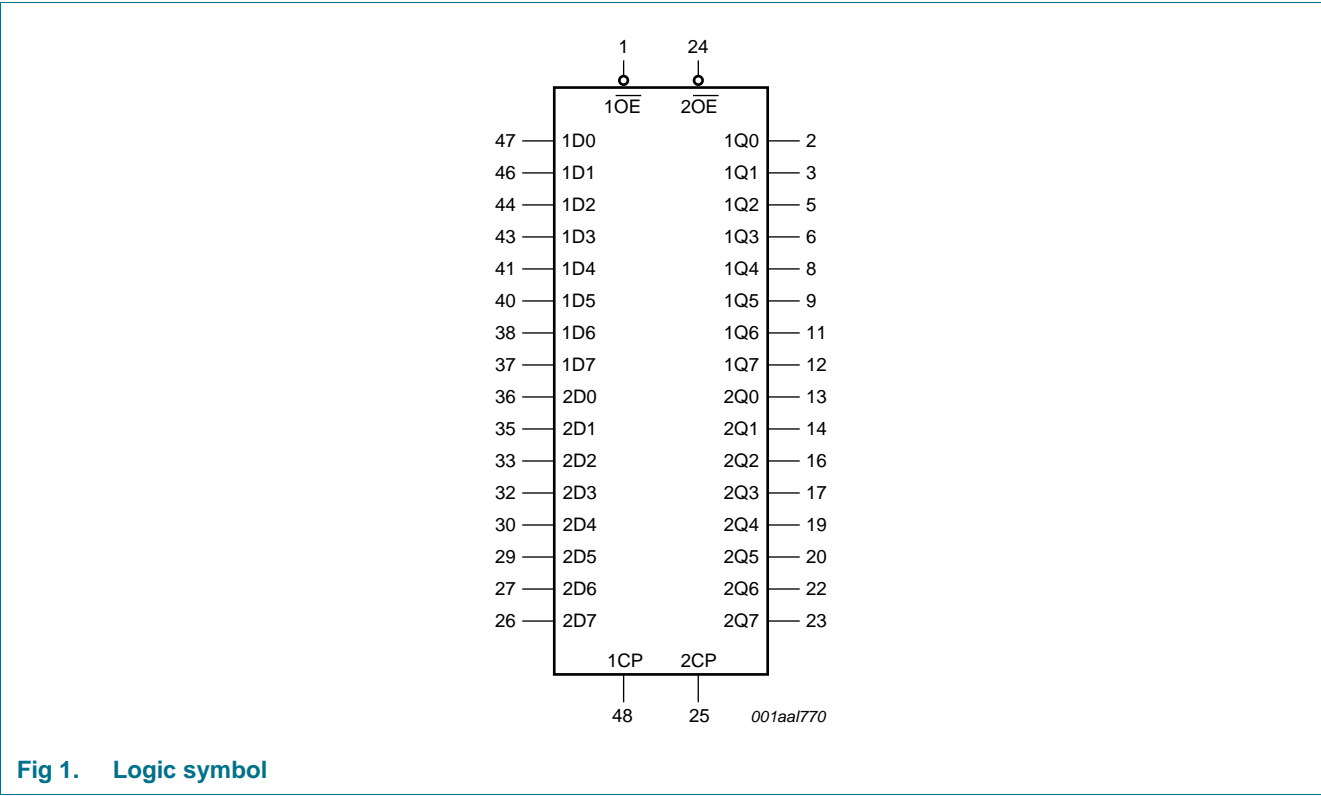


Fig 1. Logic symbol



**Fig 2. IEC logic symbol**



### Fig 3. Bus hold circuit



**Fig 4. Logic diagram**

5. Pinning information

5.1 Pinning

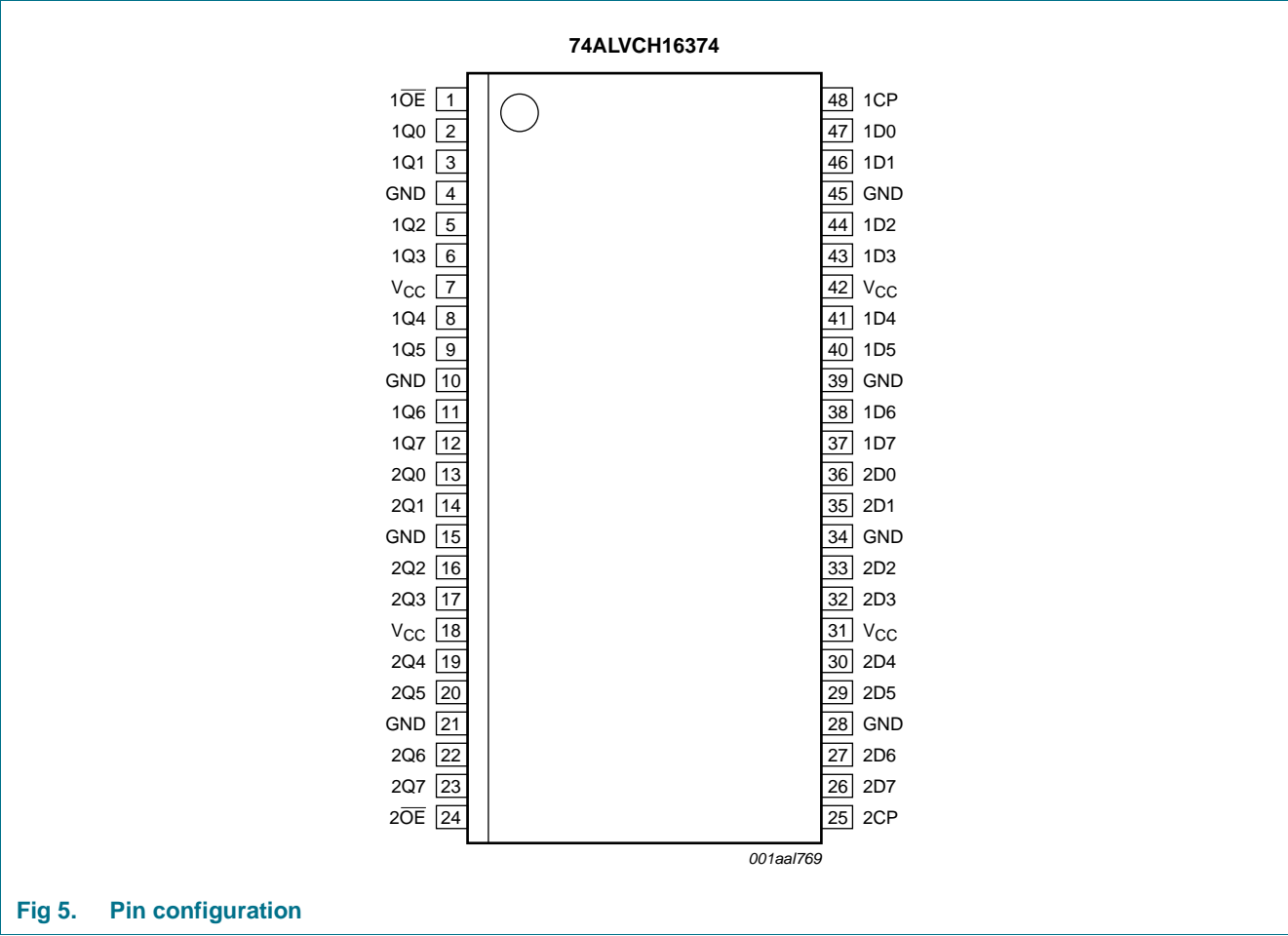


Fig 5. Pin configuration

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{1OE}, \overline{2OE}$	1, 24	output enable input (active LOW)
1Q0 to 1Q7	2, 3, 5, 6, 8, 9, 11, 12	3-state flip-flop outputs
2Q0 to 2Q7	13, 14, 16, 17, 19, 20, 22, 23	3-state flip-flop outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	positive supply voltage
1D0 to 1D7	47, 46, 44, 43, 41, 40, 38, 37	data inputs
2D0 to 2D7	36, 35, 33, 32, 30, 29, 27, 26	data inputs
1CP, 2CP	48, 25	clock input

## 6. Functional description

### 6.1 Function table

Table 3. Function table<sup>[1]</sup>

Inputs			Internal flip-flops	Outputs Q0 to Q7	Operating mode
$\overline{nOE}$	$\overline{nCP}$	Dn			
L	↑	l	L	L	load and read register
L	↑	h	H	H	
H	↑	l	L	Z	load register and disable outputs
H	↑	h	H	Z	

[1] H = HIGH voltage level;

L = LOW voltage level;

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

↑ = LOW-to-HIGH clock transition;

Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage	control inputs	[1] -0.5	+4.6	V
		data inputs	[1] -0.5	$V_{CC} + 0.5$	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$V_O$	output voltage		[1] -0.5	$V_{CC} + 0.5$	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C;			
		SSOP48 package	[2] -	850	mW
		TSSOP48 package	[3] -	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 55 °C the value of  $P_{tot}$  derates linearly with 11.3 mW/K.

[3] Above 55 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage	maximum speed performance				
		$C_L = 30$ pF	2.3	-	2.7	V
		$C_L = 50$ pF	3.0	-	3.6	V
		low voltage applications	1.2	-	3.6	V
$V_I$	input voltage	data inputs	0	-	$V_{CC}$	V
		control inputs	0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 3.0 V	0	-	20	ns/V
		$V_{CC} = 3.0$ V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 1.8 V	0.7V <sub>CC</sub>	0.9	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	1.2	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	1.5	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0	V
		V <sub>CC</sub> = 1.8 V	-	0.9	0.2V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	1.2	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	1.5	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 1.8 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> - 0.4	V <sub>CC</sub> - 0.1	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.17	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 1.0	V <sub>CC</sub> - 0.28	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 1.8 V to 3.6 V	-	0	0.20	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 1.8 V	-	0.09	0.30	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 2.3 V	-	0.07	0.20	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.3 V	-	0.15	0.40	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	0.14	0.40	V
		I <sub>O</sub> = 18 mA; V <sub>CC</sub> = 2.3 V	-	0.23	0.60	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	0.27	0.55	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 1.8 V to 3.6 V				
		control input; V <sub>I</sub> = 5.5 V or GND	-	0.1	5	µA
		data input; V <sub>I</sub> = V <sub>CC</sub> or GND	-	0.1	5	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND				
		V <sub>CC</sub> = 1.8 V to 2.7 V	-	0.1	5	µA
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	0.1	10	µA
I <sub>LIZ</sub>	OFF-state input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND				
		V <sub>CC</sub> = 1.8 V to 2.7 V	-	0.1	10	µA
		V <sub>CC</sub> = 3.6 V	-	0.1	15	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A;				
		V <sub>CC</sub> = 1.8 V to 2.7 V	-	0.1	20	µA
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	0.2	40	µA

**Table 6.** Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$\Delta I_{CC}$	additional supply current	$V_I = V_{CC} - 0.6\text{ V}$ ; $I_O = 0\text{ A}$ ; $V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$				
		per control input	-	5	500	$\mu\text{A}$
		per data I/O input	-	150	750	$\mu\text{A}$
$I_{BHL}$	bus hold LOW current	$V_{CC} = 2.3\text{ V}$ ; $V_I = 0.7\text{ V}$	[2]	45	-	$\mu\text{A}$
		$V_{CC} = 3.0\text{ V}$ ; $V_I = 0.8\text{ V}$	[2]	75	150	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	$V_{CC} = 2.3\text{ V}$ ; $V_I = 1.7\text{ V}$	[2]	-45	-	$\mu\text{A}$
		$V_{CC} = 3.0\text{ V}$ ; $V_I = 2.0\text{ V}$	[2]	-75	-175	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	$V_{CC} = 2.7\text{ V}$	[2]	300	-	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$	[2]	450	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	$V_{CC} = 2.7\text{ V}$	[2]	-300	-	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$	[2]	-450	-	$\mu\text{A}$
$C_I$	input capacitance		-	5.0	-	pF

[1] All typical values are measured at  $T_{amb} = 25\text{ }^\circ\text{C}$ .

[2] Valid for data inputs of bus hold parts only.

## 10. Dynamic characteristics

**Table 7.** Dynamic characteristicsAt recommended operating conditions. Voltages are referenced to GND (ground = 0 V); test circuit [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$T_{amb} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$						
$f_{max}$	maximum frequency	see <a href="#">Figure 6</a>				
		$V_{CC} = 1.8\text{ V}$		125	250	MHz
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	[2]	150	300	MHz
		$V_{CC} = 2.7\text{ V}$		150	300	MHz
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	[3]	200	350	MHz
$t_{pd}$	propagation delay	nCP to nQn; see <a href="#">Figure 6</a>	[4]			
		$V_{CC} = 1.2\text{ V}$		-	7.7	ns
		$V_{CC} = 1.8\text{ V}$		1.5	3.6	6.5 ns
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	[2]	1.0	2.3	4.3 ns
		$V_{CC} = 2.7\text{ V}$		1.0	2.3	3.8 ns
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	[3]	1.0	2.4	3.4 ns
$t_{en}$	enable time	nOE to nQn; see <a href="#">Figure 7</a>	[4]			
		$V_{CC} = 1.2\text{ V}$		-	8.7	ns
		$V_{CC} = 1.8\text{ V}$		1.5	4.0	7.2 ns
		$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$	[2]	1.0	2.6	4.8 ns
		$V_{CC} = 2.7\text{ V}$		1.0	2.9	4.8 ns
		$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$	[3]	1.0	2.3	4.0 ns



**Table 7. Dynamic characteristics ...continued**At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); test circuit [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nQn; see <a href="#">Figure 7</a>	<sup>[4]</sup>			
		V <sub>CC</sub> = 1.2 V	-	6.2	-	ns
		V <sub>CC</sub> = 1.8 V	1.5	3.1	5.4	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	<sup>[2]</sup> 1.0	2.1	4.0	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.9	4.5	ns
t <sub>w</sub>	pulse width	V <sub>CC</sub> = 3.0 V to 3.6 V	<sup>[3]</sup> 1.0	2.6	4.1	ns
		nCP HIGH or LOW; see <a href="#">Figure 6</a>				
		V <sub>CC</sub> = 1.8 V	4.0	2.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	<sup>[2]</sup> 3.0	1.6	-	ns
		V <sub>CC</sub> = 2.7 V	3.0	1.6	-	ns
t <sub>su</sub>	set-up time	V <sub>CC</sub> = 3.0 V to 3.6 V	<sup>[3]</sup> 2.5	1.4	-	ns
		Dn to nCP; see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 1.8 V	1.5	0.2	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	<sup>[2]</sup> 1.2	0.2	-	ns
		V <sub>CC</sub> = 2.7 V	1.5	0.4	-	ns
t <sub>h</sub>	hold time	V <sub>CC</sub> = 3.0 V to 3.6 V	<sup>[3]</sup> 1.2	0.2	-	ns
		Dn to nCP; see <a href="#">Figure 8</a>				
		V <sub>CC</sub> = 1.8 V	0.6	-0.2	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	<sup>[2]</sup> 0.8	-0.1	-	ns
		V <sub>CC</sub> = 2.7 V	0.6	-0.2	-	ns
C <sub>PD</sub>	power dissipation capacitance	V <sub>CC</sub> = 3.0 V to 3.6 V	<sup>[3]</sup> 0.8	0.0	-	ns
		per flip-flop; V <sub>I</sub> = GND to V <sub>CC</sub>	<sup>[5]</sup>			
		outputs enabled	-	16	-	pF
		outputs disabled	-	10	-	pF

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.[2] Typical values are measured at V<sub>CC</sub> = 2.5 V.[3] Typical values are measured at V<sub>CC</sub> = 3.3 V.

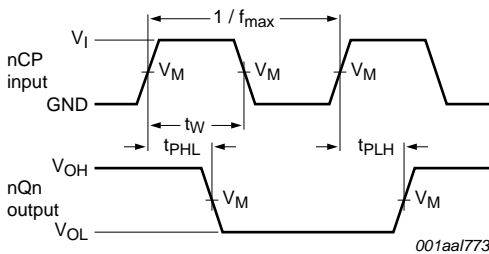
[4] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz;C<sub>L</sub> = output load capacitance in pF;V<sub>CC</sub> = supply voltage in Volts;

N = number of inputs switching;

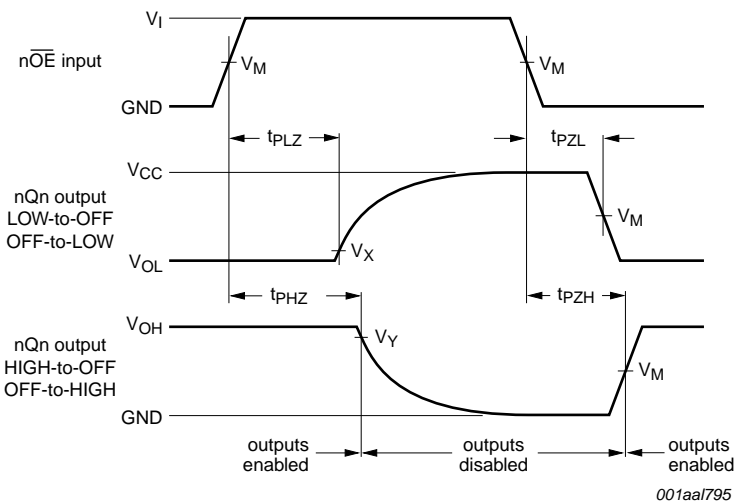
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

11. Waveforms



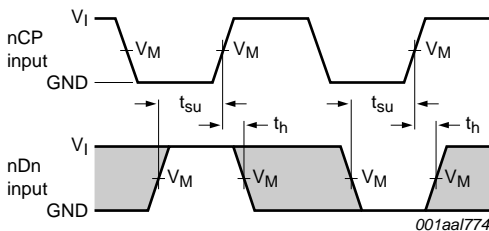
Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output levels that occur with the output load.

Fig 6. Propagation delay, clock input (nCP) to data output (nQn), and pulse width



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output levels that occur with the output load.

Fig 7. 3-state enable and disable times



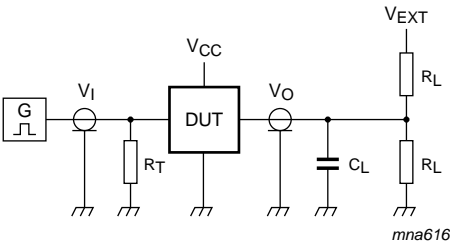
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 8. Data setup and hold times for input (nDn) to input (nCP)

Table 8. Measurement points

Supply voltage	Input		Output		
V <sub>CC</sub>	V <sub>I</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
2.3 V to 2.7 V and < 2.3 V	V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> − 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> − 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> − 0.3 V

12. Test information



Test data is given in [Table 9](#).  
Definitions for test circuit:  
RL = Load resistance.  
CL = Load capacitance including jig and probe capacitance.  
RT = Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator.  
V<sub>EXT</sub> = External voltage for measuring switching times.

Fig 9. Load circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V <sub>EXT</sub>		
V <sub>CC</sub>	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>
2.3 V to 2.7 V and < 2.3 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	500 Ω	open	2 × V <sub>CC</sub>	GND
2.7 V	2.7 V	2.5 ns	50 pF	500 Ω	open	2 × V <sub>CC</sub>	GND
3.0 V to 3.6 V	2.7 V	2.5 ns	50 pF	500 Ω	open	2 × V <sub>CC</sub>	GND

13. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

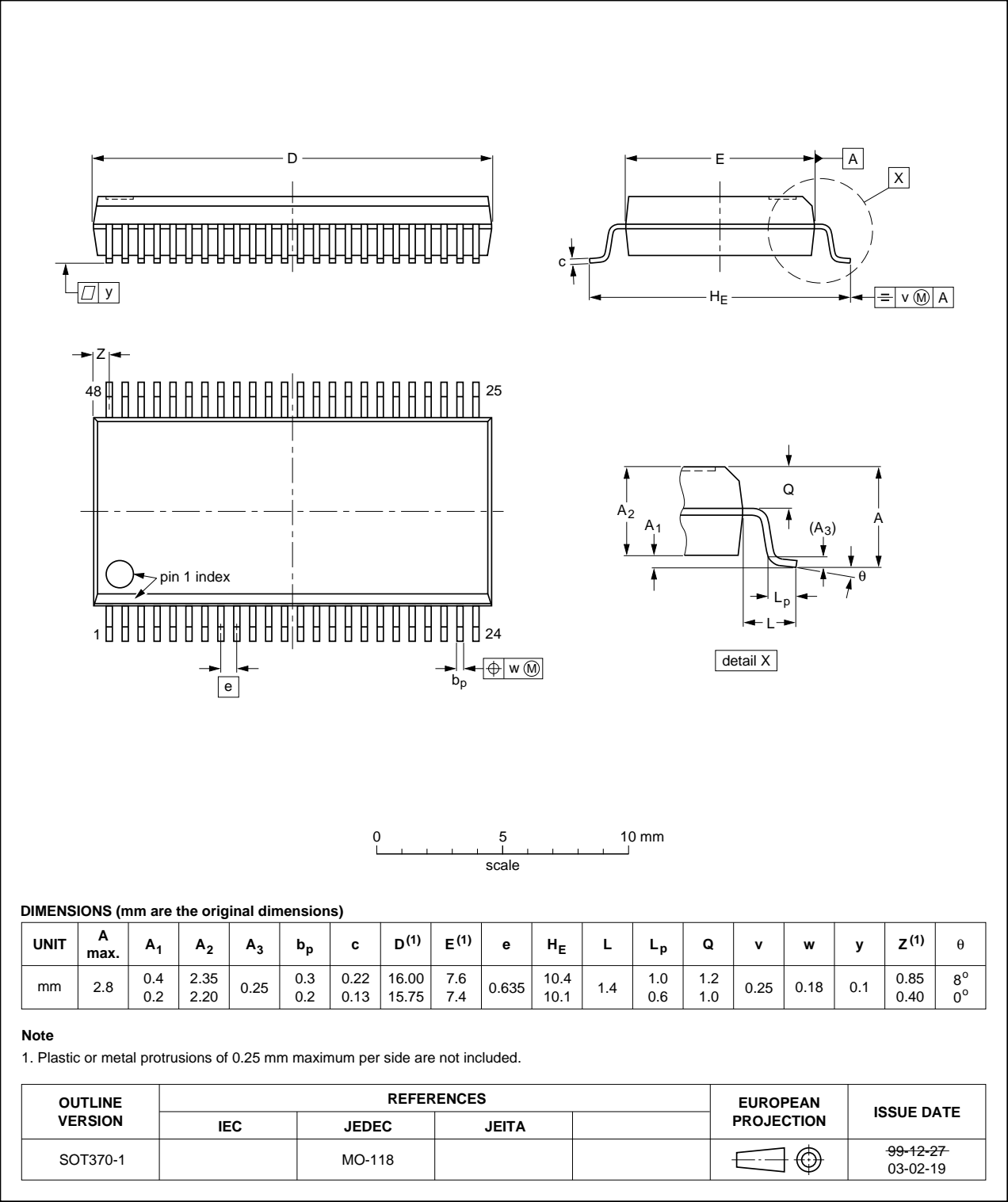


Fig 10. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

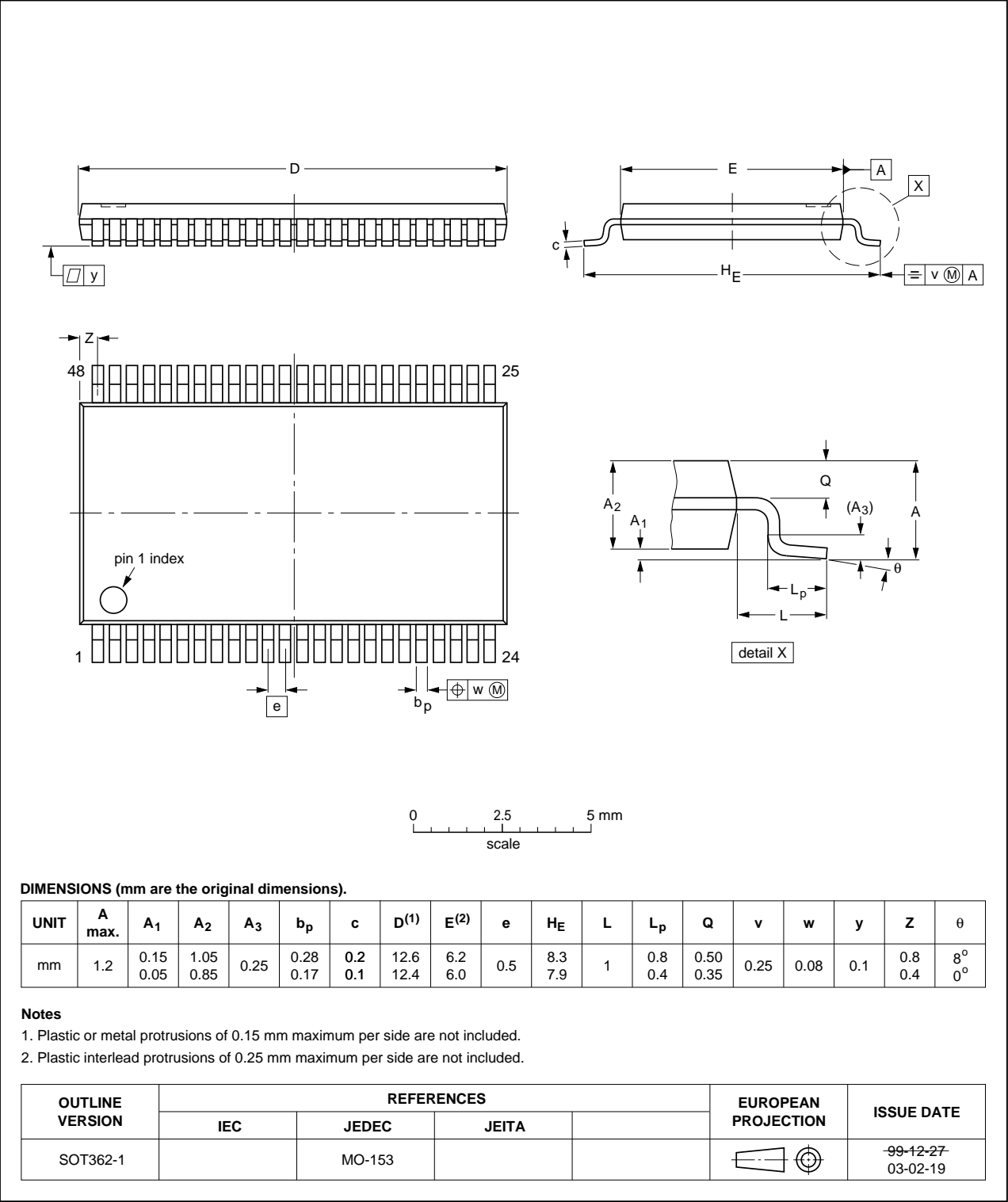


Fig 11. Package outline SOT362-1 (TSSOP48)

## 14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16374 v.5	20120709	Product data sheet	-	74ALVCH16374 v.4
Modifications:	• Table 8 corrected (errata).			
74ALVCH16374 v.4	20111117	Product data sheet	-	74ALVCH16374 v.3
Modifications:	• Legal pages updated.			
74ALVCH16374 v.3	20100427	Product data sheet	-	74ALVCH16374 v.2
74ALVCH16374 v.2	19980618	Product specification	-	74ALVCH16374 v.1

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 16.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 16.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)



## 18. Contents

---

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>4</b>
5.1	Pinning .....	4
5.2	Pin description .....	5
<b>6</b>	<b>Functional description</b> .....	<b>5</b>
6.1	Function table .....	5
<b>7</b>	<b>Limiting values</b> .....	<b>6</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>6</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>7</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>8</b>
<b>11</b>	<b>Waveforms</b> .....	<b>10</b>
<b>12</b>	<b>Test information</b> .....	<b>11</b>
<b>13</b>	<b>Package outline</b> .....	<b>12</b>
<b>14</b>	<b>Abbreviations</b> .....	<b>14</b>
<b>15</b>	<b>Revision history</b> .....	<b>14</b>
<b>16</b>	<b>Legal information</b> .....	<b>15</b>
16.1	Data sheet status .....	15
16.2	Definitions .....	15
16.3	Disclaimers .....	15
16.4	Trademarks .....	16
<b>17</b>	<b>Contact information</b> .....	<b>16</b>
<b>18</b>	<b>Contents</b> .....	<b>17</b>

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

---

© NXP B.V. 2012.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 9 July 2012

Document identifier: 74ALVCH16374