CT1508-2
MIL-STD-1397 Type E 10MHz
Serial Manchester 4-Bit SIS / SOS Decoder

Features

- **Unique Manchester decoder requires no clock**
- **4 Bit SIS / SOS output**
- **Operates with ±5 volt supply**
- **Removes sync, word identifier and parity bits**
- **Does both data and SIS / SOS decoding**
- **Detects parity on all received data**
- **Flags received messages with word lengths greater than 4 bits**
- **Accepts self-test inputs for BITE applications**
- **Generates one clock edge per received bit for bit counting applications**
- **May be used as a serial decoder for indefinite word lengths**
- **Interfaces directly to the CT1496-2 (Manchester Encoder) and CT1469-2 (Transceiver)**
- **MIL-PRF-38534 compliant devices available**

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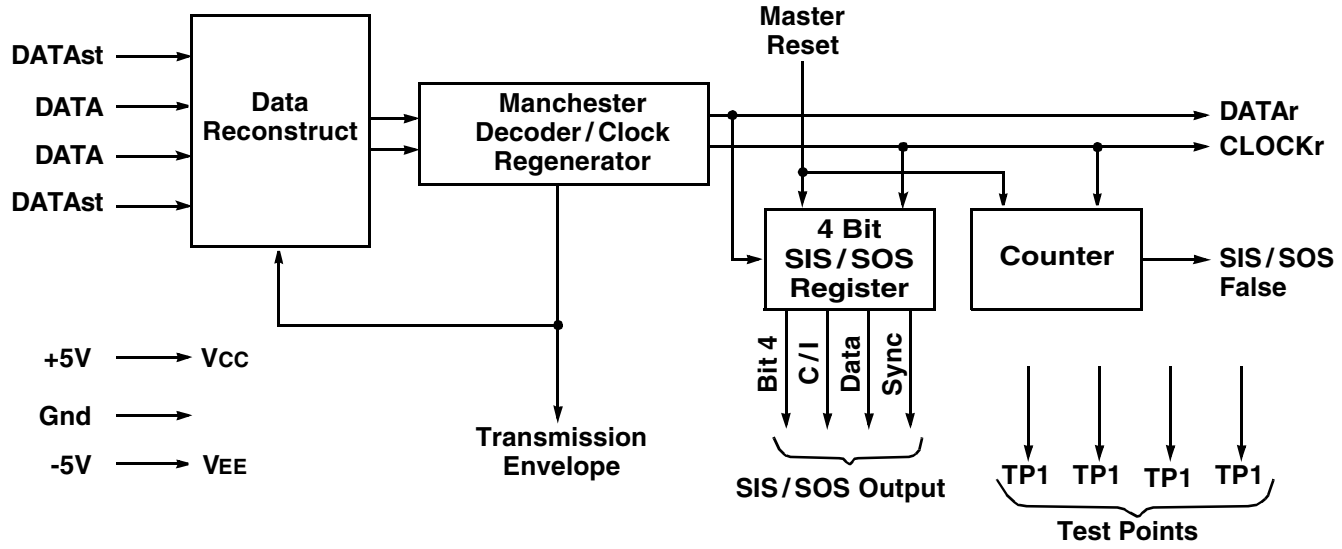
General Description

CT1508-2 is a hybrid microcircuit which incorporates a serial decoder in a single package. The encoder accepts a "N" Bit (Typically 4, 34 or 35) serial Manchester encoded TTL NRZ signals and outputs a 4 bit SIS / SOS TTL output along with "N" recovered data Bits/Clocks. Aeroflex Circuit Technology is a 80,000 square foot MIL-PRF-38534 certified facility in Plainview, N.Y.



Block Diagram

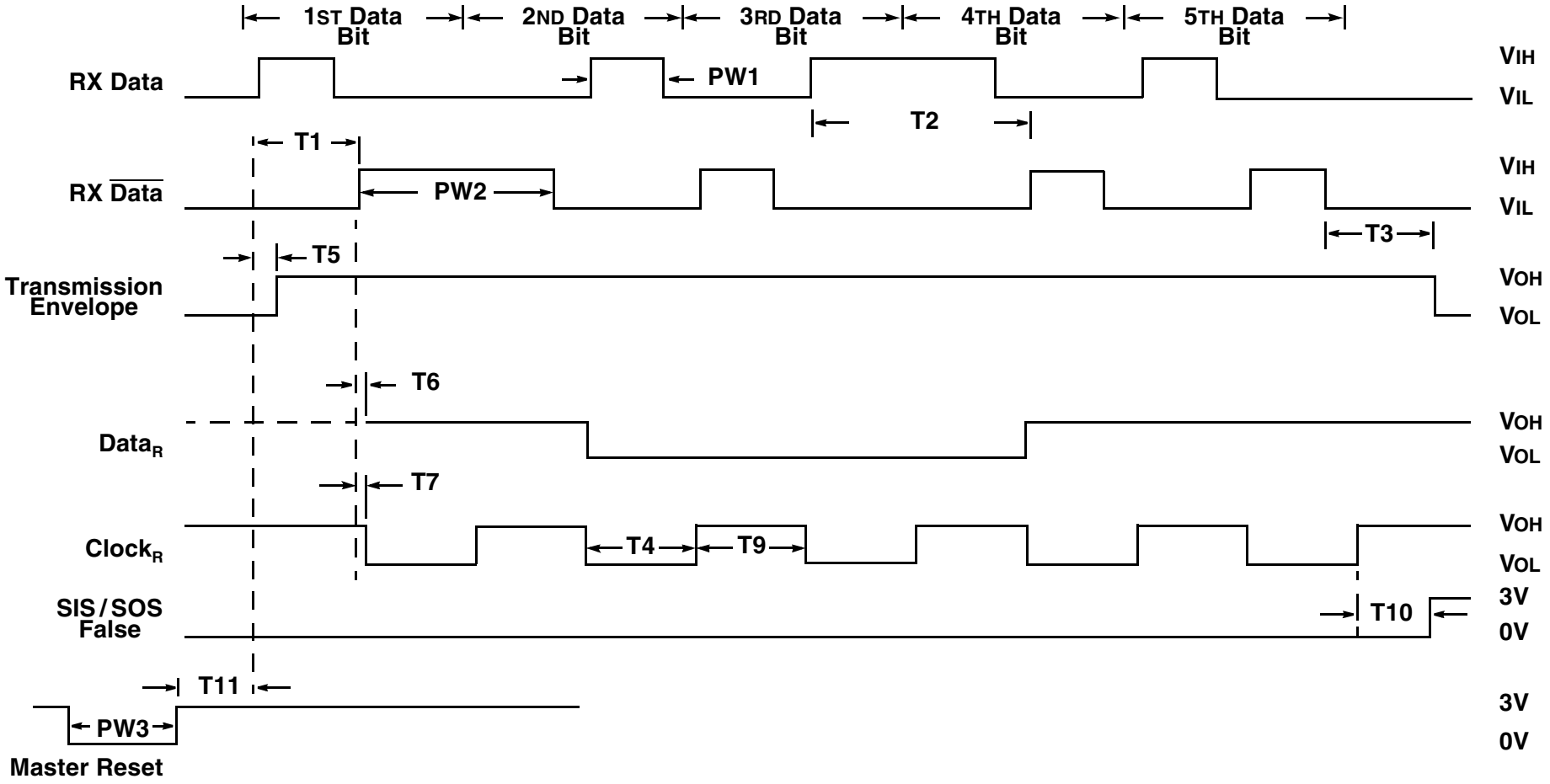


Figure 1 – Decoder Timing Waveforms

Absolute Maximum Ratings

Parameter	Rating	Units
Supply Voltage V_{CC} V_{EE}	 +7.0 -7.0	 V V
Input Voltage	+0.5 to +5.5	V
Applied Output Voltage	-0.5 to +7.0	V
Power Dissipation	2.17	W
Storage Temperature Range	-60 to +150	°C
Operating Case Temperature Range	-55 to +100	°C

DC Electrical Characteristics

(V_{DD} = 5V ±10%, T_C = -55 °C to +100°C, unless otherwise specified)

SYMBOL	PARAMETER	LIMIT
SIS / SOS False & SIS / SOS Outputs		
V_{OH}	Logic High Output Voltage	2.4V min @ I_{OH} = -50µA, V_{CC} = +4.5V
V_{OL}	Logic Low Output Voltage	0.4V max @ I_{OL} = 2mA, V_{CC} = +4.5V
$Clock_r$ & $Data_r$		
V_{OH}	Logic High Output Voltage	2.4V min @ I_{OH} = -150mA, V_{CC} = +4.5
V_{OL}	Logic Low Output Voltage	0.4V max @ I_{OL} = 6mA, V_{CC} = +4.5V
Transmission Envelope		
V_{OH}	Logic High Output Voltage	2.4V min @ I_{OH} = -200mA, V_{CC} = +4.5V
V_{OL}	Logic Low Output Voltage	0.4V max @ I_{OL} = 8mA, V_{CC} = +4.5V
RX DATA, RX $\overline{\text{DATA}}$, DATAst, $\overline{\text{DATA}}$st & Master Reset		
I_{IH}	Logic High Input Current	50µA max @ V_{IH} = 2.7V, V_{CC} = +5.5V
I_{IL}	Logic Low Input Current	2mA max @ V_{IL} = 0.4V, V_{CC} = +5.5V
DC Supply Currents		
I_{CC}	V_{CC} = +5.5V (pin 1)	360mA max
I_{EE}	V_{EE} = -5.5V (pin 9)	35mA max

Decoder Timing Characteristics

(V_{CC} = 5V ±10%, T_C = -55 °C to +100°C, See Figure 1, unless otherwise specified)

Symbol	Parameter / Condition	Min	Typ	Max	Unit
T1	Bit transition 0 - 0, 1 - 1	35	60	65	ns
T2	Bit transition 0 - 1, 1 - 0	90	100	130	ns
T3	Transmission envelope off delay	100	-	250	ns
T4	$Clock_R$ low time	35	50	65	ns
T5	Envelope delay time	-	25	40	ns
T6	Data decode delay	-	35	45	ns
T7	Clock low transition delay	-	50	-	ns
T8	Word Parity Delay	-	120	-	ns
T9	$Clock_R$ low time	35	50	65	ns
T10	SIS / SOS false delay time	-	40	80	ns
T11	minimum reset disable time	20	-	-	ns
PW1	Half Bit input pulse	20	50	65	ns
PW2	Full Bit input pulse	90	100	130	ns
PW3	Master reset pulse width	60	-	-	ns

Functional Description and Pinout

Pin #	Pin Name	Function	Load or Drive
1	V_{CC}	+5V ± 10%	-
9	V_{EE}	-5V ± 10%	-
2	RX $\overline{DATA}$	Connect to $\overline{DATA}$ output of RX	1 S Load
4	RX DATA	Connect to DATA output of RX	1 S Load
3	$\overline{DATA}_{ST}$	Connect to $\overline{DATA}_{ST}$ output of encoder	1 S Load
6	$DATA_{ST}$	Connect to $DATA_{ST}$ output of encoder	1 S Load
14	Transmission Envelope	High within approximately 40nSec of reception of first half bit; goes low approximately 100nSec after reception of last half bit (normally low in inactive state).	4 S Drives
19	SIS / SOS False	Reset to low state on clear. Goes high reception of transmission with word length greater than 4 bits.	1 S Drive
20 21 22 24	SIS / SOS Output (Pin 24 - LSB) (Pin 20 - MSB)	Last 4 bits received reside in this register until cleared. If valid SIS / SOS then register contains SIS / SOS message.	1 S Drive
17	$Data_R$	Reconstructed Data. Data state to be considered in conjunction with positive edges of $Clock_R$.	
8	$Clock_R$	Reconstructed Clock (approximately 50% duty cycle) to be used in conjunction with Reconstructed Data and maybe used for bit counting applications.	
7	Master Reset	Clears all data registers, bit counter, WORD PARITY on low. Must be used after each word to initialize bit counter and parity detector.	
11	TP1	Do not connect.	
15	TP2	Do not connect.	
16	TP3	Do not connect.	
13	TP4	Do not connect.	

Functional Description and Pinout (con't)

Pin #	Pin Name	Function	Load or Drive

General Notes:

1 S Load: Requires I_{IL} = 2 mA Max. I_{IH} = 50 µA Max. C_{IN} <15pF

1 S Drive: Requires I_{OH} = 50 µA Min. I_{OL} = 2 mA Min.

Thruput Delay - 150 nSec Max to serial outputs

Power Dissipation
1.38 Watts Typ +5V ±10% 250 mA Typ, 360 mA Max.
2.17 Watts Max. -5V ±10% 25 mA Typ, 35 mA Max.

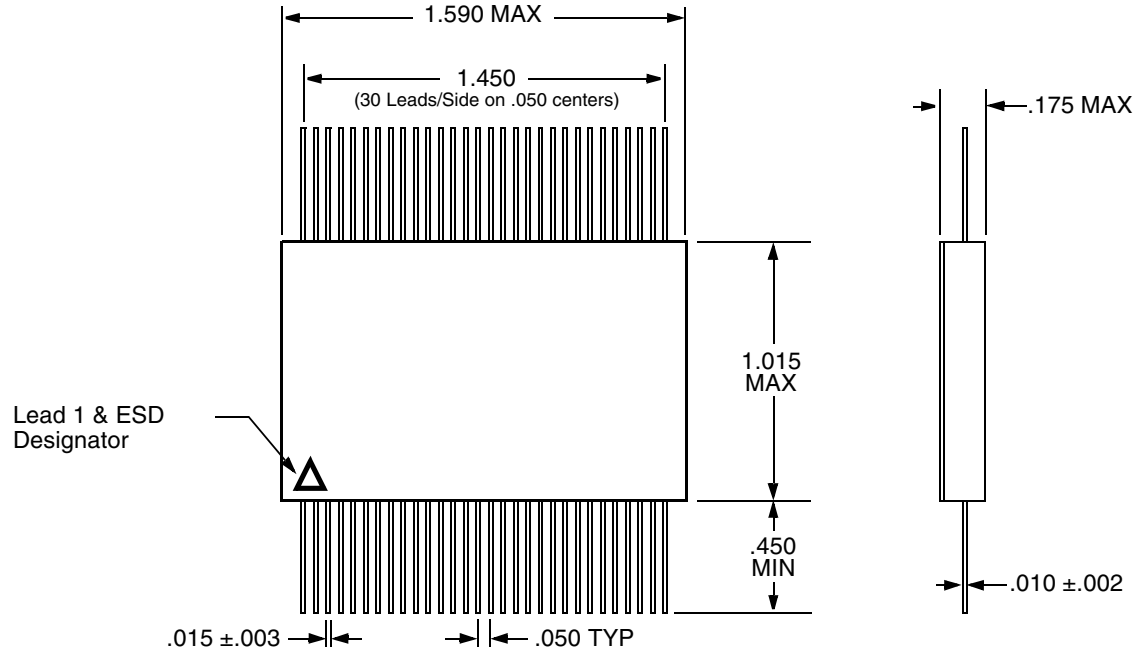
Power Sequence is not required.

Pin #'s	Functions	Pin #'s	Functions
1	Vcc (+5V)	31	NC
2	DATA	32	NC
3	DATA ST	33	NC
4	DATA	34	NC
5	GND	35	NC
6	$\overline{\text{DATA}}$ ST	36	NC
7	MASTER RESET	37	NC
8	CLOCK R	38	NC
9	V_{EE} (-5V)	39	NC
10	GND	40	NC
11	TP1	41	NC
12	GND	42	NC
13	TP4	43	NC
14	TRANSMISSION ENVELOPE	44	NC
15	TP2	45	NC
16	TP3	46	NC
17	DATA R	47	NC
18	GND	48	NC
19	SIS / SOS FALSE	49	NC
20	BIT 4	50	NC
21	C / I	51	NC
22	DATA (SIS/SOS)	52	NC
23	GND	53	NC
24	SYNC	54	NC
25	NC	55	NC
26	NC	56	NC
27	NC	57	NC
28	NC	58	NC
29	NC	59	NC
30	NC	60	NC

Ordering Information

Model Number	Package
CT1508-2	Flat Package

Flat Package Outline



Specifications subject to change without notice.

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