

CMOS 21-Stage Counter

High-Voltage Types (20-Volt Rating)

■ CD4045B is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, and input inverters for use in a crystal oscillator. The CD4045B configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers.

The first inverter is intended for use as a crystal oscillator/amplifier. However, it may be used as a normal logic inverter if desired. A crystal oscillator circuit can be made less sensitive to voltage-supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_p to V_{DD} , S_n to V_{SS}). See Fig. 1. The first inverter in conjunction with an outboard inverter, such as 1/6 CD4069, and R_X , C_X , and R_S can also be used to construct an RC oscillator. The following data is supplied as a guide in the selection of values for R_X , R_S , and C_X used in Fig. 11:

1. R_X max = 10 M Ω with R_S = 10 M Ω and C_X = 50 pF
2. C_X max = 25 μ F with R_S = 560 k Ω and R_X = 50 k Ω

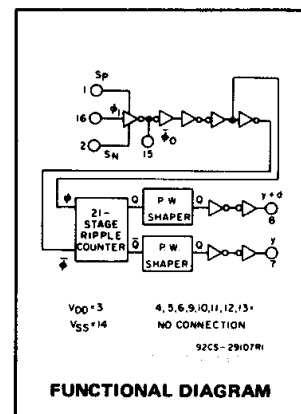
The CD4045B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline package (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Applications:

- Digital equipment in which ultra-low dissipation and/or operation using a battery source is required.
- Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.
- Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.

Features:

- Very low operating dissipation <1 mW (typ.) @ V_{DD} = 5 V, $f\phi$ = 1 MHz
- Output drivers with sink or source capability 7 mA (typ.) @ V_{DD} = 5 V
- Medium speed (typ.) $f\phi$ = 25 MHz @ V_{DD} = 10 V
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, Standard Specifications for Description of 'B' Series CMOS Devices"



MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	 -0.5V to +20V
Voltages referenced to V_{SS} Terminal	
INPUT VOLTAGE RANGE, ALL INPUTS	 -0.5V to V_{DD} + 0.5V
DC INPUT CURRENT, ANY ONE INPUT	 $\pm$ 10mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -55°C to +100°C	 500mW
For T_A = +100°C to +125°C	 Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	 100mW
OPERATING-TEMPERATURE RANGE (T_A)	 -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg})	 -85°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max	 +265°C

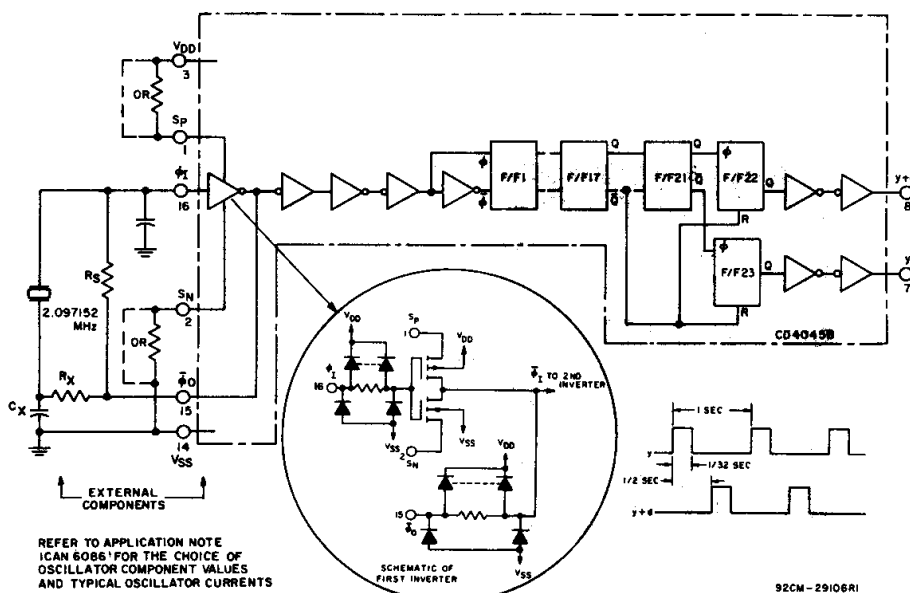


Fig. 1 – CD4045B and outboard components in a typical 21-stage counter application.

CD4045B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	4.5	4.3	2.9	2.5	3.6	7	—	mA
	0.5	0,10	10	11.2	10.5	7.7	6.3	9.1	18	—	
	1.5	0,15	15	29.4	28	19.6	16.8	23.8	47	—	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-4.5	-4.3	-2.9	-2.5	-3.6	-7	—	mA
	9.5	0,10	10	-11.2	-10.5	-7.7	-6.3	-9.1	-18	—	
	13.5	0,15	15	-29.4	-28	-19.6	-16.8	-23.8	-47	—	
Pin 15 Output Low and High Current, I _{OL} , I _{OH}	0.4,4.6	0,5	5	—				±0.1	±0.18	—	mA
	0.5,9.5	0,10	10	—				±0.2	±0.3	—	
	1.5,13.5	0,15	15	—				±0.5	±1	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	—	0.05	V
	—	0,10	10	0.05				—	—	0.05	
	—	0,15	15	0.05				—	—	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage V _{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	V
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I _{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	V _{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range)	—	3	18	V
Minimum Input-Pulse Width, t _W	5	—	100	ns
	10	—	50	
	15	—	40	
Maximum Input-Pulse Frequency, f _φ (External Pulse Source)	5	5	—	MHz
	10	12	—	
	15	15	—	

CD4045B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS			UNITS
			Min.	Typ.	Max.	
Propagation Delay Time: ϕ_1 to y or y+d out t_{PHL}, t_{PLH}		5 10 15	— — —	2.2 0.9 0.65	5.5 2.7 2	μs
Transition Time: t_{THL}, t_{TLH}		5 10 15	— — —	25 13 10	50 25 20	ns
Minimum Input-Pulse Width t_W		5 10 15	— — —	50 25 20	100 50 40	ns
Input-Pulse Rise or Fall Time: $t_r\phi, t_f\phi$		5 10 15	— — —	— — —	500 500 500	μs
Maximum Input-Pulse Frequency: (External Pulse Source) f_ϕ		5 10 15	5 12 15	10 25 30	— — —	MHz
Input Capacitance, C_{IN}	Any Input		—	5	7.5	pF
Variation of Output Frequency (Unit-to-Unit)	$f = 5\text{ MHz}$	5 10 15	— — —	0.05 0.03 0.1	— — —	%
RC Oscillator Operation						
Maximum Oscillator Frequency (See Fig. 11) f_{osc}	$R_X = 50\text{ k}\Omega$, $R_S = 560\text{ k}\Omega$, $C_X = 50\text{ pF}$	5 10 15	45 45 45	60 60 60	75 75 75	kHz

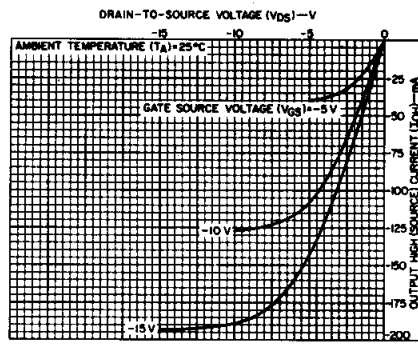


Fig. 4 - Typical output high (source) current characteristics.

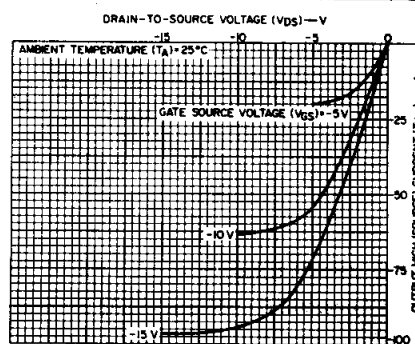


Fig. 5 - Minimum output high (source) current characteristics.

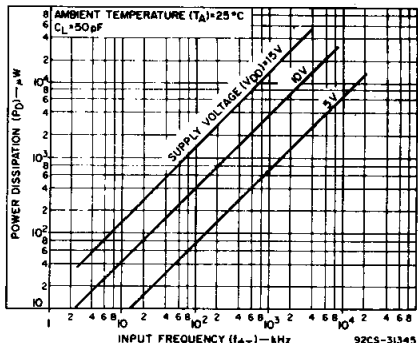


Fig. 7 - Typical power dissipation as a function of input frequency (21 counting stages).

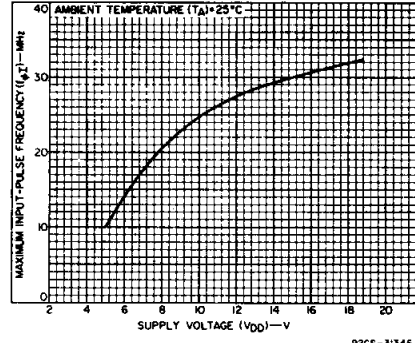


Fig. 8 - Typical maximum input-pulse frequency as a function of supply voltage.

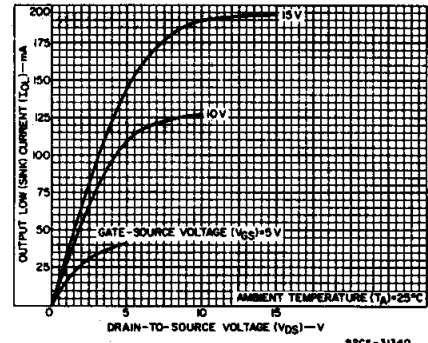


Fig. 2 - Typical output low (sink) current characteristics.

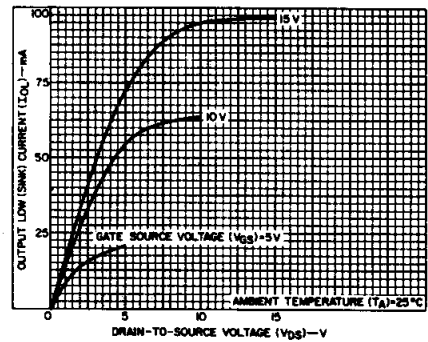


Fig. 3 - Minimum output low (sink) current characteristics.

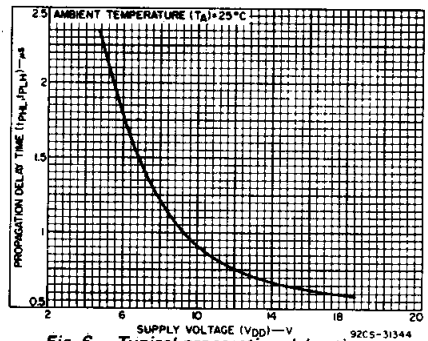


Fig. 6 - Typical propagation delay time as a function of supply voltage (ϕ_1 to y or y + d out vs. V_{DD}).

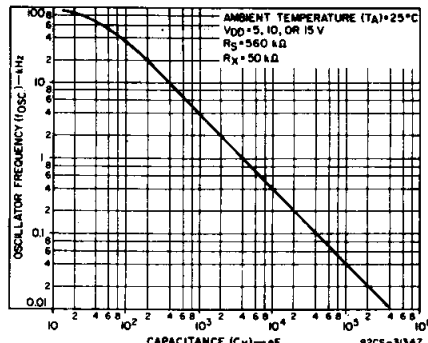


Fig. 9 - Typical RC oscillator frequency as a function of capacitance (C_X), See Fig. 11.

CD4045B Types

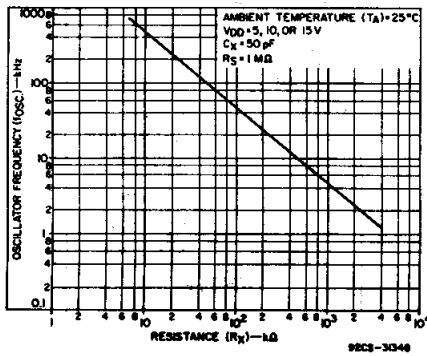


Fig. 10 - Typical RC oscillator frequency as a function of resistance (R_X). See Fig. 11.

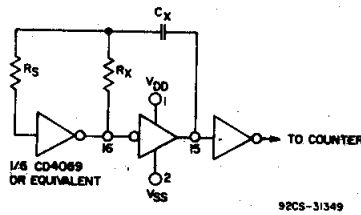


Fig. 11 - Typical RC circuit.

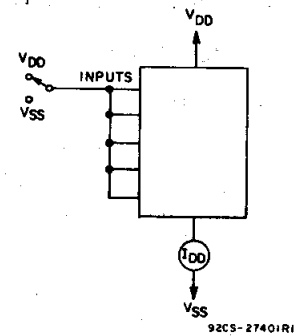


Fig. 12 - Quiescent-device-current test circuit.

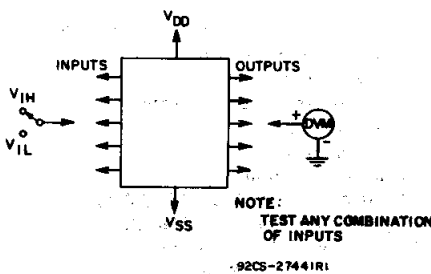


Fig. 13 - Noise-immunity test circuit.

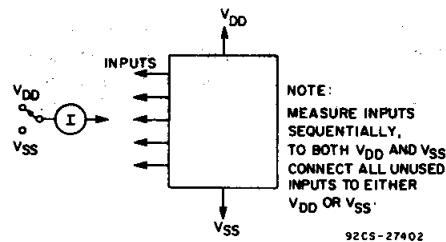


Fig. 14 - Input-leakage-current test circuit.

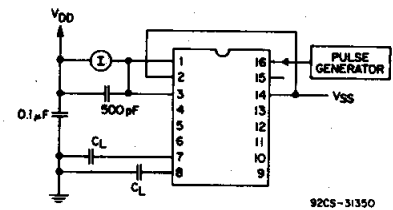
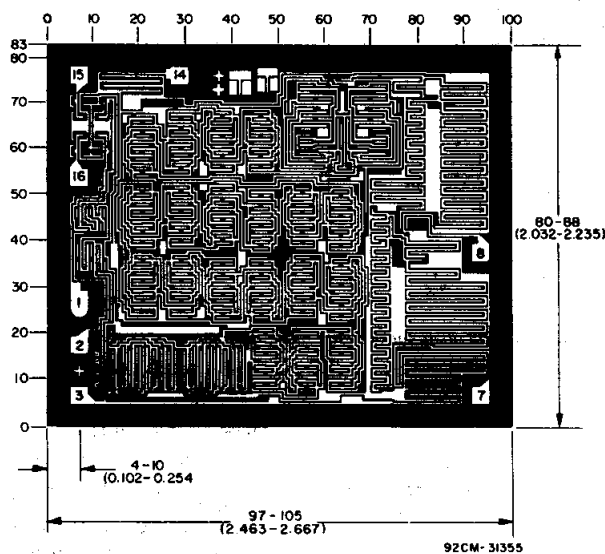


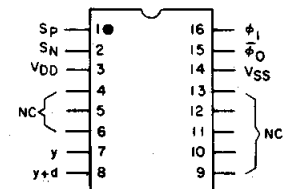
Fig. 15 - Dynamic power dissipation test circuit.



Chip dimensions and pad layout for CD4045B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

TERMINAL DIAGRAM Top View



NC = NO CONNECTION

NOTE Observe power-supply terminal connections, V_{DD} is terminal No. 3 and V_{SS} is terminal No. 14 (not 16 and 8 respectively, as in other CD4000B Series 16-lead devices).

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD4045BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4045BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4045BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4045BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4045BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

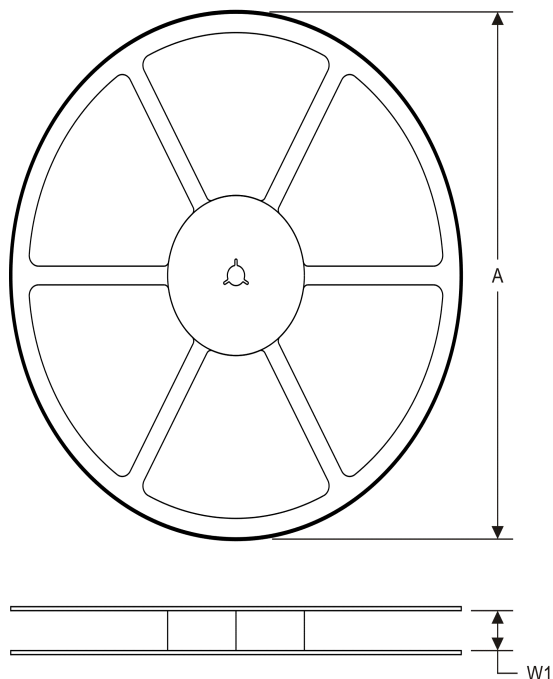
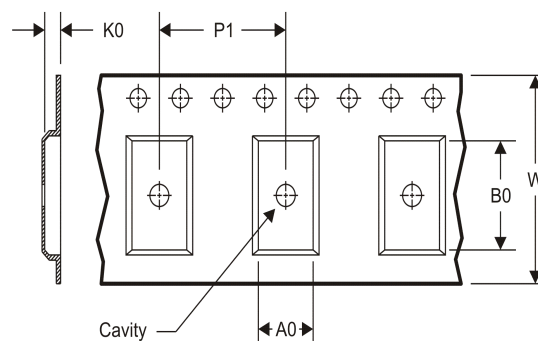
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


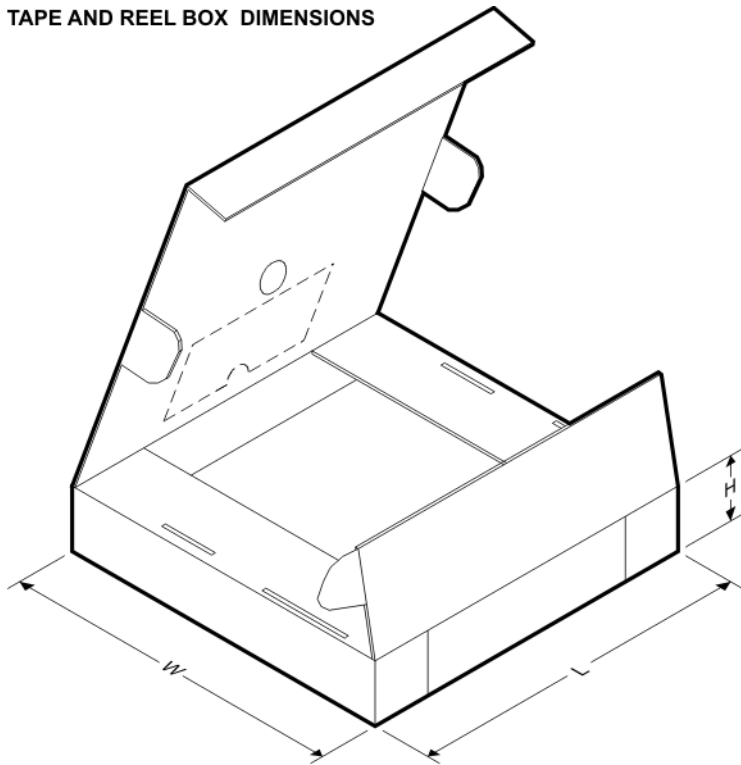
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4045BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



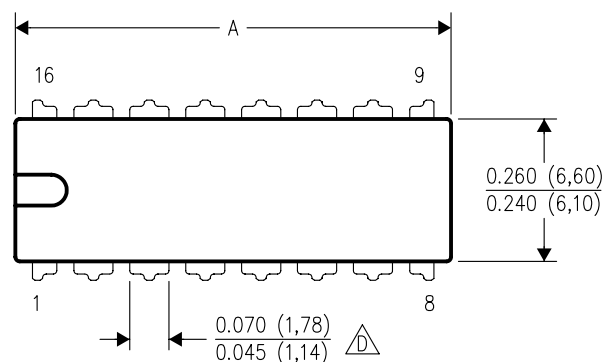
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4045BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

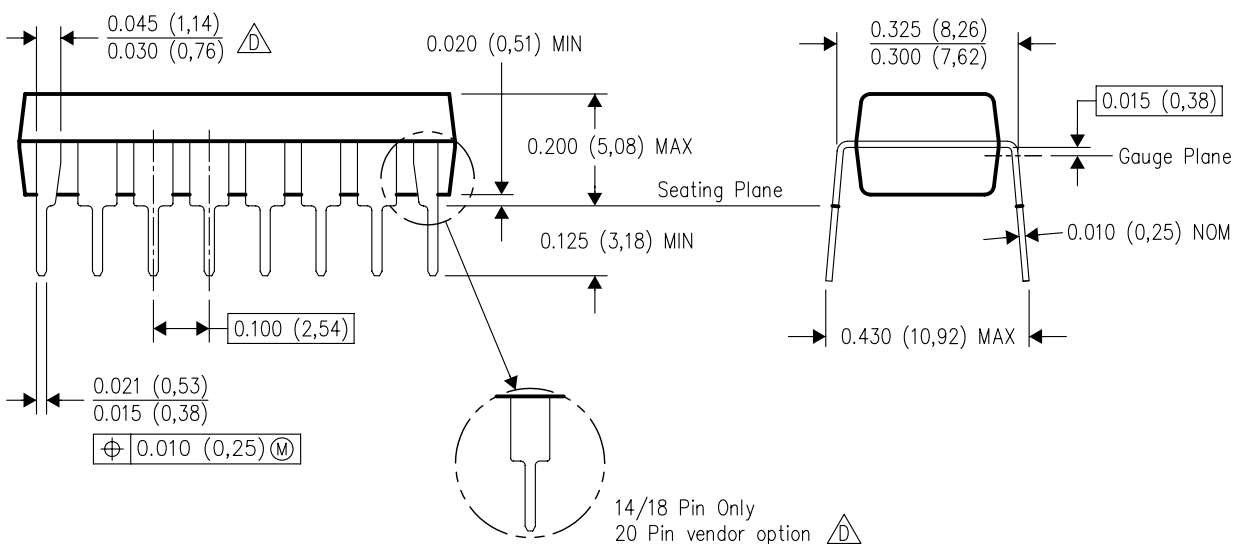
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



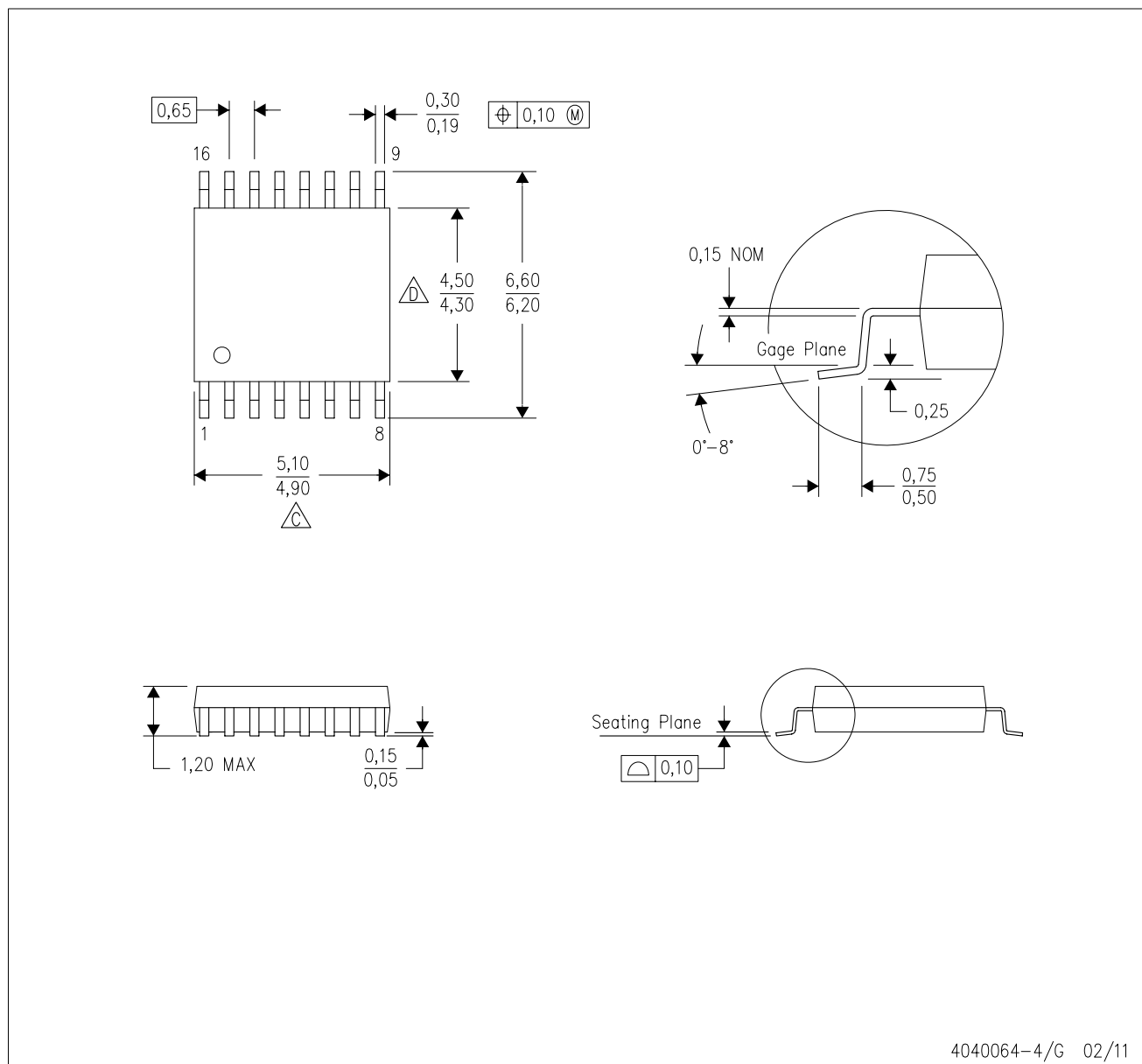
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

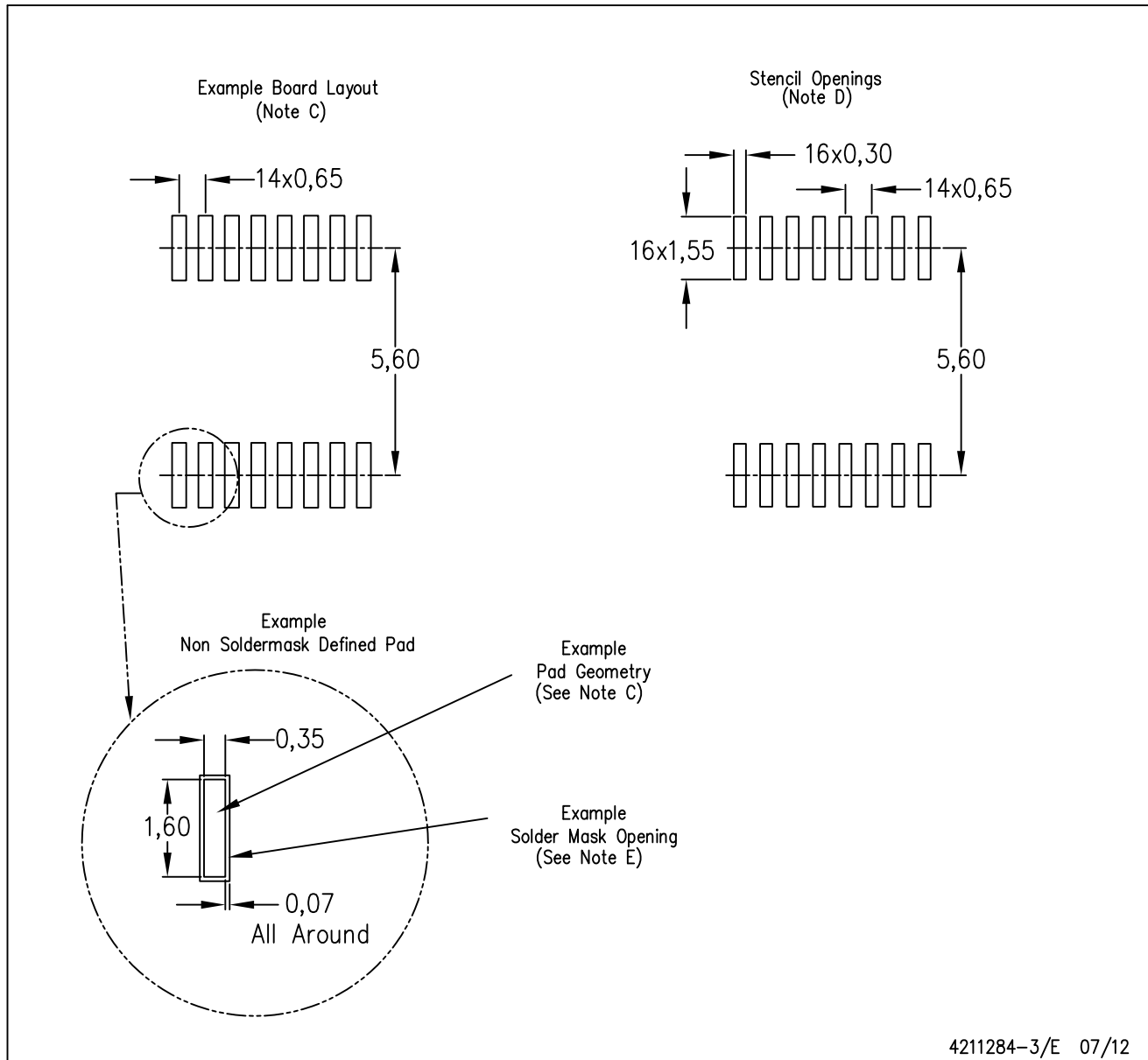


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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