



EMIF08-VID01F2

8 line low capacitance EMI filter
and ESD protection

Main product characteristics

Where EMI filtering in ESD sensitive equipment is required :

- LCD & camera for mobile phones
- Computers and printers
- Communication systems
- MCU Boards

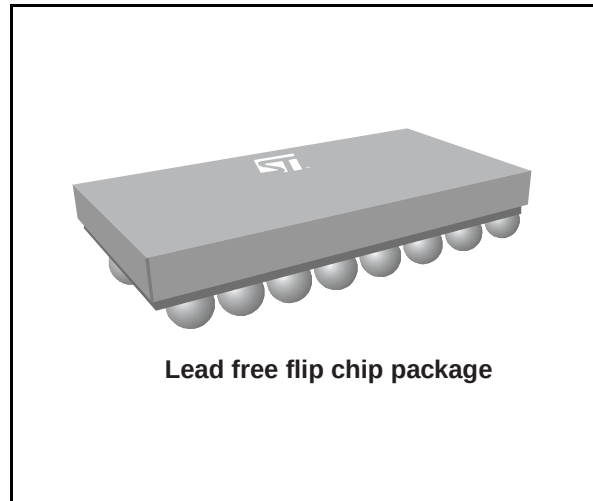
Description

The EMIF08-VID01F2 is an 8 line highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference. The flip chip packaging means the package size is equal to the die size.

This filter includes ESD protection circuitry, which prevents damage to the application when it is subjected to ESD surges up to 15kV.

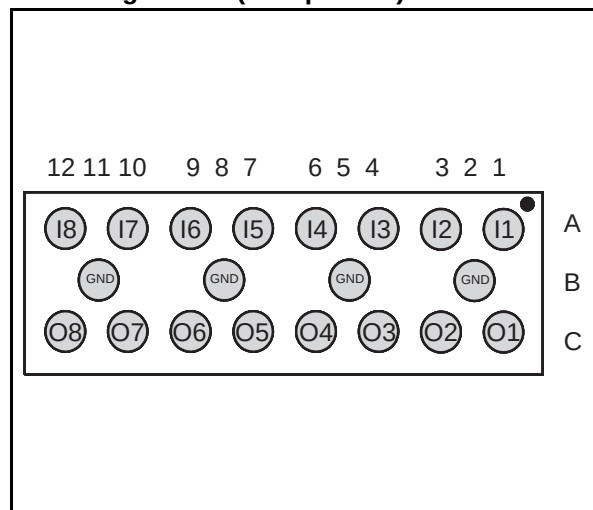
Benefits

- High efficiency EMI filter (-33 dB @ 900 Mhz)
- Low line capacitance suitable for high speed data bus
- Low serial resistance for camera impedance adaptation
- Optimized PCB space consuming: 1.29 mm x 3.92 mm
- Very thin package: 0.65 mm
- Lead free package
- High efficiency in ESD suppression on inputs pins (IEC61000-4-2 level 4).
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.



Lead free flip chip package

Pin configuration (Bumps side)



Complies with following standards:

IEC61000-4-2

level 4 input pins	15 kV	(air discharge)
	8 kV	(contact discharge)
level 1 output pins	2 kV	(air discharge)
	2 kV	(contact discharge)

MIL STD 883E - Method 3015-6 Class 3

Figure 1. Basic cell configuration

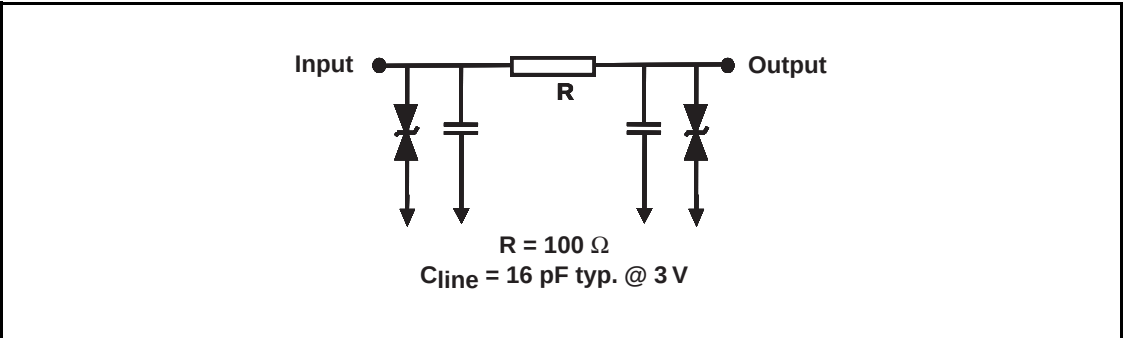
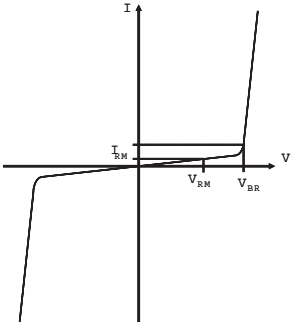


Table 1. Absolute ratings (limiting values)

Symbol	Parameter	Value	Unit
V _{pp}	ESD discharge IEC61000-4-2 air discharge	15	kV
	ESD discharge IEC61000-4-2 contact discharge	8	KV
T _j	Maximum junction temperature	125	°C
T _{op}	Operating temperature range	-40 to +85	°C
T _{stg}	Storage temperature range	-55 to +150	°C

1 Electrical characteristics (T_{amb} = 25°C)

Symbol	Parameters	
V _{BR}	Breakdown voltage	
I _{RM}	Leakage current @ V _{RM}	
V _{RM}	Stand-off voltage	
R	Series resistance between Input & Output	
C _{line}	Input capacitance per line	

Symbol	Test conditions	Min	Typ	Max	Unit
V _{BR}	I _R = 1mA	6	8	10	V
I _{RM}	V _{RM} = 3V per line			500	nA
R _{I/O}	I=10mA	80	100	120	Ω
C _{line}	V _R = 3V DC, 1 MHz		16	19	pF

Figure 2. S21 (dB) attenuation measurement

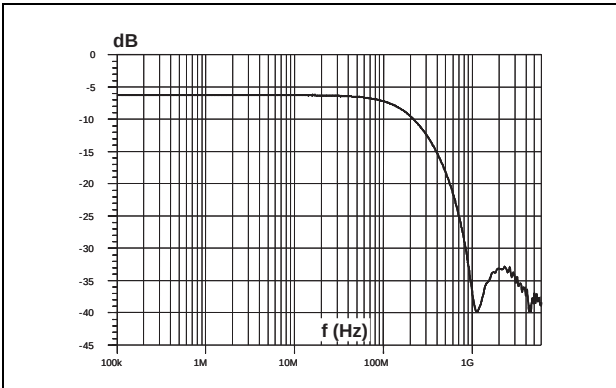


Figure 3. Analog crosstalk measurement

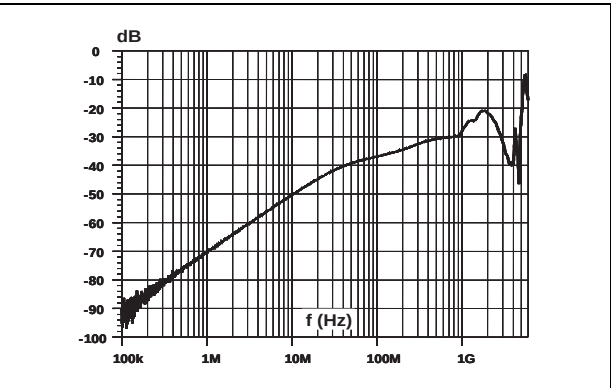


Figure 4. ESD response to IEC61000-4-2 (+15 kV air discharge) on one input V_{in} and one output V_{out}

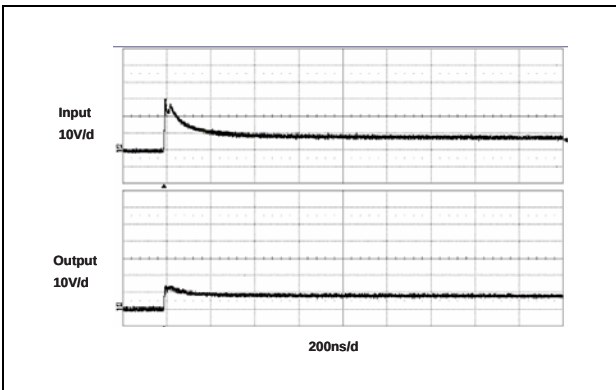


Figure 5. ESD response to IEC61000-4-2 (- 15 kV air discharge) on one input V_{in} and one output V_{out}

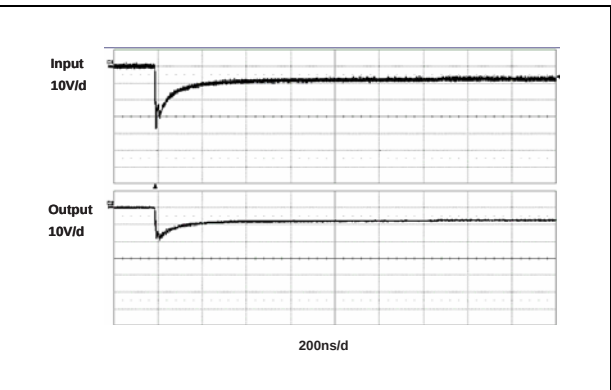
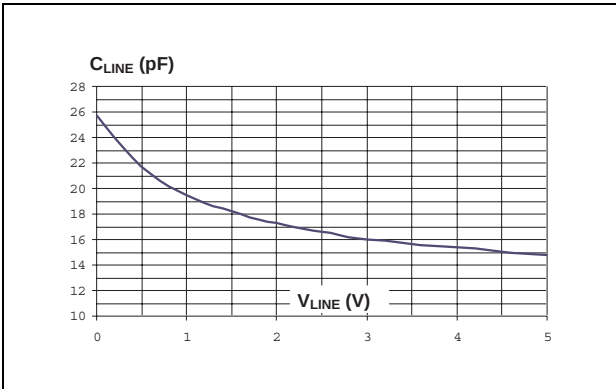
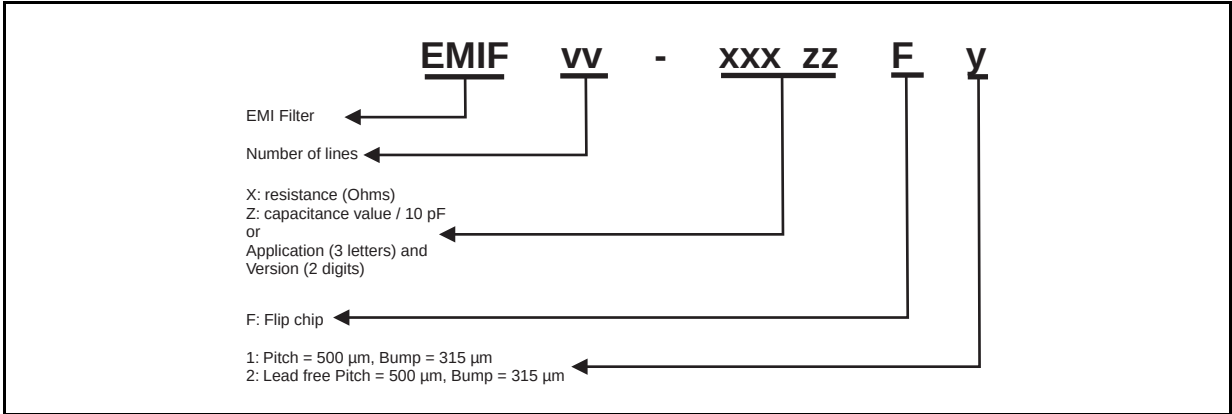


Figure 6. Line capacitance versus applied voltage



2 Ordering information scheme



3 Package mechanical data flip chip

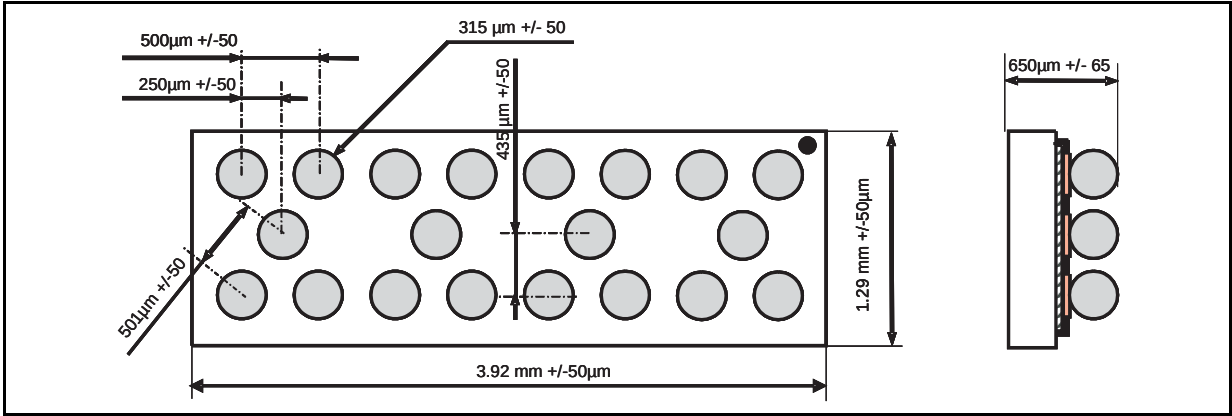


Figure 7. Marking

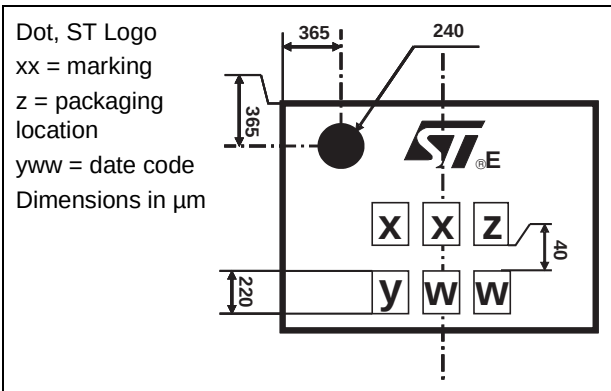


Figure 8. Foot print recommendation

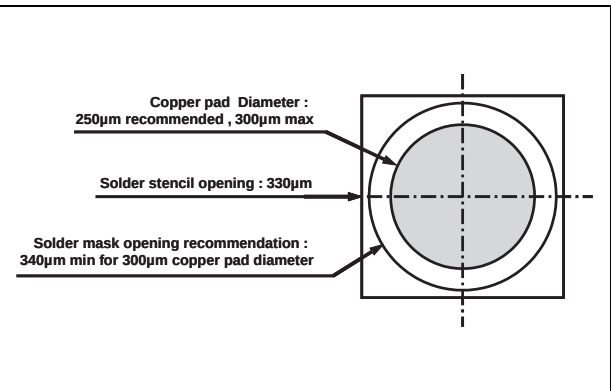
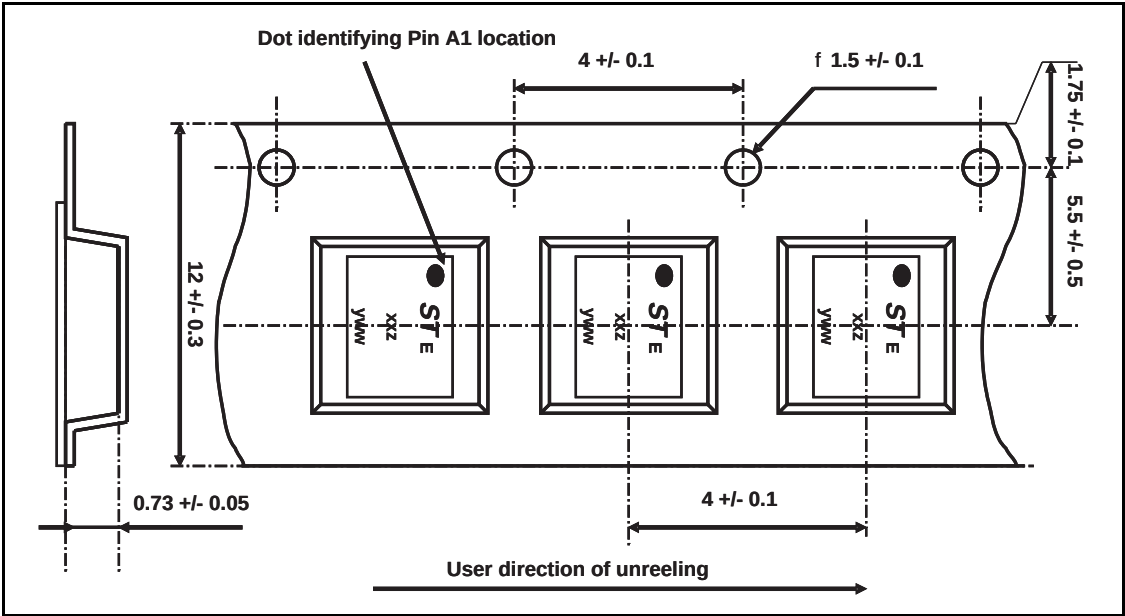


Figure 9. Flip chip tape and reel specification



4 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF08-VID01F2	GS	Flip Chip	6.8 mg	5000	7" Tape and reel

5 Revision history

Date	Revision	Changes
13-Jul-2005	1	Initial release.
11-Aug-2005	2	Fonts changed in Figures 7, 8, and 9

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