200mA 2-Terminal Programmable Current Source

FEATURES

- **Programmable 2-Terminal Current Source**
- **Maximum Output Current: 200mA**
- **Wide Input Voltage Range: 1.2V to 40V**
- **Input/Output Capacitors Not Required**
- **Resistor Ratio Sets Output Current**
- **Initial Set Pin Current Accuracy: 1%**
- **Reverse-Voltage Protection**
- **Reverse-Current Protection**
- <0.001%/V Line Regulation Typical
- Current Limit and Thermal Shutdown Protection
- Available in 8-Lead SOT-23, 3-Lead SOT-223 and 8-Lead 3mm × 3mm DFN Packages

APPLICATIONS

- 2-Terminal Floating Current Source
- GND Referred Current Source
- Variable Current Source
- In-Line Limiter
- Intrinsic Safety Circuits

DESCRIPTION

The LT®3092 is a programmable 2-terminal current source. It requires only two resistors to set an output current between 0.5mA and 200mA. A multitude of analog techniques lend themselves to actively programming the output current. The LT3092 is stable without input and output capacitors, offering high DC and AC impedance. This feature allows operation in intrinsically safe applications.

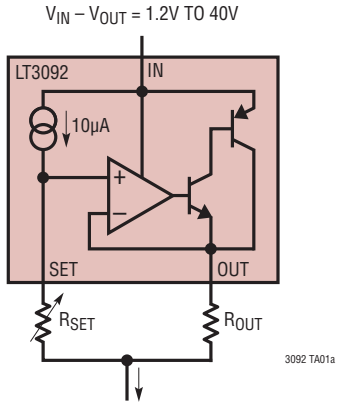
The SET pin features 1% initial accuracy and low temperature coefficient. Current regulation is better than 10ppm/V from 1.5V to 40V.

The LT3092 can operate in a 2-terminal current source configuration in series with signal lines. It is ideal for driving sensors, remote supplies, and as a precision current limiter for local supplies.

Internal protection circuitry includes reverse-battery and reverse-current protection, current limiting and thermal limiting. The LT3092 is offered in the 8-lead TSOT-23, 3-lead SOT-223 and 8-lead 3mm × 3mm DFN packages.

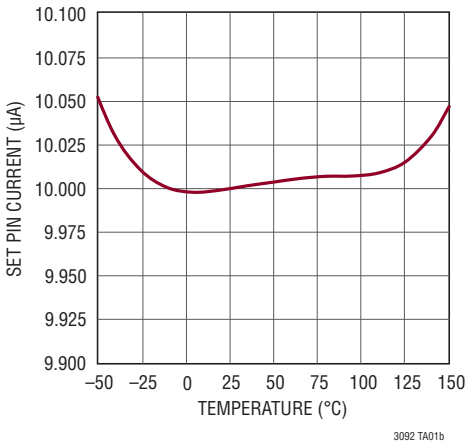
TYPICAL APPLICATION

Adjustable 2-Terminal Current Source



$$I_{SOURCE} = 10\mu A \bullet \frac{R_{SET}}{R_{OUT}}$$

SET Pin Current vs Temperature

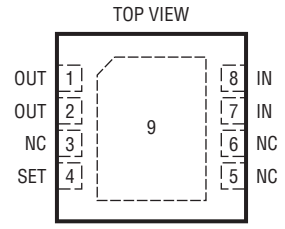


ABSOLUTE MAXIMUM RATINGS (Note 1) All Voltages Relative to V_{OUT}

IN Pin Voltage Relative to SET, OUT .....±40V
SET Pin Current (Note 6) .....±15mA
SET Pin Voltage (Relative to OUT, Note 6).....±10V
Output Short-Circuit Duration ..... Indefinite

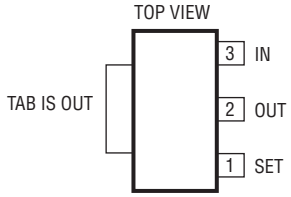
Operating Junction Temperature Range (Notes 2, 8)
E, I Grades ..... –40°C to 125°C
MP Grade..... –55°C to 125°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (ST, TS8 Packages Only)
Soldering, 10 sec..... 300°C

PIN CONFIGURATION



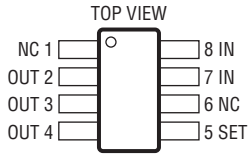
DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 28°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 9) IS OUT, MUST BE SOLDERED TO OUT ON THE PCB. SEE THE APPLICATIONS INFORMATION SECTION.



ST PACKAGE
3-LEAD PLASTIC SOT-223

T_{JMAX} = 125°C, θ_{JA} = 24°C/W, θ_{JC} = 15°C/W
TAB IS OUT, MUST BE SOLDERED TO OUT ON THE PCB. SEE THE APPLICATIONS INFORMATION SECTION.



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23

T_{JMAX} = 125°C, θ_{JA} = 57°C/W, θ_{JC} = 15°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3092EDD#PBF	LT3092EDD#TRPBF	LFJD	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3092IDD#PBF	LT3092IDD#TRPBF	LFJD	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3092EST#PBF	LT3092EST#TRPBF	3092	3-Lead Plastic SOT-223	–40°C to 125°C
LT3092IST#PBF	LT3092IST#TRPBF	3092	3-Lead Plastic SOT-223	–40°C to 125°C
LT3092MPST#PBF	LT3092MPST#TRPBF	3092MP	3-Lead Plastic SOT-223	–55°C to 125°C
LT3092ETS8#PBF	LT3092ETS8#TRPBF	LTFJW	8-Lead Plastic SOT-23	–40°C to 125°C
LT3092ITS8#PBF	LT3092ITS8#TRPBF	LTFJW	8-Lead Plastic SOT-23	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3092EDD	LT3092EDD#TR	LFJD	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3092IDD	LT3092IDD#TR	LFJD	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3092EST	LT3092EST#TR	3092	3-Lead Plastic SOT-223	–40°C to 125°C
LT3092IST	LT3092IST#TR	3092	3-Lead Plastic SOT-223	–40°C to 125°C
LT3092MPST	LT3092MPST#TR	3092MP	3-Lead Plastic SOT-223	–55°C to 125°C
LT3092ETS8	LT3092ETS8#TR	LTFJW	8-Lead Plastic SOT-23	–40°C to 125°C
LT3092ITS8	LT3092ITS8#TR	LTFJW	8-Lead Plastic SOT-23	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
SET Pin Current	I_{SET}	V_{IN} = 2V, I_{LOAD} = 1mA		9.9	10	10.1	µA
		2V ≤ V_{IN} ≤ 40V, 1mA ≤ I_{LOAD} ≤ 200mA	●	9.8	10	10.2	µA
Offset Voltage (V_{OUT} – V_{SET})	V_{OS}	V_{IN} = 2V, I_{LOAD} = 1mA		–2		2	mV
		V_{IN} = 2V, I_{LOAD} = 1mA	●	–4		4	mV
Current Regulation (Note 7)	ΔI_{SET}	ΔI_{LOAD} = 1mA to 200mA			–0.1		nA
	ΔV_{OS}	ΔI_{LOAD} = 1mA to 200mA	●		–0.5	–2	mV
Line Regulation	ΔI_{SET}	ΔV_{IN} = 2V to 40V, I_{LOAD} = 1mA			0.03	0.2	nA/V
	ΔV_{OS}	ΔV_{IN} = 2V to 40V, I_{LOAD} = 1mA			0.003	0.010	mV/V
Minimum Load Current (Note 3)		2V ≤ V_{IN} ≤ 40V	●		300	500	µA
Dropout Voltage (Note 4)		I_{LOAD} = 10mA	●		1.22	1.45	V
		I_{LOAD} = 200mA	●		1.3	1.65	V
Current Limit		V_{IN} = 5V, V_{SET} = 0V, V_{OUT} = –0.1V	●	200	300		mA
Reference Current RMS Output Noise (Note 5)		10Hz ≤ f ≤ 100kHz			0.7		nA_{RMS}
Ripple Rejection		f = 120Hz, V_{RIPPLE} = 0.5V_{P-P}, I_{LOAD} = 0.1A, C_{SET} = 0.1µF, C_{OUT} = 2.2µF			90		dB
		f = 10kHz			75		dB
		f = 1MHz			20		dB
Thermal Regulation	I_{SET}	10ms Pulse			0.003		%/W

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Unless otherwise specified, all voltages are with respect to V_{OUT}. The LT3092E is tested and specified under pulse load conditions such that $T_J \cong T_A$. The LT3092E is 100% tested at T_A = 25°C. Performance at –40°C and 125°C is assured by design, characterization, and correlation with statistical process controls. The LT3092I is guaranteed to meet all data sheet specifications over the full –40°C to 125°C operating junction temperature range. The LT3092MP is 100% tested and guaranteed over the –55°C to 125°C operating junction temperature range.

Note 3: Minimum load current is equivalent to the quiescent current of the part. Since all quiescent and drive current is delivered to the output of the part, the minimum load current is the minimum current required to maintain regulation.

Note 4: For the LT3092, dropout is specified as the minimum input-to-output voltage differential required supplying a given output current.

Note 5: Adding a small capacitor across the reference current resistor lowers output noise. Adding this capacitor bypasses the resistor shot noise and reference current noise (see the Applications Information section).

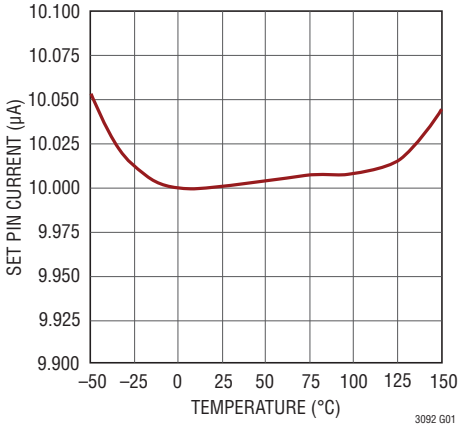
Note 6: Diodes with series 1k resistors clamp the SET pin to the OUT pin. These diodes and resistors only carry current under transient overloads.

Note 7: Current regulation is Kelvin-sensed at the package.

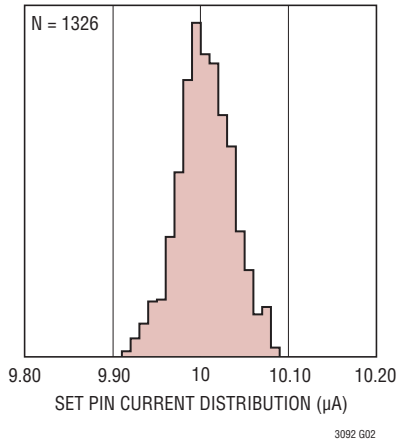
Note 8: This IC includes overtemperature protection that protects the device during momentary overload conditions. Junction temperature exceeds the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

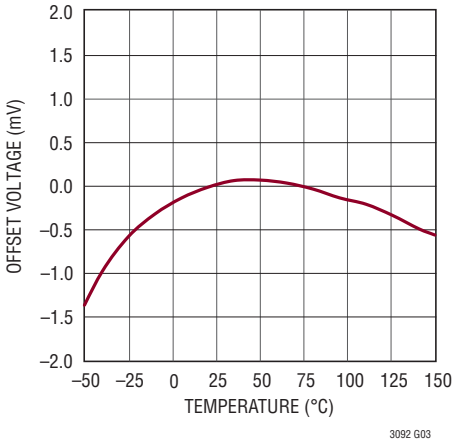
SET Pin Current



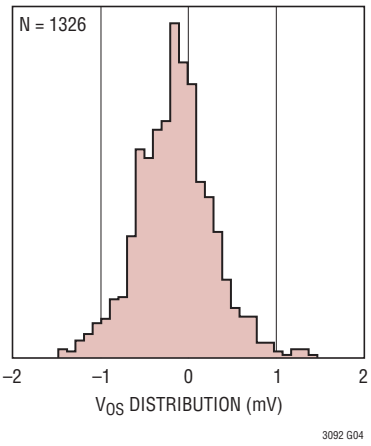
SET Pin Current Distribution



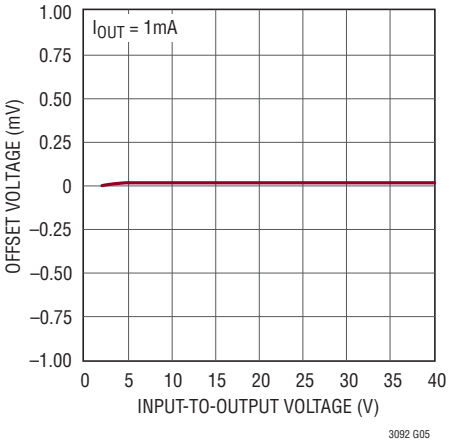
Offset Voltage ($V_{OUT} – V_{SET}$)



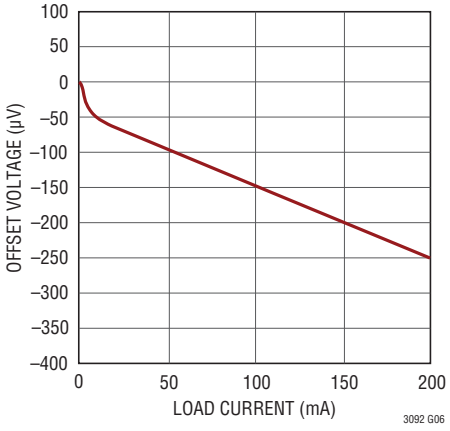
Offset Voltage Distribution



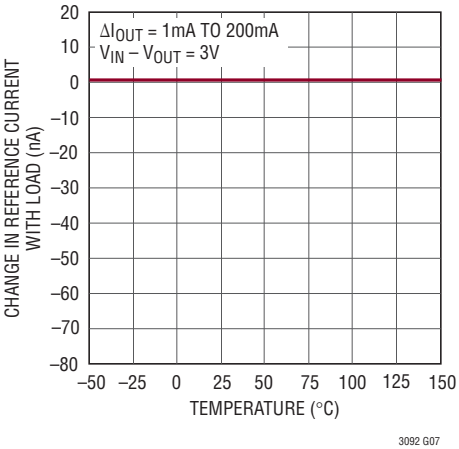
Offset Voltage



Offset Voltage

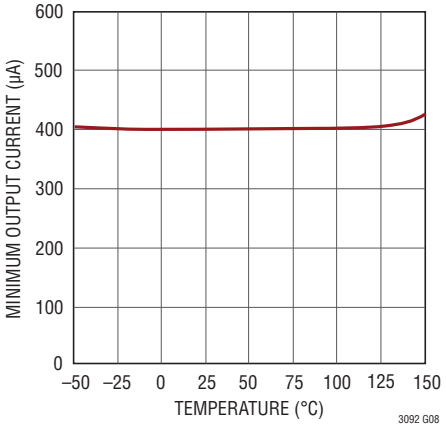


Current Regulation

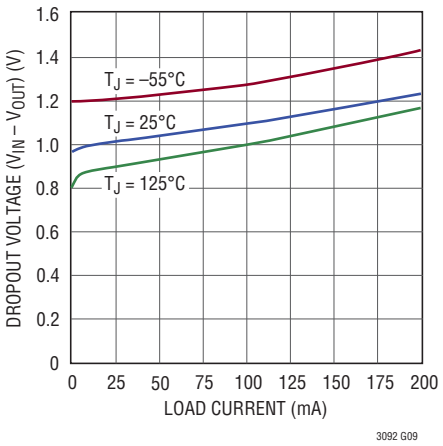


TYPICAL PERFORMANCE CHARACTERISTICS

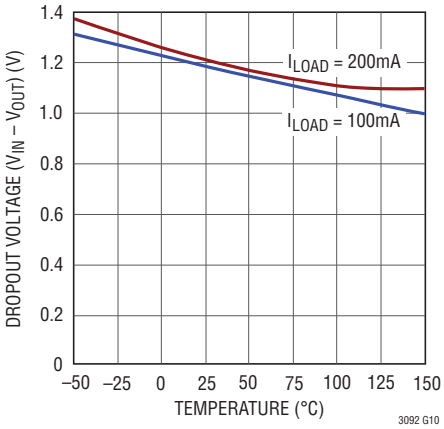
Minimum Output Current



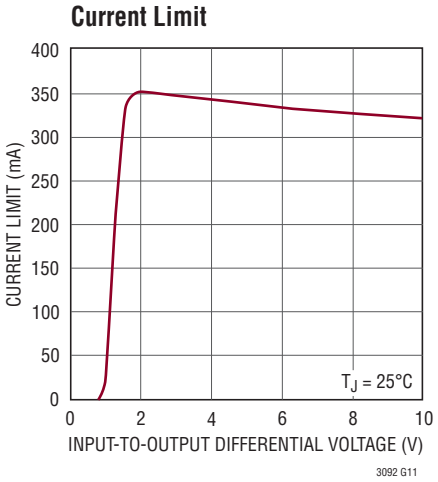
Dropout Voltage



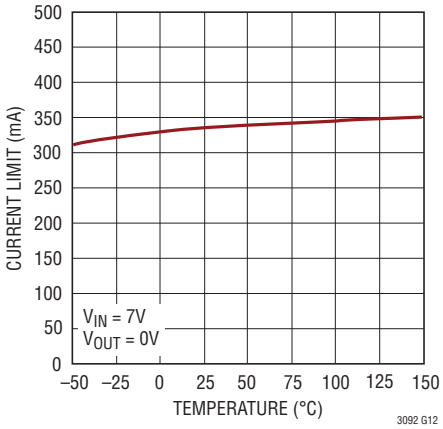
Dropout Voltage



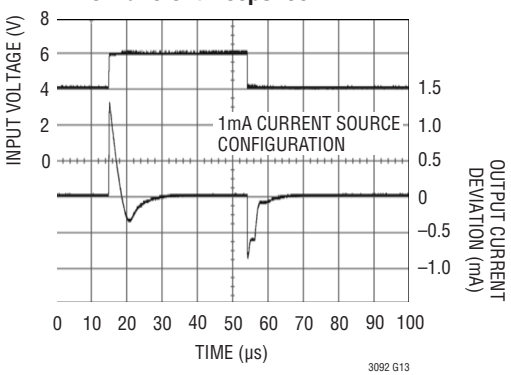
Current Limit



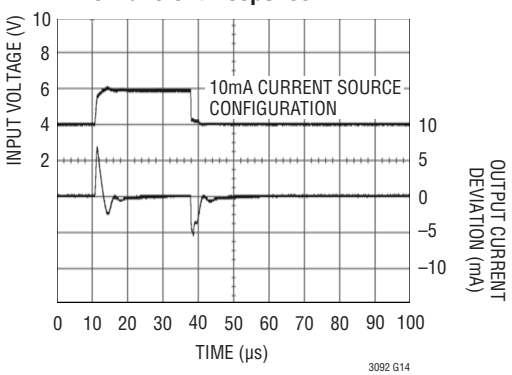
Current Limit



Line Transient Response

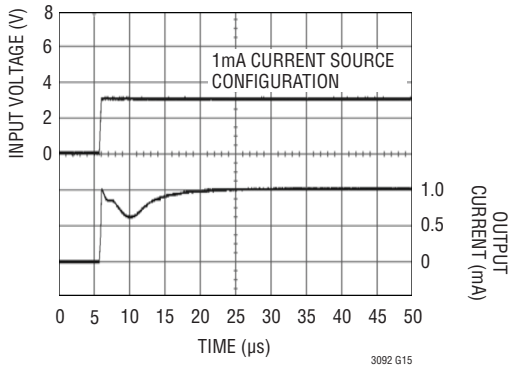


Line Transient Response

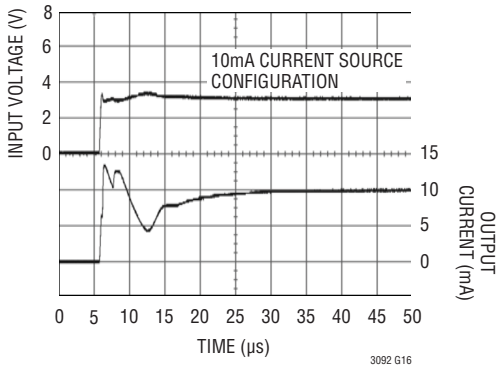


TYPICAL PERFORMANCE CHARACTERISTICS

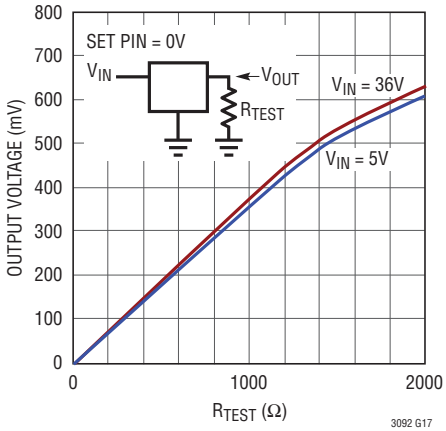
Turn-On Response



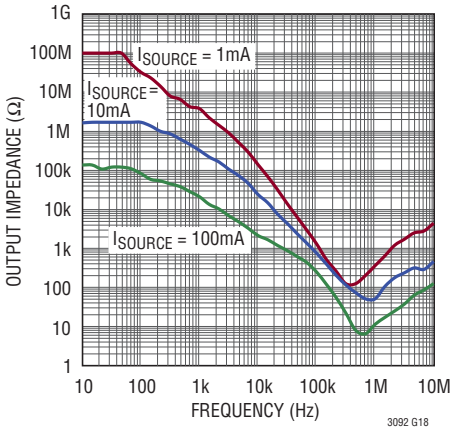
Turn-On Response



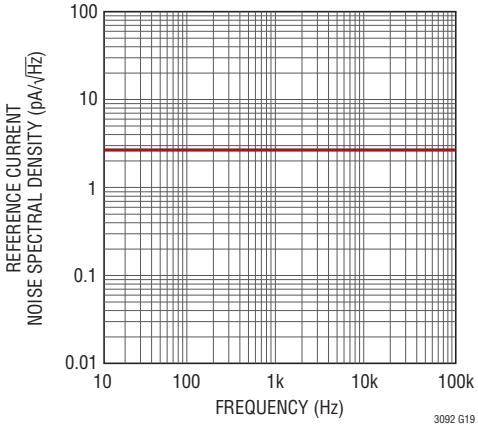
Residual Output for Less Than Minimum Output Current



Output Impedance



Noise Spectral Density



PIN FUNCTIONS (DD/ST/TS8)

IN (Pins 7, 8/Pin 3/Pins 7, 8): Input. This pin supplies power to bias internal circuitry and supply output load current. For the device to operate properly and regulate, the voltage on this pin must be 1.2V to 1.4V above the OUT pin (depending on output load current—see the dropout voltage specifications in the Electrical Characteristics table).

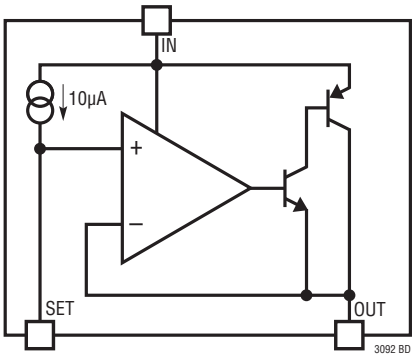
NC (Pins 3, 5, 6/NA/Pins 1, 6): No Connection. These pins have no connection to internal circuitry and may be tied to IN, OUT, GND or floated.

OUT (Pins 1, 2/Pin 2/Pins 2, 3, 4): Output. This is the power output of the device. The minimum current source value to which the LT3092 can be set is 0.5mA or the device will not regulate.

SET (Pin 4/Pin 1/Pin 5): Set. This pin is the error amplifier's noninverting input and also sets the operating bias point of the circuit. A fixed 10µA current source flows out of this pin. Two resistors program I_{OUT} as a function of the resistor ratio relative to 10µA. Output current range is 0.5mA to the maximum rated 200mA level.

Exposed Pad/Tab (Pin 9/Tab/NA): Output. The Exposed Pad of the DFN package and the Tab of the SOT-223 package are tied internally to OUT. Tie them directly to the OUT pins (Pins 1, 2/Pin 2) at the PCB. The amount of copper area and planes connected to OUT determine the effective thermal resistance of the packages (see the Applications Information section).

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Introduction

The LT3092 is a versatile IC that operates as a 2-terminal programmable current source with the addition of only two external resistors; no external bypass capacitors are needed for stability.

The LT3092 is easy to use and has all the protection features expected in high performance products. Included are reverse-voltage protection, reverse-current protection, short-circuit protection and thermal shutdown with hysteresis.

The LT3092 operates with or without input and output capacitors. The simplest current source application requires only two discrete resistors to set a constant output current up to 200mA. A variety of analog techniques lend themselves to regulating and varying the current source value.

The device utilizes a precision "0" TC 10µA reference current source to program output current. This 10µA current source connects to the noninverting input of a power operational amplifier. The power operational amplifier provides a low impedance buffered output of the voltage on the noninverting input.

Many application areas exist in which operation without input and output capacitors is advantageous. A few of these applications include sensitive circuits that cannot endure surge currents under fault or overload conditions and intrinsic safety applications in which safety regulations limit energy storage devices that may spark or arc.

Programming Output Current in 2-Terminal Current Source Mode

Setting the LT3092 to operate as a 2-terminal current source is a simple matter. The 10µA reference current from the SET pin is used with one resistor to generate a small voltage, usually in the range of 100mV to 1V (200mV is a level that will help reject offset voltage, line regulation, and other errors without being excessively large). This voltage is then applied across a second resistor that connects from OUT to the first resistor. Figure 1 shows connections and formulas to calculate a basic current source configuration.

With a 10µA current source generating the reference that gains up to set output current, leakage paths to or from the SET pin can create errors in the reference and output currents. High quality insulation should be used (e.g., Teflon, Kel-F). The cleaning of all insulating surfaces to remove fluxes and other residues may be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Minimize board leakage by encircling the SET pin and circuitry with a guard ring operated at a potential close to itself; tie the guard ring to the OUT pin. Guarding both sides of the circuit board is required. Bulk leakage reduction depends on the guard ring width. Ten nanoamperes of leakage into or out of the SET pin and its associated circuitry creates a 0.1% reference current error. Leakages of this magnitude, coupled with other sources of leakage, can cause significant offset voltage and reference current drift, especially over the possible operating temperature range.

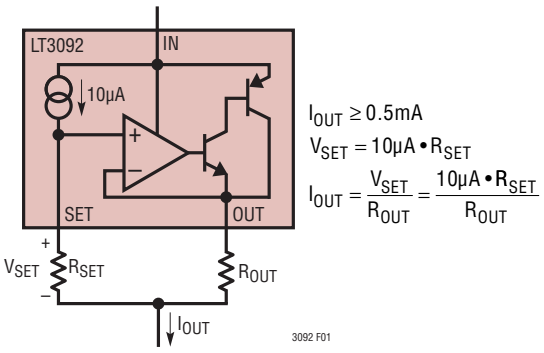


Figure 1. Using the LT3092 as a Current Source

Selecting R_{SET} and R_{OUT}

In Figure 1, both resistors R_{SET} and R_{OUT} program the value of the output current. The question now arises: the ratio of these resistors is known, but what value should each resistor be?

The first resistor to select is R_{SET}. The value selected should generate enough voltage to minimize the error caused by the offset between the SET and OUT pins. A reasonable starting level is 200mV of voltage across R_{SET} (R_{SET} equal to 20k). Resultant errors due to offset voltage are a few percent. The lower the voltage across R_{SET} becomes, the higher the error term due to the offset.

APPLICATIONS INFORMATION

From this point, selecting R_{OUT} is easy, as it is a straightforward calculation from R_{SET}. Take note, however, resistor errors must be accounted for as well. While larger voltage drops across R_{SET} minimize the error due to offset, they also increase the required operating headroom.

Obtaining the best temperature coefficient does not require the use of expensive resistors with low ppm temperature coefficients. Instead, since the output current of the LT3092 is determined by the ratio of R_{SET} to R_{OUT}, those resistors should have matching temperature characteristics. Less expensive resistors made from the same material will provide matching temperature coefficients. See resistor manufacturers' data sheets for more details.

Stability and Frequency Compensation

The LT3092 does not require input or output capacitors for stability in many current-source applications. Clean, tight PCB layouts provide a low reactance, well controlled operating environment for the LT3092 without requiring capacitors to frequency-compensate the circuit. The front page Typical Application circuit illustrates the simplicity of using the LT3092.

Some current source applications will use a capacitor connected in parallel with the SET pin resistor to lower the current source's noise. This capacitor also provides a soft-start function for the current source. This capacitor connection is depicted in Figure 7 (see the Quieting the Noise section).

When operating with a capacitor across the SET pin resistor, external compensation is usually required to maintain stability and compensate for the introduced pole. The following paragraphs discuss methods for stabilizing the LT3092 for either this capacitance or other complex impedances that may be presented to the device. Linear Technology strongly recommends testing stability in situ with final components before beginning production.

Although the LT3092's design strives to be stable without any capacitors over a wide variety of operating conditions, it is not possible to test for all possible combinations of input and output impedances that the LT3092 will encounter. These impedances may include resistive, capacitive and inductive components and may be complex distributed networks. In addition, the current source's value will differ between applications and its connection may be GND referenced, power supply referenced or floating in a signal line path. Linear Technology strongly recommends that stability be tested in situ for any LT3092 application.

In LT3092 applications with long wires or PCB traces, the inductive reactance may cause instability. In some cases, adding series resistance to the input and output lines (as shown in Figure 2) may sufficiently dampen these possible high-Q lines and provide stability. The user must evaluate the required resistor values against the design's headroom constraints. In general, operation at low output current levels (< 5mA) automatically requires higher values of programming resistors and may provide the necessary damping without additional series impedance.

If the line impedances in series with the LT3092 are complex enough such that series damping resistors are not sufficient, a frequency compensation network may be necessary. Several options may be considered.

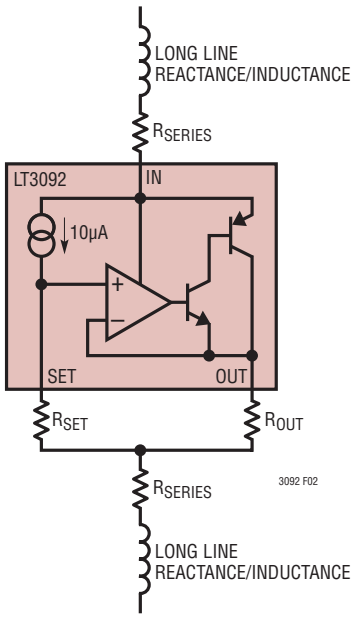


Figure 2. Adding Series Resistor Decouples and Dampens Long Line Reactances

APPLICATIONS INFORMATION

Figure 3 depicts the simplest frequency compensation network as a single capacitor connected across the two terminals of the current source. In this case, either a capacitor with a value less than 1000pF, or greater than 1µF (ESR < 0.5Ω), may stabilize the circuit. Some applications may use the small value capacitor to stand off DC voltage, but allow the transfer of data down a signal line.

For some applications, this capacitance range may be unacceptable or present a design constraint. One circuit example typifying this is an "intrinsically-safe" circuit in which an overload or fault condition potentially allows the capacitor's stored energy to create a spark or arc. For applications in which a single capacitor is unacceptable, Figure 3 alternately shows a series RC network connected across the two terminals of the current source. This network has two benefits. First, it limits the potential discharge current of the capacitor under a fault condition, preventing sparks or arcs. Second, it bridges the gap between the upper bound of 1000pF for small capacitors to the lower bound of 1µF for large capacitors such that almost any value capacitor can be used. This allows the user greater flexibility for frequency compensating the loop and fine tuning the RC network for complex impedance networks. In many instances, a series RC network is the best solution for stabilizing the application circuit. Typical resistor values will range from 100Ω to about 5k, especially for capacitor values in between 1000pF and 1µF. Once again, Linear Technology strongly recommends testing stability in situ for any LT3092 application across all operating conditions, especially ones that present complex impedance networks at the input and output of the current source.

If an application refers the bottom of the LT3092 current source to GND, it may be necessary to bypass the top of the current source with a capacitor to GND. In some cases, this capacitor may already exist and no additional capacitance is required. For example, if the LT3092 was used as a variable current source on the output of a power supply, the output bypass capacitance would suffice to provide LT3092 stability. Other applications may require the addition of a bypass capacitor. Once again, the same capacitor value requirements previously mentioned apply in that an upper bound of 1000pF exists for small values of capacitance, and a lower bound of 1µF (ESR < 0.5Ω) exists for large value capacitors. A series RC network may also be used as necessary, and depends on the application requirements.

In some extreme cases, capacitors or series RC networks may be required on both the LT3092's input and output to stabilize the circuit. Figure 4 depicts a general application using input and output capacitor networks, rather than an input-to-output capacitor. As the input of the current source tends to be high impedance, placing a capacitor on the input does not have the same effect as placing a

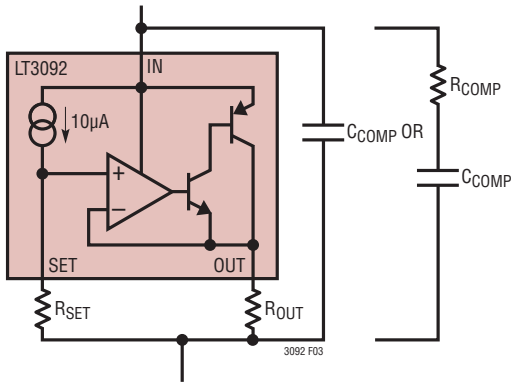


Figure 3. Compensation From Input to Output of Current Source Provides Stability

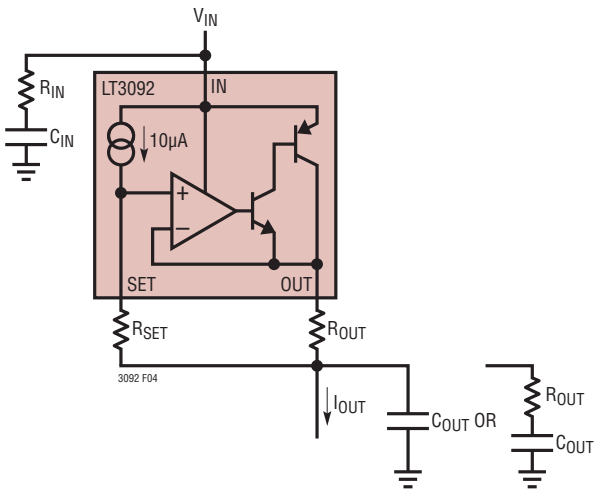


Figure 4. Input and/or Output Capacitors May Be Used for Compensation

APPLICATIONS INFORMATION

capacitor on the lower impedance output, and the same restrictions do not apply. Capacitors in the range of 0.1µF to 1µF usually provide sufficient bypassing on the input, and the value of input capacitance may be increased without limit.

If an application uses GND referred capacitors on the input or output (particularly the input), pay attention to the length of the lines powering and returning ground from the circuit. In the case where long power supply and return lines are coupled with low ESR input capacitors, application-specific voltage spikes, oscillations and reliability concerns may be seen. This is not an issue with LT3092 stability, but rather the low ESR capacitor forming a high-Q resonant tank circuit with the inductance of the input wires. Adding series resistance with the input of the LT3092, or with the input capacitor, often solves this. Resistor values of 0.1Ω to 1Ω are often sufficient to dampen this resonance.

Give extra consideration to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients as shown in Figures 5 and 6. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress. In a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients.

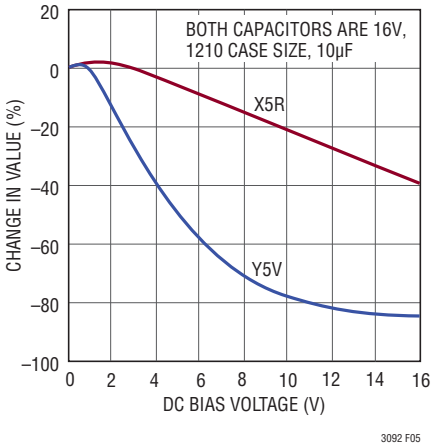


Figure 5. Ceramic Capacitor DC Bias Characteristics

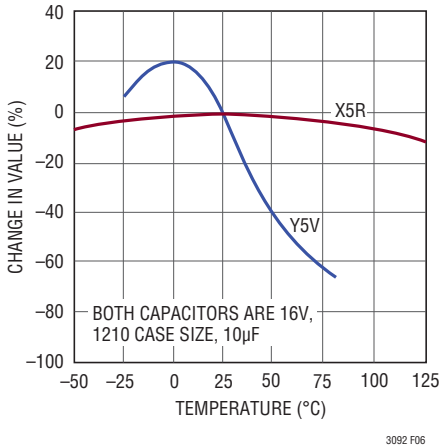


Figure 6. Ceramic Capacitor Temperature Characteristics

APPLICATIONS INFORMATION

Quieting the Noise

When a reduction in the noise of the current source is desired, a small capacitor can be placed across R_{SET} (C_{SET} in Figure 7). Normally, the 10µA reference current source generates noise current levels of 2.7pA/$\sqrt{Hz}$ (0.7nA$_{RMS}$ over the 10Hz to 100kHz bandwidth). The SET pin resistor generates a spot noise equal to $i_n = \sqrt{4kT/R}$ (k = Boltzmann's constant, $1.38 \cdot 10^{-23}$J/°K, and T is absolute temperature) which is RMS-summed with the noise generated by the 10µA reference current source. Placing a C_{SET} capacitor across R_{SET} (as shown in Figure 7) bypasses this noise current. Note that this noise reduction capacitor increases start-up time as a factor of the time constant formed by $R_{SET} \cdot C_{SET}$. When using a capacitor across the SET pin resistor, the external pole introduced usually requires compensation to maintain stability. See the Stability and Frequency Compensation section for detailed descriptions on compensating LT3092 circuits.

A curve in the Typical Performance Characteristics section depicts noise spectral density for the reference current over a 10Hz to 100kHz bandwidth.

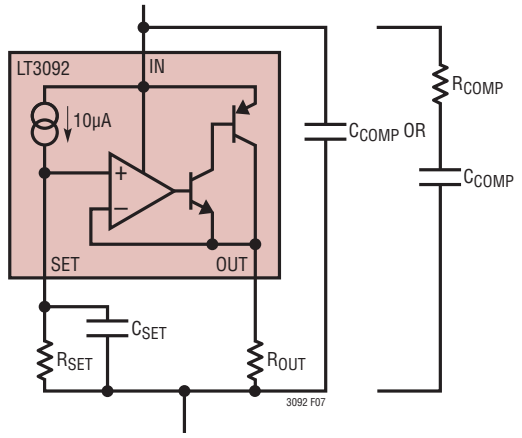


Figure 7. Adding C_{SET} Lowers Current Noise

Paralleling Devices

Obtain higher output current by paralleling multiple LT3092's together. The simplest application is to run two current sources side by side and tie their inputs together and their outputs together, as shown in Figure 8. This allows the sum of the current sources to deliver more output current than a single device is capable of delivering.

Another method of paralleling devices requires fewer components and helps to share power between devices. Tie the individual SET pins together and tie the individual IN pins together. Connect the outputs in common using small pieces of PC trace as ballast resistors to promote equal current sharing. PC trace resistance in milliohms/inch is shown in Table 1. Ballasting requires only a tiny area on the PCB.

Table 1. PC Board Trace Resistance

WEIGHT (oz)	10mil WIDTH	20mil WIDTH
1	54.3	27.1
2	27.1	13.6

Trace resistance is measured in mΩ/in

The worst-case room temperature offset, only ±2mV between the SET pin and the OUT pin, allows the use of very small ballast resistors.

As shown in Figure 9, each LT3092 has a small 40mΩ ballast resistor, which at full output current gives better than 80% equalized sharing of the current. The external resistance of 40mΩ (20mΩ for the two devices in parallel) only adds about 8mV of output voltage compliance at an output of 0.4A. Of course, paralleling more than two LT3092's yields even higher output current. Spreading the device on the PC board also spreads the heat. Series input resistors can further spread the heat if the input-to-output difference is high.

Thermal Considerations

The LT3092's internal power and thermal limiting circuitry protects itself under overload conditions. For continuous normal load conditions, do not exceed the 125°C maximum junction temperature. Carefully consider all sources of thermal resistance from junction-to-ambient. This includes (but is not limited to) junction-to-case, case-to-heat sink

APPLICATIONS INFORMATION

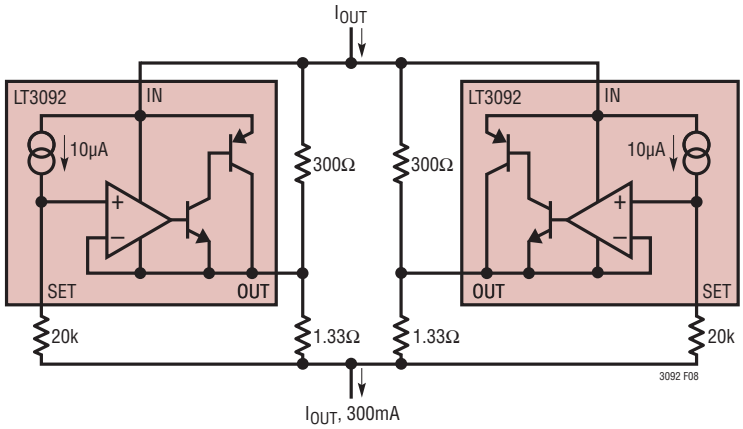


Figure 8. Connect Two LT3092s for Higher Current

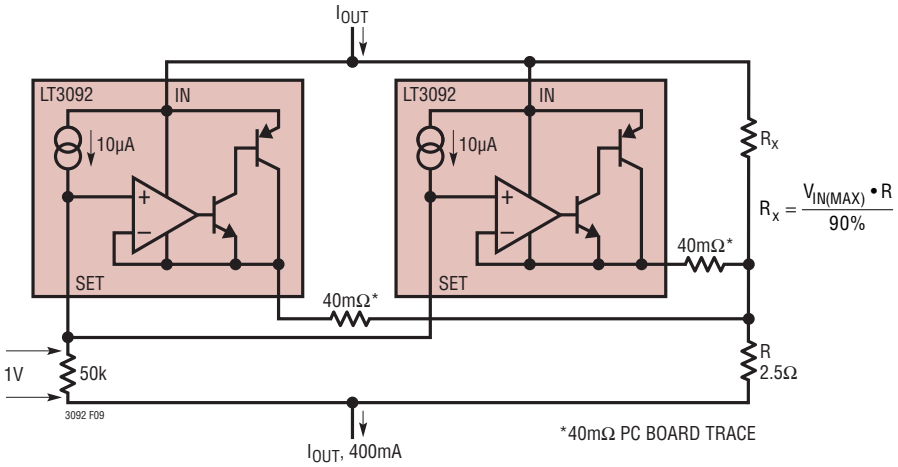


Figure 9. Parallel Devices

interface, heat sink resistance or circuit board-to-ambient as the application dictates. Consider all additional, adjacent heat generating sources in proximity on the PCB.

Surface mount packages provide the necessary heat sinking by using the heat spreading capabilities of the PC board, copper traces and planes. Surface mount heat sinks, plated through-holes and solder filled vias can also spread the heat generated by power devices.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly, or the bottom of the pin most directly, in the heat path. This is the lowest thermal resistance path for heat flow. Only proper device mounting ensures the best possible thermal flow from this area of the package to the heat sinking material.

Note that the Exposed Pad of the DFN package and the Tab of the SOT-223 package are electrically connected to the output (V_{OUT}).

The following tables list thermal resistance as a function of copper areas in a fixed board size. All measurements were taken in still air on a four-layer FR-4 board with 1oz solid internal planes and 2oz external trace planes with a total finished board thickness of 1.6mm.

PCB layers, copper weight, board layout and thermal vias affect the resultant thermal resistance. Please reference JEDEC standard JESD51-7 for further information on high thermal conductivity test boards. Achieving low thermal resistance necessitates attention to detail and careful layout.

APPLICATIONS INFORMATION

Demo circuit 1531A's board layout using multiple inner V_{OUT} planes and multiple thermal vias achieves 28°C/W performance for the DFN package.

Table 2. DD Package, 8-Lead DFN

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	25°C/W
1000mm^2	2500mm^2	2500mm^2	25°C/W
225mm^2	2500mm^2	2500mm^2	28°C/W
100mm^2	2500mm^2	2500mm^2	32°C/W

*Device is mounted on topside

Table 3. TS8 Package, 8-Lead SOT-23

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	54°C/W
1000mm^2	2500mm^2	2500mm^2	54°C/W
225mm^2	2500mm^2	2500mm^2	57°C/W
100mm^2	2500mm^2	2500mm^2	63°C/W

*Device is mounted on topside

Table 4. ST Package, 3-Lead SOT-223

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500mm^2	2500mm^2	2500mm^2	20°C/W
1000mm^2	2500mm^2	2500mm^2	20°C/W
225mm^2	2500mm^2	2500mm^2	24°C/W
100mm^2	2500mm^2	2500mm^2	29°C/W

*Device is mounted on topside

For further information on thermal resistance and using thermal information, refer to JEDEC standard JESD51, notably JESD51-12.

Calculating Junction Temperature

Example: Given an industrial factory application with an input voltage of 15V ±10%, an output voltage of 12V ±5%, an output current of 200mA and a maximum ambient temperature of 50°C, what would be the maximum junction temperature for a DFN package?

The total circuit power equals:

$$P_{TOTAL} = (V_{IN} - V_{OUT})(I_{OUT})$$

The SET pin current is negligible and can be ignored.

$V_{IN(MAX\ CONTINUOUS)}$ = 16.5 (15V + 10%)

$V_{OUT(MIN\ CONTINUOUS)}$ = 11.4V (12V – 5%)

I_{OUT} = 200mA

Power dissipation under these conditions equals:

$$P_{TOTAL} = (16.5 - 11.4V)(200mA) = 1.02W$$

Junction temperature equals:

$$T_J = T_A + P_{TOTAL} \bullet \theta_{JA}$$

$$T_J = 50°C + (1.02W \bullet 30°C/W) = 80.6°C$$

In this example, the junction temperature is below the maximum rating, ensuring reliable operation.

Protection Features

The LT3092 incorporates several protection features ideal for battery-powered circuits, among other applications. In addition to normal circuit protection features such as current limiting and thermal limiting, the LT3092 protects itself against reverse-input voltages, reverse-output voltages, and reverse OUT-to-SET pin voltages.

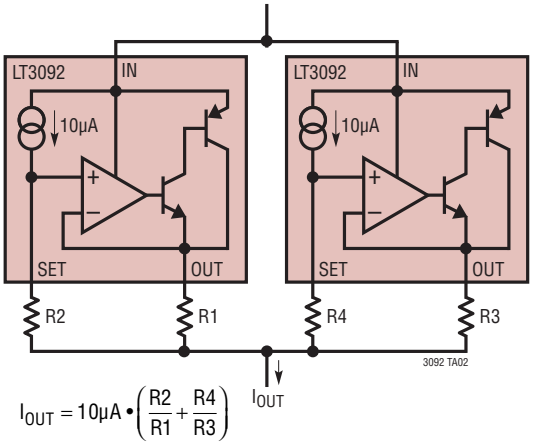
Current limit protection and thermal overload protection protect the IC against output current overload conditions. For normal operation, do not exceed a junction temperature of 125°C. The thermal shutdown circuit's typical temperature threshold is 165°C and has about 5°C of hysteresis.

The LT3092's IN pin withstands ±40V voltages with respect to the SET and OUT pins. Reverse-current flow, if OUT is greater than IN, is less than 1mA (typically under 100µA), protecting the LT3092 and sensitive loads.

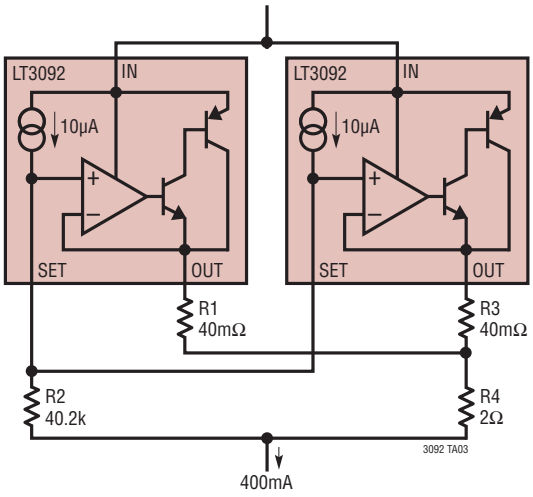
Clamping diodes and 1k limiting resistors protect the LT3092's SET pin relative to the OUT pin voltage. These protection components typically only carry current under transient overload conditions. These devices are sized to handle ±10V differential voltages and ±15mA crosspin current flow without concern.

TYPICAL APPLICATIONS

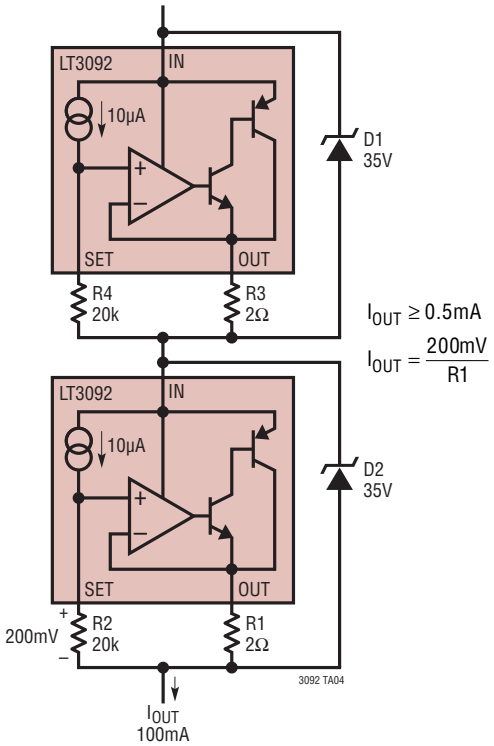
Paralleling Current Sources for Higher Current



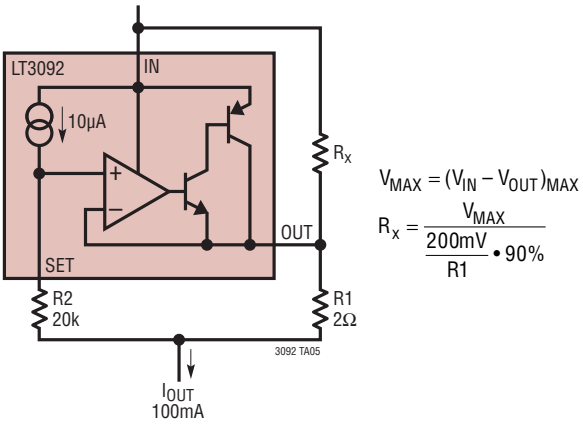
Paralleling LT3092s with Ballast Resistor



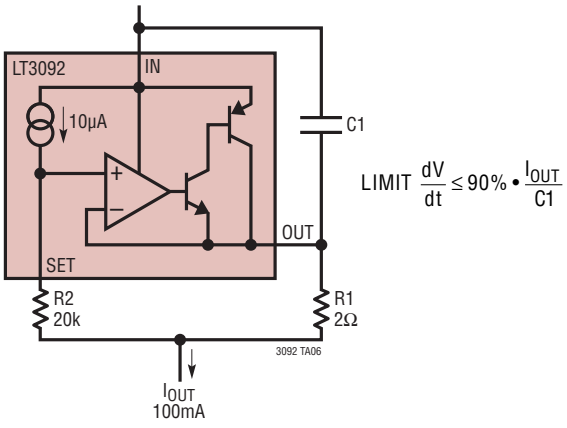
High Voltage Current Source



Decreasing Power Dissipation in LT3092 100mA Current Source

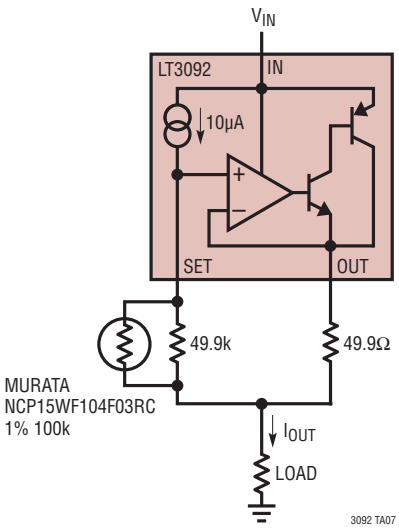


Capacitor Adds Stability, But Limits Slew Rate

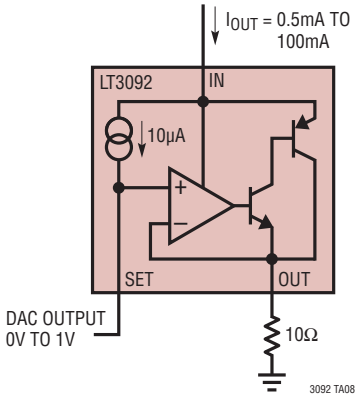


TYPICAL APPLICATIONS

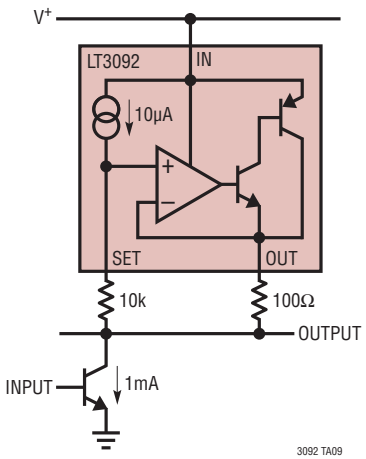
Remote Temperature Sensor



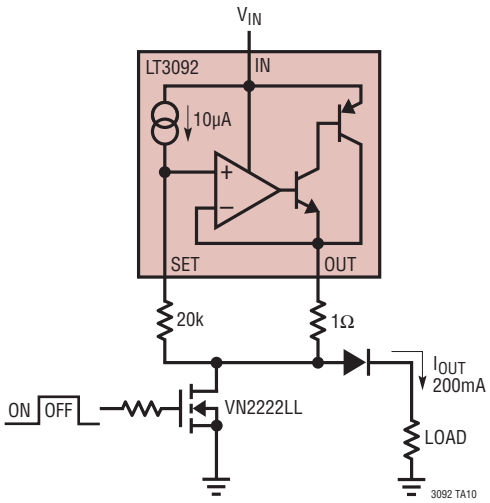
DAC Controlled Current Source



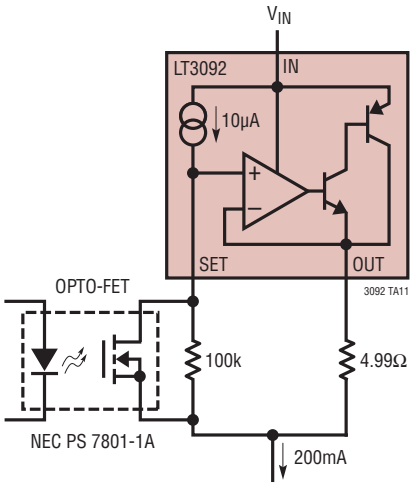
Active Load



Pulsed Current Source, Load to Ground

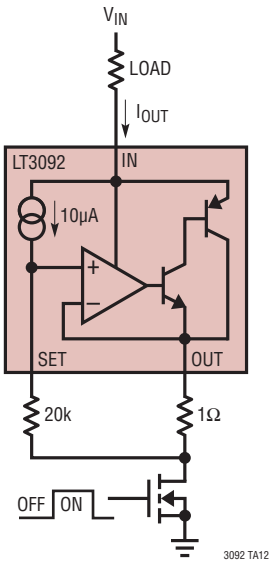


Fully Floating Current Source Switches From 200mA to Quiescent Current

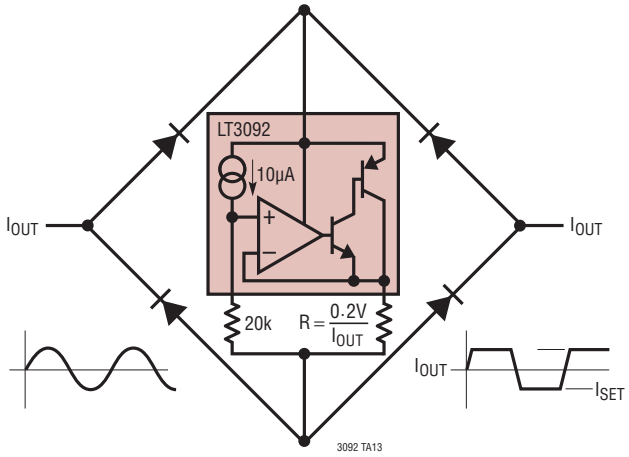


TYPICAL APPLICATIONS

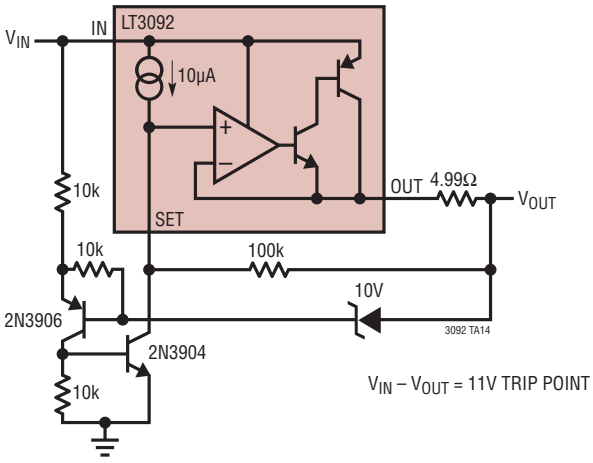
Pulsed Current Source, Load to V_{IN}



2-Terminal AC Current Limiter

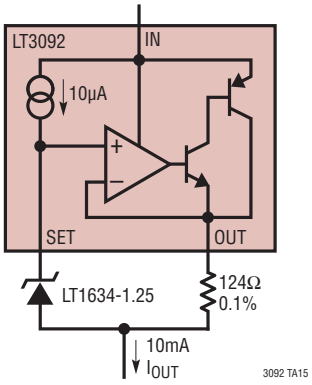


Voltage Clamp



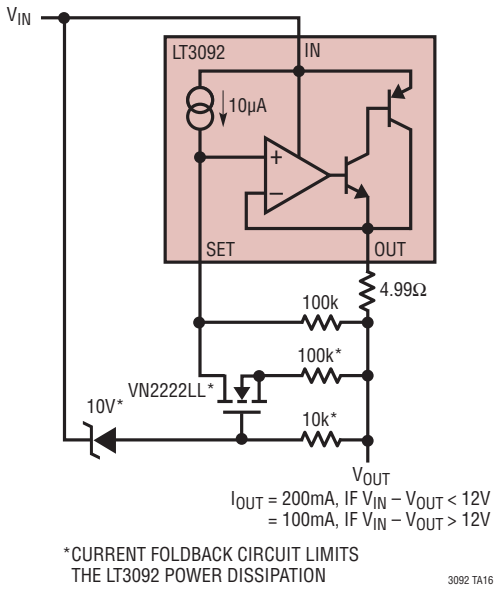
$V_{IN} - V_{OUT}$ = 11V TRIP POINT

High Accuracy Current Source

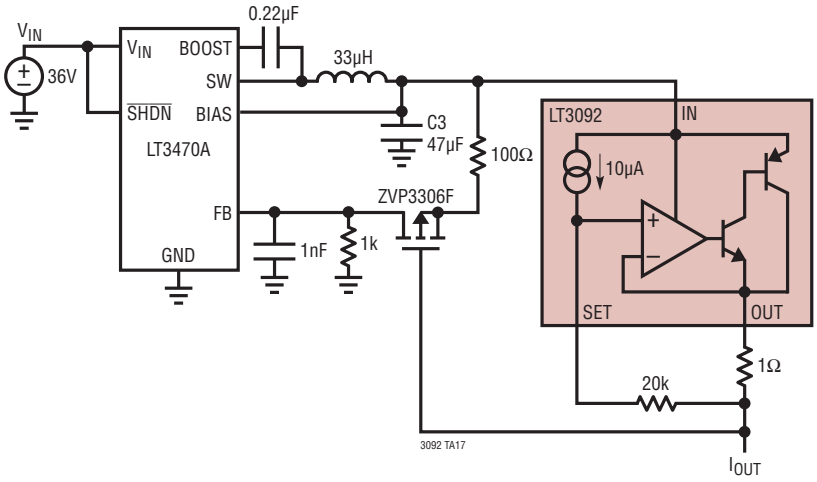


TYPICAL APPLICATIONS

2-Level Current Source

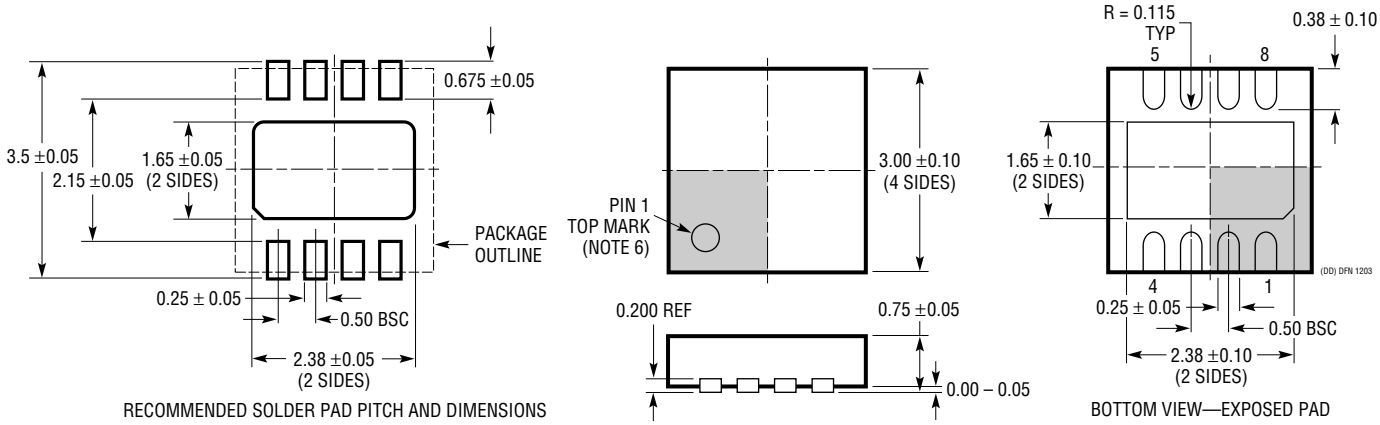


More Efficient Current Source



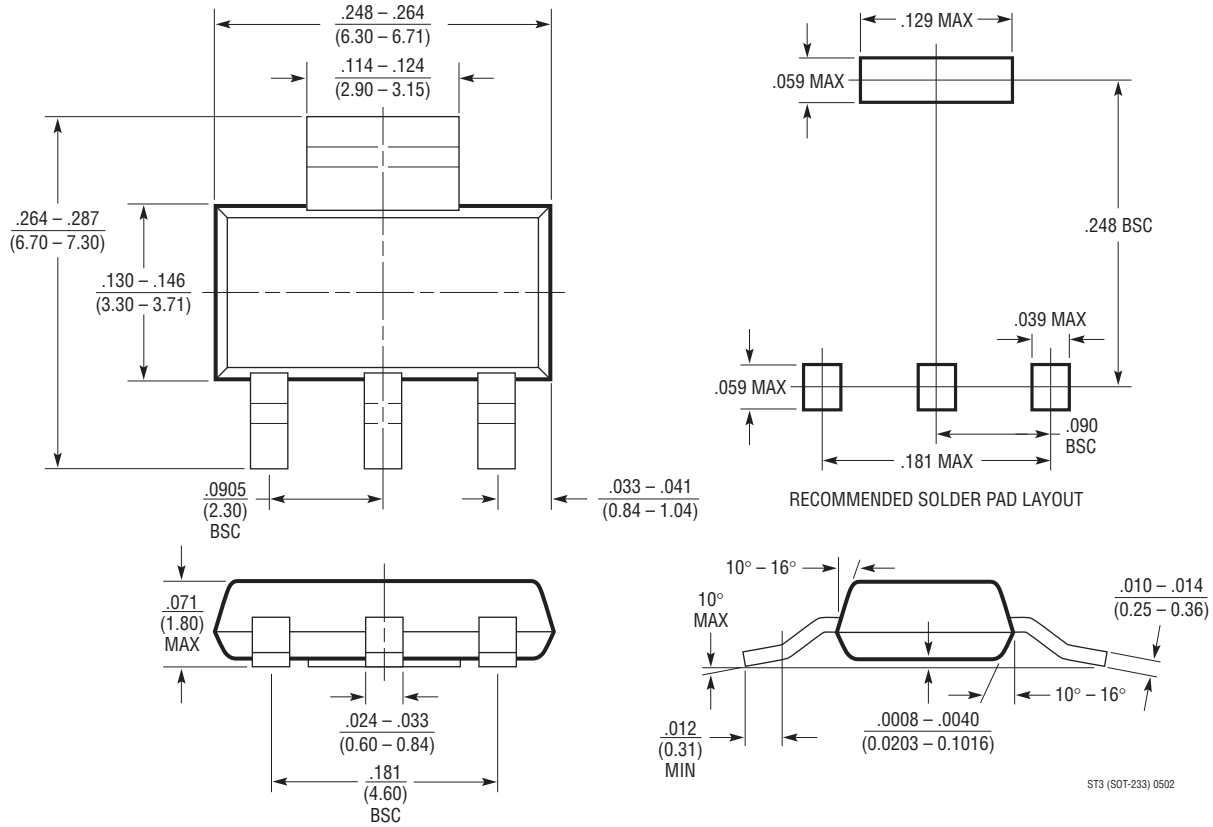
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



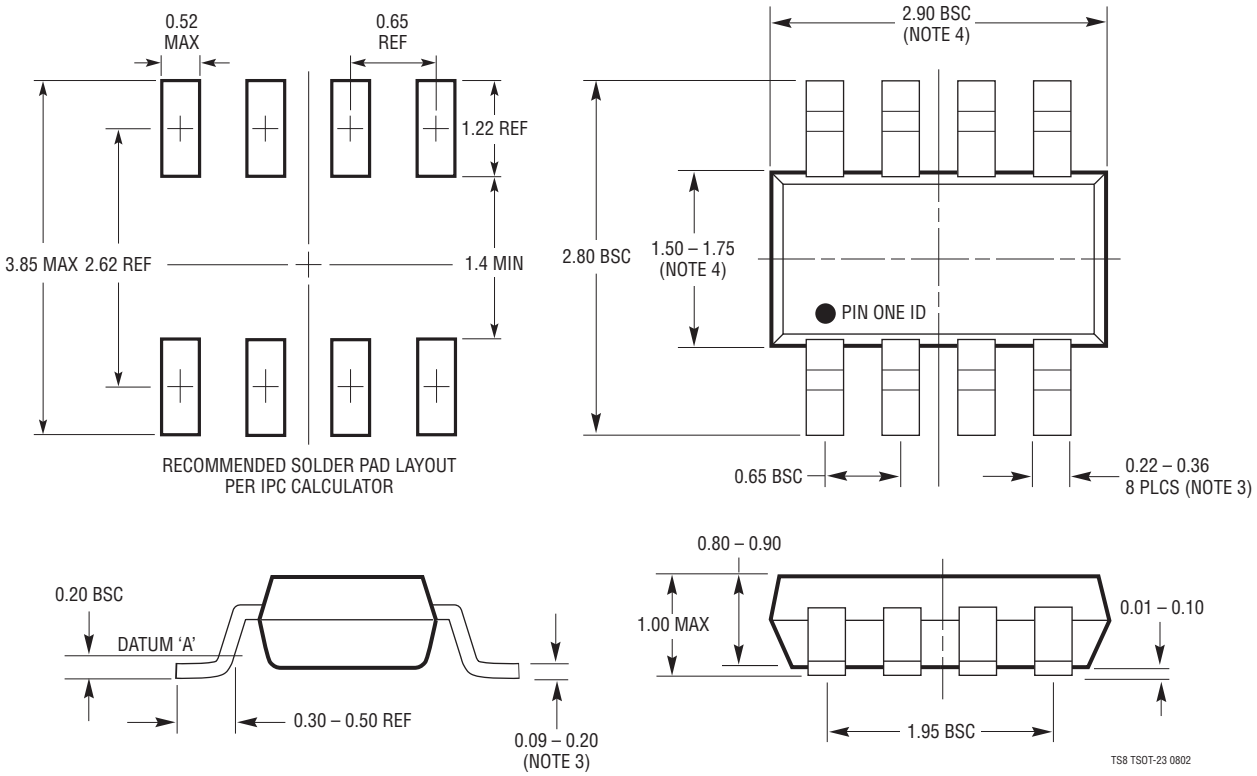
NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

ST Package
3-Lead Plastic SOT-223
(Reference LTC DWG # 05-08-1630)



PACKAGE DESCRIPTION

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



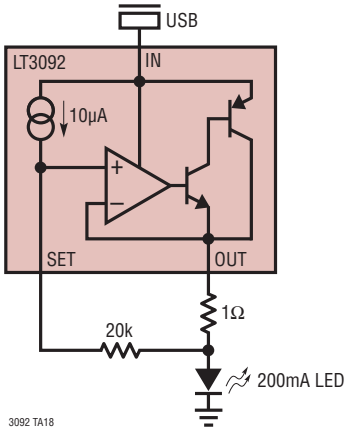
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY (Revision history begins at Rev B)

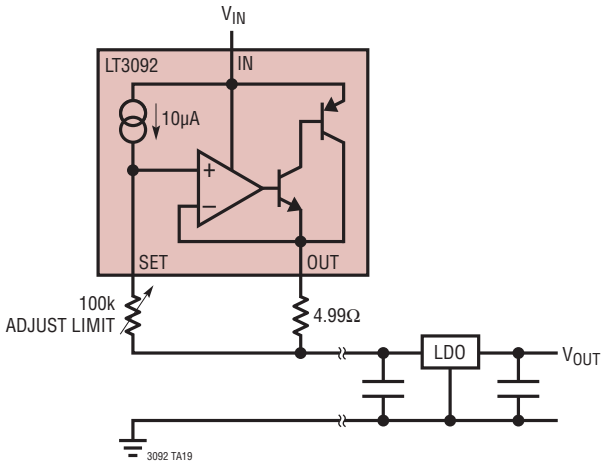
REV	DATE	DESCRIPTION	PAGE NUMBER
B	12/09	Update Order Information	2

TYPICAL APPLICATIONS

USB LED Driver



Current Limiter for Remote Power



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LDO		
LT1761	100mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, ThinSOT™ Package
LT1762	150mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 Package
LTC1844	150mA, Very Low Dropout LDO	80mV Dropout Voltage, Low Noise <30µV_{RMS}, V_{IN} = 1.6V to 6.5V, Stable with 1µF Output Capacitors, ThinSOT Package
LT1962	300mA, Low Noise LDO	270mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 Package
LT1964	200mA, Low Noise, Negative LDO	340mV Dropout Voltage, Low Noise 30µV_{RMS}, V_{IN} = –1.8V to –20V, ThinSOT Package
LT3008	20mA, 45V, 3µA I_Q Micropower LDO	280mV Dropout Voltage, Low I_Q: 3µA, V_{IN} = 2V to 45V, V_{OUT} = 0.6V to 39.5V; ThinSOT and 2mm × 2mm DFN-6 Packages
LT3009	20mA, 20V, 3µA I_Q Micropower LDO	280mV Dropout Voltage, Low I_Q: 3µA, V_{IN} = 1.6V to 20V, V_{OUT} = 0.6V to 19.5V; ThinSOT and SC70 Packages
LT3020	100mA, Low Voltage VLDO Linear Regulator	V_{IN}: 0.9V to 10V, V_{OUT}: 0.2V to 5V (Min), V_{DO} = 0.15V, I_Q = 120µA, Noise: <250µV_{RMS}, Stable with 2.2µF Ceramic Capacitors, DFN-8, MS8 Packages
LTC3025	300mA Micropower VLDO Linear Regulator	V_{IN} = 0.9V to 5.5V, Dropout Voltage: 45mV, Low Noise 80µV_{RMS}, Low I_Q: 54µA, 6-Lead 2mm × 2mm DFN Package
LTC3035	300mA VLDO Linear Regulator with Charge Pump Bias Generator	V_{IN} = 1.7V to 5.5V, V_{OUT}: 0.4V to 3.6V, Dropout Voltage: 45mV, I_Q: 100µA, 3mm × 2mm DFN-8
LT3080/ LT3080-1	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Caps, TO-220, SOT-223, MSOP-8 and 3mm × 3mm DFN-8 Packages; LT3080-1 Version Has Integrated Internal Ballast Resistor
LT3085	500mA, Parallelable, Low Noise, Low Dropout Linear Regulator	275mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-based Reference with 1-Resistor V_{OUT} Set; Directly Parallelable (No Op Amp Required), Stable with Ceramic Caps, MSOP-8 and 2mm × 3mm DFN-6 Packages
Current Sense Amplifiers		
LT6106	Low Cost, 36V High Side Current Sense Amplifier	36V (44V Max) Current Sense, Dynamic Range of 2000:1, 106dB of PSRR
LT6107	High Temperature High Side Current Sense Amp in SOT-23	36V (44V Max) Current Sense, Dynamic Range of 2000:1, 106dB of PSRR, –55 to 150°C (MP-Grade)

ThinSOT is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 1209 REV B • PRINTED IN USA