

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4541B **MSI** Programmable timer

Product specification
File under Integrated Circuits, IC04

January 1995

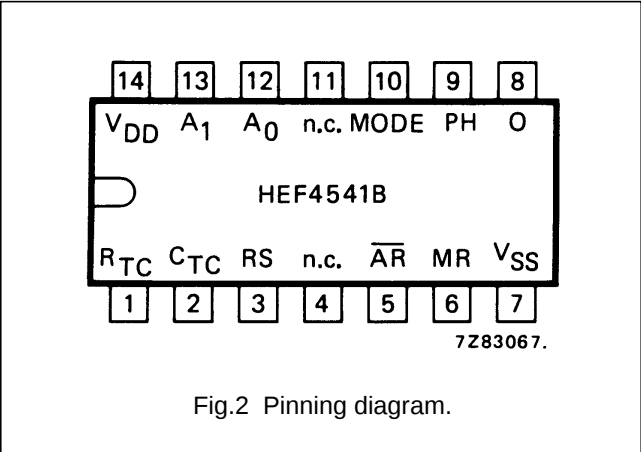
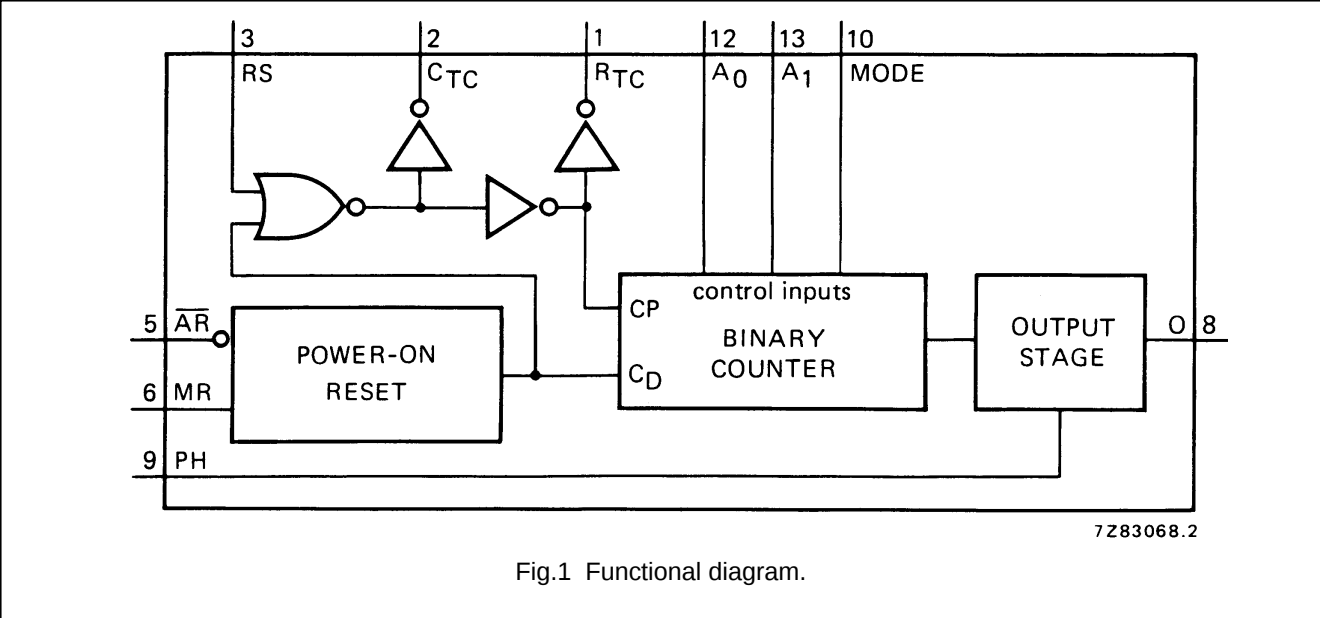
Programmable timer

HEF4541B
MSI

DESCRIPTION

The HEF4541B is a programmable timer which consists of a 16-stage binary counter, an integrated oscillator to be used with external timing components, an automatic power-on reset and output control logic. The frequency of the oscillator is determined by the external components R_T and C_T within the frequency range 1 Hz to 100 kHz. This oscillator may be replaced by an external clock signal at input RS, the timer advances on the positive-going transition of RS. A LOW on the auto reset input ($\overline{AR}$) and a LOW on the master reset input (MR) enables the internal power-on reset. A HIGH level at input MR resets the counter independent on all other inputs. Resetting

disables the oscillator to provide no active power dissipation. A HIGH at input $\overline{AR}$ turns off the power-on reset to provide a low quiescent power dissipation of the timer. The 16-stage counter divides the oscillator frequency by 2^8 , 2^{10} , 2^{13} or 2^{16} depending on the state of the address inputs (A_0 , A_1). The divided oscillator frequency is available at output O. The phase input (PH) features a complementary output signal. If the mode select input (MODE) is LOW or HIGH the timer can be used respectively as a single transition timer or 2^n frequency divider.

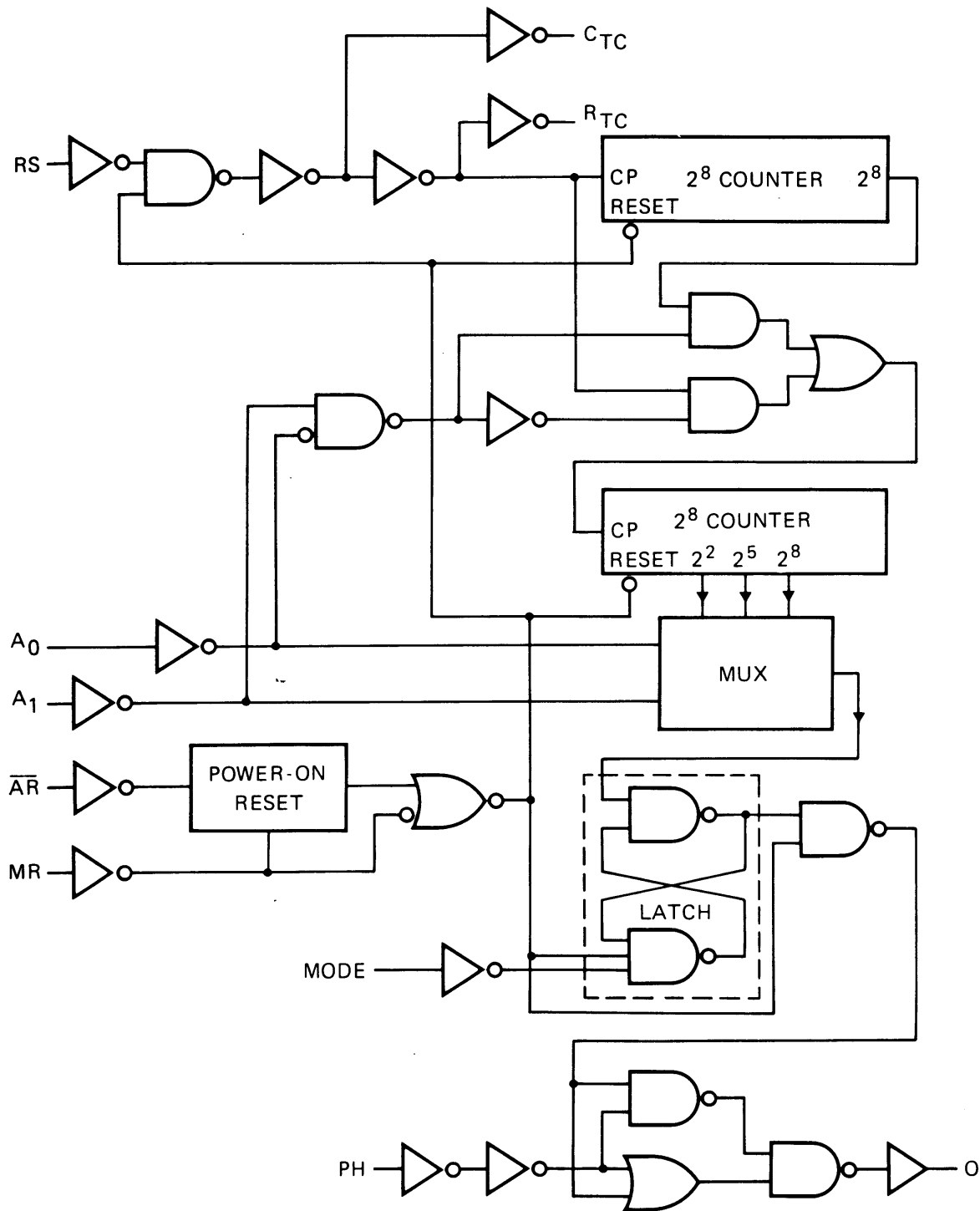


- HEF4541BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4541BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4541BT(D): 14-lead SO; plastic (SOT108-1)
- (): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI
See Family Specifications

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7Z83070.2

Fig.3 Logic diagram.

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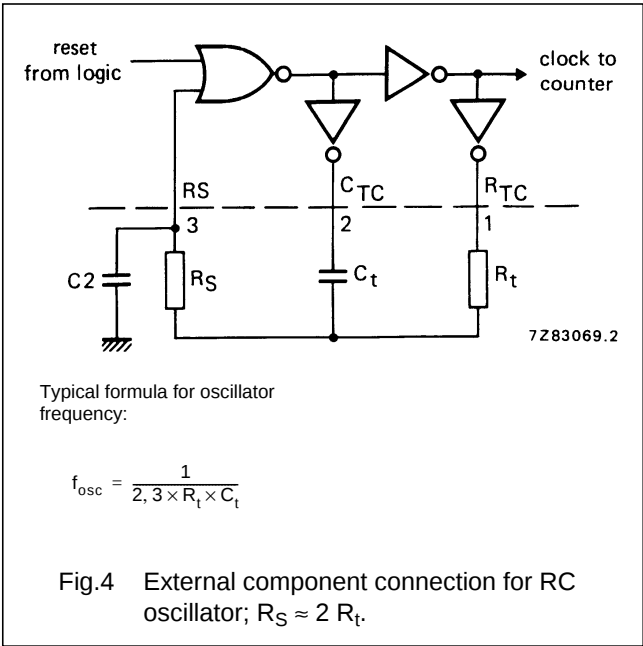
PINNING

A ₀ , A ₁	address inputs
MODE	mode select input
$\overline{\text{AR}}$	auto reset input
MR	master reset input
PH	phase input
R _{TC}	external resistor connection (R _t)
C _{TC}	external capacitor connection (C _t)
RS	external resistor connection (R _S) or external clock input

FREQUENCY SELECTION TABLE

A ₀	A ₁	NUMBER OF COUNTER STAGES n	$\frac{f_{\text{osc}}}{f_{\text{out}}} = 2^n$
L	L	13	8 192
L	H	10	1 024
H	L	8	256
H	H	16	65 536

RC oscillator



FUNCTION TABLE

INPUTS				MODE
$\overline{\text{AR}}$	MR	PH	MODE	
H	L	X	X	auto reset disabled
L	L	X	X	auto reset enabled ⁽¹⁾
X	H	X	X	master reset active
X	L	X	H	normal operation selected
X	L	X	L	division to output
X	L	L	X	single-cycle mode ⁽²⁾
X	L	L	X	output initially LOW, after reset
X	L	H	X	output initially HIGH, after reset

Notes

- For correct power-on reset, the supply voltage should be above 8.5 V. For $V_{\text{DD}} < 8.5 \text{ V}$, disable the autoreset and connect $\overline{\text{AR}}$ to V_{DD} .
- The timer is initialized on a reset pulse and the output changes state after 2^{n-1} counts and remains in that state (latched). Reset of this latch is obtained by master reset or by a LOW to HIGH transition on the MODE input.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

Timing component limitations

The oscillator frequency is mainly determined by $R_t C_t$, provided $R_t \ll R_S$ and $R_S C_2 \ll R_t C_t$. The function of R_S is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C_2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the LOCMOS 'ON' resistance in series with it, which typically is 500 Ω at $V_{\text{DD}} = 5 \text{ V}$, 300 Ω at $V_{\text{DD}} = 10 \text{ V}$ and 200 Ω at $V_{\text{DD}} = 15 \text{ V}$.

The recommended values for these components to maintain agreement with the typical oscillation formula are:
 $C_t \geq 100 \text{ pF}$, up to any typical value,
 $10 \text{ k}\Omega \leq R_t \leq 1 \text{ M}\Omega$.

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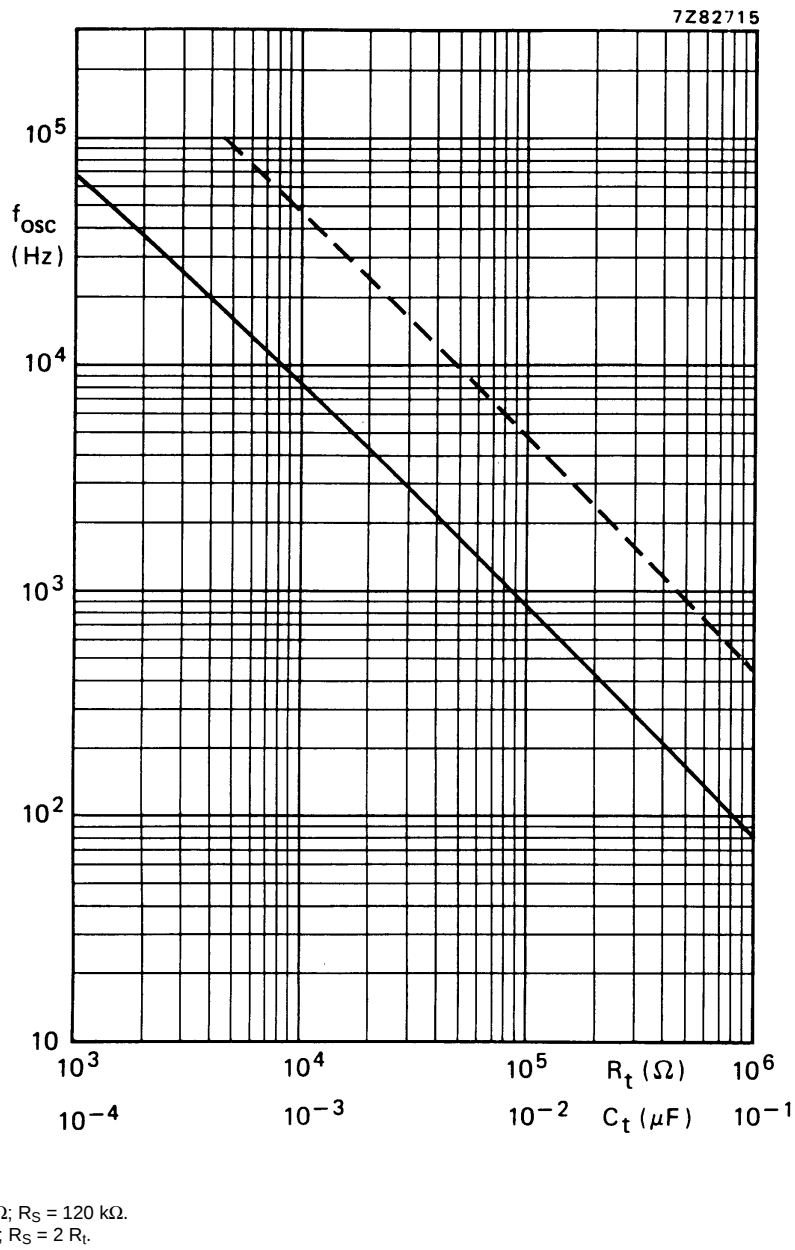


Fig.5 RC oscillator frequency as a function of R_t and C_t at $V_{DD} = 5\text{ to }15\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$.

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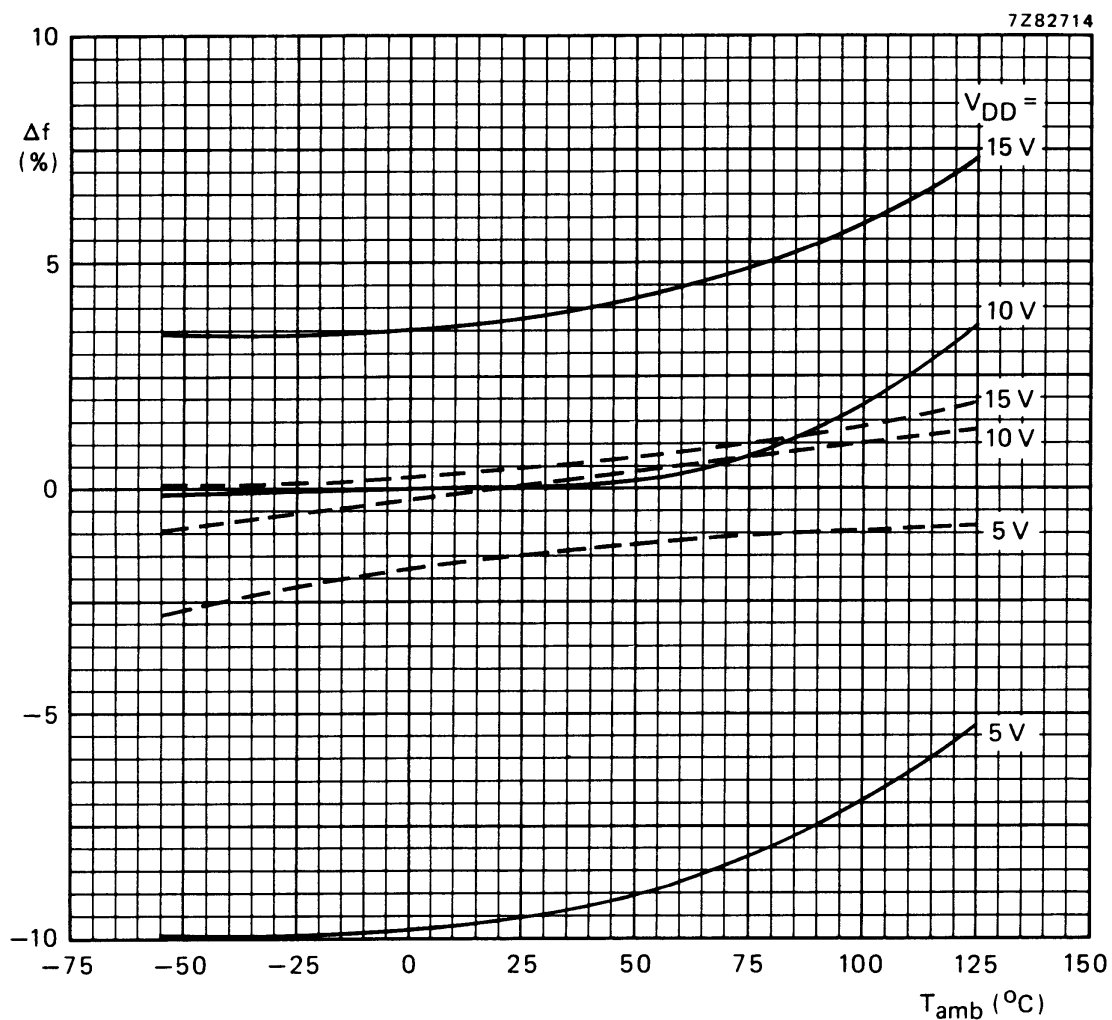
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Fig.6 Frequency deviation (Δf) as a function of ambient temperature; referenced at : f_{osc} at $T_{amb} = 25\text{ }^{\circ}\text{C}$ and $V_{DD} = 10\text{ V}$.

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DC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$

	V_{DD} V	V_{OL} V	V_{OH} V	SYMBOL	$T_{amb} (^{\circ}\text{C})$					
					-40		+ 25		+ 85	
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.
Supply current	5			I_D	–	80	–	20	80	– 230 μA
power-on reset	10				–	750	–	250	600	– 700 μA
enabled (note)	15				–	1600	–	500	1300	– 1500 μA
Supply voltage for automatic reset initialization (note)				V_{DD}	–	–	8,5	5	–	– – V
Output current HIGH; C_{TC} , R_{TC}	5		4,6	$-I_{OH}$	0,5	–	0,4	–	–	0,3 – mA
	10		9,5		1,4	–	1,2	–	–	0,95 – mA
	15		13,5		4,8	–	4,0	–	–	3,2 – mA
	5		2,5	$-I_{OH}$	1,4	–	1,2	–	–	0,95 – mA
Output current LOW; C_{TC} , R_{TC}	5	0,4		I_{OL}	0,33	–	0,27	–	–	0,20 – mA
	10	0,5			1,00	–	0,85	–	–	0,68 – mA
	15	1,5			3,20	–	2,70	–	–	2,30 – mA

Note

- All inputs at 0 V or V_{DD} ; except input $\overline{AR}$ = input MR = 0 V (power-on reset active).

AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	TYPICAL FORMULA FOR P (μW) ⁽¹⁾			
Dynamic power dissipation per package (P)	5	1 300	$f_i + f_o C_L V_{DD}^2$		
	10	5 300	$f_i + f_o C_L V_{DD}^2$		
	15	12 000	$f_i + f_o C_L V_{DD}^2$		
Total power dissipation when using the on-chip oscillator (P)	5	1 300	$f_{osc} + f_o C_L V_{DD}^2$	$+ 2C_t V_{DD}^2 f_{osc}$	$+ 10 V_{DD}$
	10	5 300	$f_{osc} + f_o C_L V_{DD}^2$	$+ 2C_t V_{DD}^2 f_{osc}$	$+ 100 V_{DD}$
	15	12 000	$f_{osc} + f_o C_L V_{DD}^2$	$+ 2C_t V_{DD}^2 f_{osc}$	$+ 400 V_{DD}$

Notes

- where:

 f_i = input frequency (MHz) f_o = output frequency (MHz) C_L = load capacitance (pF) V_{DD} = supply voltage (V) C_t = timing capacitance (pF) f_{osc} = oscillator frequency (MHz)

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AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays RS $\rightarrow$ O						
2 ⁸ selected	5	t_{PHL} ; t_{PLH}		375	750 ns	348 ns + (0,55 ns/pF) C_L
HIGH to LOW	10			150	300 ns	139 ns + (0,23 ns/pF) C_L
LOW to HIGH	15			110	220 ns	102 ns + (0,16 ns/pF) C_L
RS $\rightarrow$ O						
2 ¹⁰ selected	5	t_{PHL} ; t_{PLH}		425	850 ns	398 ns + (0,55 ns/pF) C_L
HIGH to LOW	10			165	330 ns	154 ns + (0,23 ns/pF) C_L
LOW to HIGH	15			120	240 ns	112 ns + (0,16 ns/pF) C_L
RS $\rightarrow$ O						
2 ¹³ selected	5	t_{PHL} ; t_{PLH}		510	1020 ns	483 ns + (0,55 ns/pF) C_L
HIGH to LOW	10			190	380 ns	179 ns + (0,23 ns/pF) C_L
LOW to HIGH	15			135	270 ns	127 ns + (0,16 ns/pF) C_L
RS $\rightarrow$ O						
2 ¹⁶ selected	5	t_{PHL} ; t_{PLH}		575	1150 ns	548 ns + (0,55 ns/pF) C_L
HIGH to LOW	10			210	420 ns	199 ns + (0,23 ns/pF) C_L
LOW to HIGH	15			150	300 ns	142 ns + (0,16 ns/pF) C_L
Minimum clock pulse width; LOW	5	t_{WRSL}	60	30	ns	
	10		30	15	ns	
	15		24	12	ns	
Minimum reset pulse width; HIGH	5	t_{WMRH}	60	30	ns	
	10		30	15	ns	
	15		24	12	ns	
Maximum clock pulse frequency	5	f_{max}	8	16	MHz	
	10		15	30	MHz	
	15		18	36	MHz	
Oscillator frequency	5	f_{osc}		90	kHz	$R_t = 5\text{ k}\Omega$
	10			90	kHz	$C_t = 1\text{ nF}$
	15			90	kHz	$R_S = 10\text{ k}\Omega$
Oscillator frequency	5	f_{osc}		8	kHz	$R_t = 56\text{ k}\Omega$
	10			8	kHz	$C_t = 1\text{ nF}$
	15			8	kHz	$R_S = 120\text{ k}\Omega$