

NCS37000

Ground Fault Circuit Interrupter (GFCI)

Description

The NCS37000 is a fully UL943 compliant signal processor for GFCI applications. The device integrates a flexible power supply (including both shunt and LDO regulators), differential fault, and grounded-neutral detection circuits. Proprietary impedance measurement and signal processing techniques are used to minimize the number of external components and improve performance. The device also includes a specialized DSP controller that offers best in class immunity to nuisance loads without the need for external analog filters.

Features

- 6.0 – 12 Volt Operation (120 – 480 V AC mains with the appropriate series impedance)
- –40 to 85°C
- Very Low Power Consumption: <5 mW @ 5 V
- 16 Pin QFN Package or 20 Pin TSSOP Package
- Single Current Transformer (CT) Detection of both Differential and Grounded-Neutral Faults
- Self Syncing Internal Oscillator Adjusts to AC Mains Frequency to Guarantee Full Resolution on 50 and 60 Hz Distribution Systems
- Optimized Solenoid Deployment (coil is not energized near the AC mains zero crossings)
- Randomized Testing Sequence to Minimize Noise and Potential Interactions on the AC Mains
- >5 mA SCR Driver for use with High Igt SCR's for Improved Noise Immunity
- Superior Immunity to Nuisance Loads/Noise (up to 10 A) without Loss of Detection Capability or CT Saturation
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Load Panel GFCI Breakers
- GFCI Receptacles
- In-line GFCI Circuits (power cords)

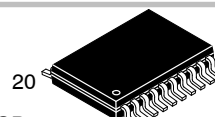


ON Semiconductor®

<http://onsemi.com>

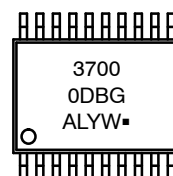
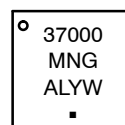


QFN16
MN SUFFIX
CASE 485G



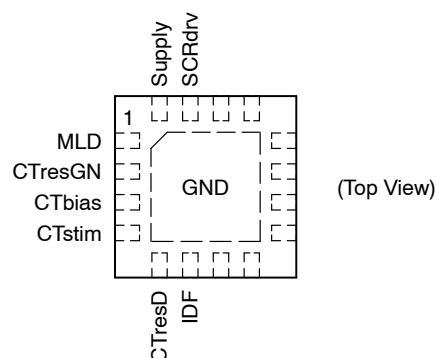
TSSOP-20
DA SUFFIX
CASE 948E

MARKING DIAGRAMS



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCS37000MNTWG	QFN16	2500/Tape & Reel
NCS37000MNG	(Pb-Free)	120 Units / Tube
NCS37000DBRG	TSSOP20	2500/Tape & Reel
NCS37000DBG	(Pb-Free)	74 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCS37000

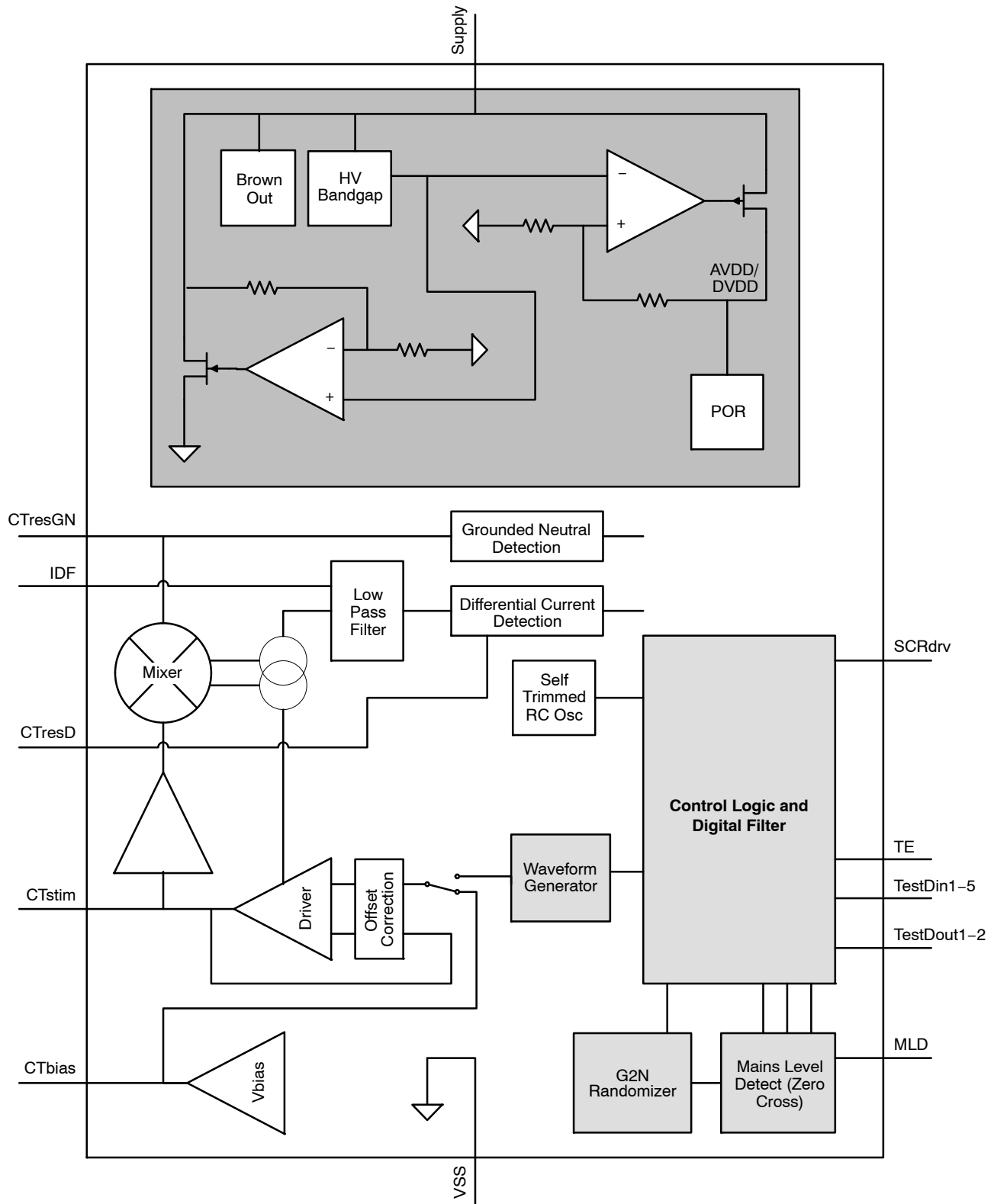


Figure 1. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION – QFN

Pin #	Name	Pad Description
0	Ground	QFN center slug
1	MLD	Mains Level Detect (Zero Cross)
2	CTresGN	Determines IV converter gain for detection threshold / matched to CT turns ratio (Ground-Neutral)
3	CTbias	Direct connection to the CT
4	CTstim	Direct connection to the CT
5	CTresD	Determines IV converter gain for detection threshold / matched to CT turns ratio (Differential Current)
6	IDF	Front end noise filter capacitor
7	NC	Tie to Ground or leave floating
8	NC	Float
9	NC	Tie to Ground or leave floating
10	NC	Tie to Ground or leave floating
11	NC	Tie to Ground or leave floating
12	NC	Tie to Ground or leave floating
13	NC	Float
14	NC	Float
15	SCRdrv	Used to trigger the solenoid at a fault detection
16	Supply	Power supply

Table 2. PIN FUNCTION DESCRIPTION – TSSOP

Pin #	Name	Pad Description
1	CTstim	Differential and ground to neutral stimulus point for the current transformer
2	Ground	Ground connection for IC
3	CTresD	Determines IV converter gain for detection threshold / matched to CT turns ratio (Differential Current)
4	IDF	Determines corner frequency of the differential current path filter
5	GFtest	Output to induce external differential current
6	NC	Tie to Ground or leave floating
7	NC	Float
8	NC	Tie to Ground or leave floating
9	NC	Tie to Ground or leave floating
10	NC	Tie to Ground or leave floating
11	Ground	Ground connection for IC
12	NC	Float
13	NC	Float
14	SCRdrv	Used to trigger the solenoid at a fault detection
15	DVDD	Internal digital 5 V regulated supply
16	AVDD	Internal analog 5 V regulated supply
17	Supply	12 V shunt regulated power supply
18	MLD	Mains Level Detect (Zero Cross) and AM slope detect (for oscillator sync/trim and AM init)
19	CTresGN	Determines IV converter gain for detection threshold / matched to CT turns ratio (Ground-Neutral)
20	CTbias	External 2 V bias for the current transformer

Table 3. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	V _S	6.0 to 12 V	V
Input Voltage Range (Note 1)	V _{in}	–0.3 to 6.0	V
Output Voltage Range	V _{out}	–0.3 to 6.0 V or (V _{in} + 0.3), whichever is lower	V
Maximum Junction Temperature	T _{J(max)}	140	°C
Storage Temperature Range	T _{STG}	–65 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD _{HBM}	2	kV
ESD Capability, Machine Model (Note 2)	ESD _{MM}	200	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb–Free Versions (Note 3)	T _{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
 ESD Human Body Model tested per AEC–Q100–002 (EIA/JESD22–A114)
 ESD Machine Model tested per AEC–Q100–003 (EIA/JESD22–A115)
 Latchup Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 4. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, QFN16, 3x3.3 mm (Note 4) Thermal Resistance, Junction–to–Air (Note 5)	R _{θJA}	64	°C/W
Thermal Characteristics, TSOP–5 (Note 4) Thermal Resistance, Junction–to–Air (Note 5)	R _{θJA}	118.6	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 645 mm² (or 1 in²) of 1 oz copper thickness and FR4 PCB substrate.

Table 5. OPERATING RANGES (Note 6)

Parameter	Conditions	Min	Typ	Max	Units
Operating Temperature		–40		85	C
IDD in typical power state			2.0		mA
Stimulus Generator Frequency	Tri–tone	3.1		3.4	kHz
SCR Trigger Current				8.0	mA
SCR Trigger output voltage	With 5 V supply	4.5		5.5	V
Fault Current Sensitivity	Programmable with CTresD	4.6	4.8	5.0	mA
Ground Fault Response Time	5 – 20 mA		150		ms
Ground Fault Response Time	20 – 40 mA		75		ms
Ground Fault Response Time	>40 mA		25		ms
Saturation Fault Response Time	>300 mA		1.4		ms
CT Turns Ratio		200		300	
Ground – Neutral Detection Threshold	Total series impedance (R _n and R _g)	3.0		6.0	Ω
Internal Oscillator Frequency			2.0		MHz
CT Stimulus Current	Internally limited			1.0	mA
CT Driver Closed Loop BW				500	kHz

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

APPLICATIONS INFORMATION

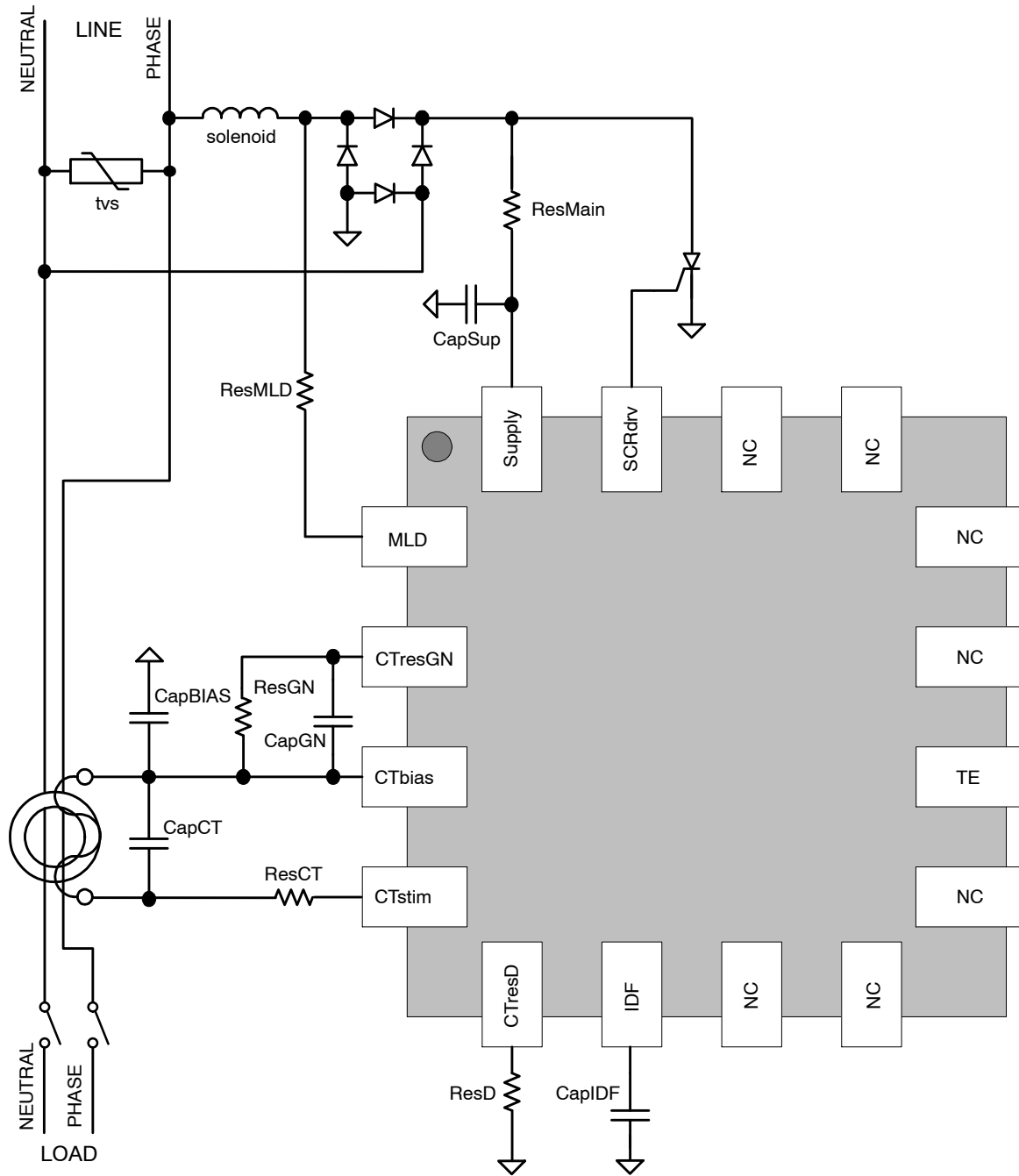


Figure 2. Typical Application Schematic

RECOMMENDED EXTERNAL COMPONENTS:

Component Type	Instance	Value	Note
SCR	Q1	–	ON–MCR08
Diode	Dx	–	ON–1N4007
Capacitor	Csup	1 – 5 μ F	For a full bridge rectifier
Capacitor	Cgn	2 – 10 nF	Low pass corner frequency for GN detection
Capacitor	Cidf	220 nF	1kHz differential corner frequency
Capacitor	Cct	2.2 – 5 nF	Match to current transformer for resonance
Capacitor	Cbias	10 nF	Added for filtering
Resistor	RctresD	40 – 80K	Matched to current transformer
Resistor	RctGN	100 – 400K	Matched to current transformer
Resistor	Rzc	400 – 800K	Zero cross detector shunt resistance
Resistor	Rmains	10 – 20K	For a full bridge rectifier
TVS	T1	–	~250 – 400 V

Filtering

The analog signal capture portion of the IC includes a single pole filter that can be set externally with Cidf. This provides an additional layer of protection against false tripping under steady state noise conditions. High frequency steady state noise is common with pumps, motors or other cyclic noise generators.

$Cidf = 220 \text{ nF} = 1 \text{ KHz low pass.}$

Setting Trip Sensitivity

The CTresD resistor sets the threshold for the differential current fault levels. Increasing CTresD causes the fault levels to trip at lower differential currents. CT efficiency at 60 Hz must be considered.

$CTresD = 200 * \#Turns - \text{Subject to CT efficiency at 60 Hz}$

The CTresGN resistor sets the threshold for ground to neutral fault detection. The Rt parameter is the desired

ground to neutral resistance trip level. Higher CTresGN values will cause the part to trip at higher ground to neutral impedances.

$CTresGN = \#Turns^2 \times Rt/2 - \text{Subject to CT efficiency from 3 kHz to 4 kHz}$

Setting Grounded–Neutral response time

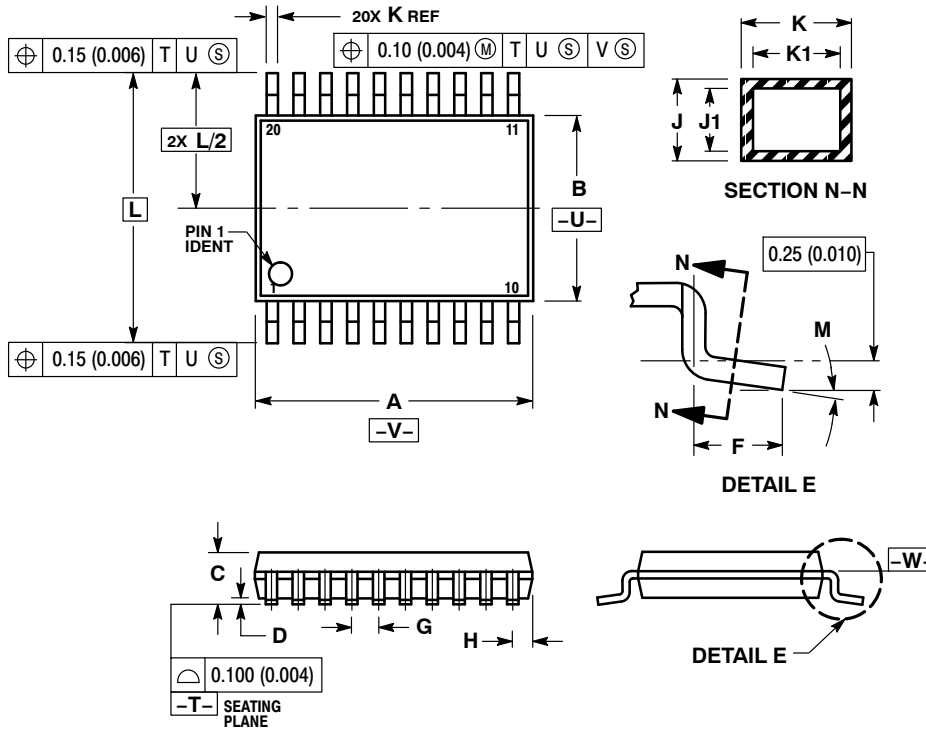
Cgn is used to define the response time of the grounded–neutral detection circuit. The analog portion converts the impedance into a DC voltage and a high frequency (aliased) component. The capacitor is used to remove the high frequency component leaving just the DC representation of the impedance.

$CTcapGN = 1.8E-4/CTresGN$

NCS37000

PACKAGE DIMENSIONS

TSSOP-20
CASE 948E-02
ISSUE C

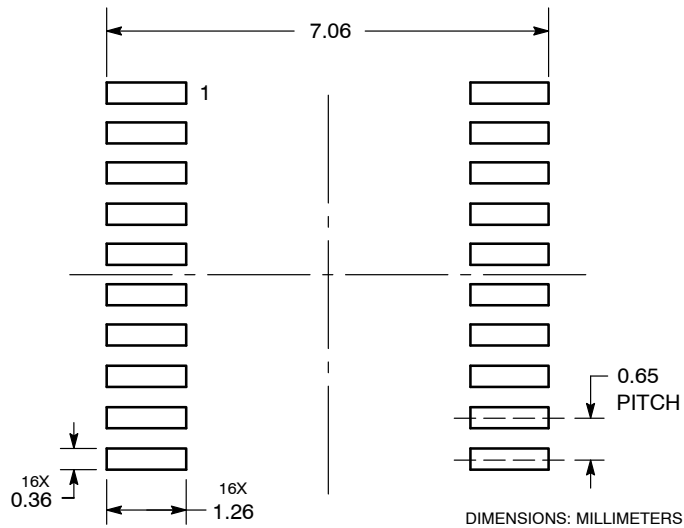


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

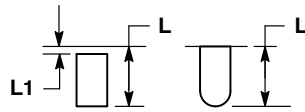
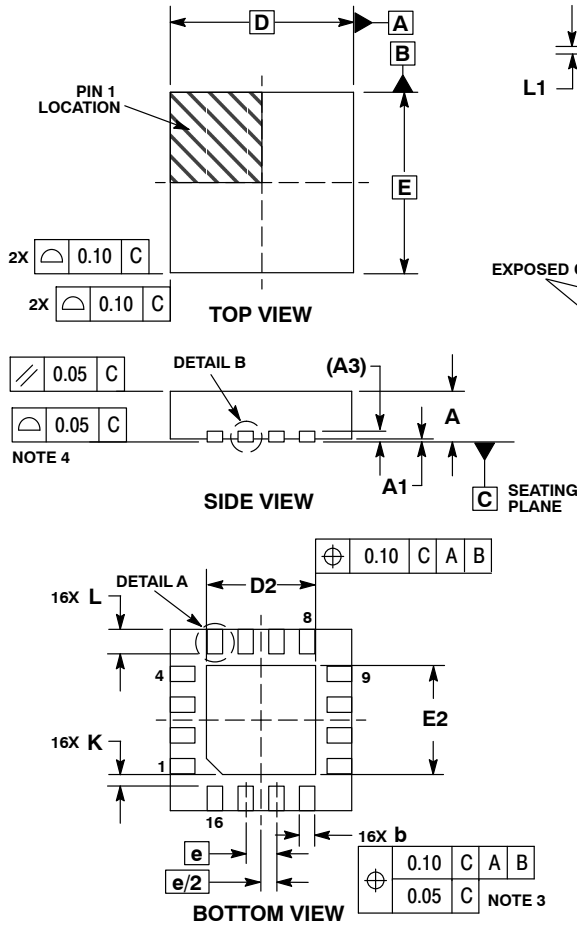
SOLDERING FOOTPRINT



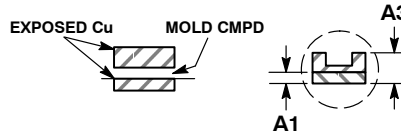
NCS37000

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P CASE 485G ISSUE F



DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS



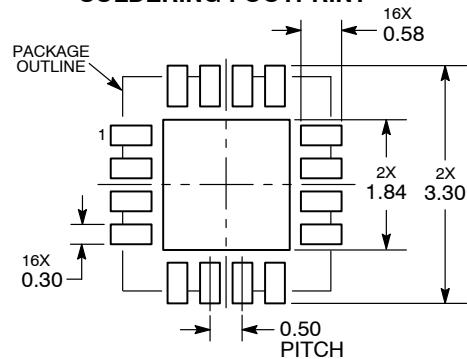
DETAIL B
ALTERNATE
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
K	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative