# DATA SHEET

## 74LV04
Hex inverter

Product specification
Supersedes data of 1997 Feb 03
IC24 Data Handbook

1998 Apr 20

Philips
Semiconductors

PHILIPS

## FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between $V_{CC}$ = 2.7 V and $V_{CC}$ = 3.6 V
- Typical $V_{OLP}$ (output ground bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_{amb}$ = 25°C
- Typical $V_{OHV}$ (output $V_{OH}$ undershoot) > 2 V at $V_{CC}$ = 3.3 V, $T_{amb}$ = 25°C
- Output capability: standard
- $I_{CC}$ category: SSI

## DESCRIPTION

The 74LV04 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT04.

The 74LV04 provides six inverting buffers.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25°C; $t_r = t_f \leq 2.5$ ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation delay nA to nY | $C_L$ = 15 pF; $V_{CC}$ = 3.3 V | 6 | ns |
| $C_I$ | Input capacitance | | 3.5 | pF |
| $C_{PD}$ | Power dissipation capacitance per gate | See Notes NO TAG and 2 | 21 | pF |

**NOTES:**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   $f_i$ = input frequency in MHz; $C_L$ = output load capacitance in pF;
   $f_o$ = output frequency in MHz; $V_{CC}$ = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_1$ is $V_1$ = GND to $V_{CC}$.

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | PKG. DWG. # |
|---|---|---|---|---|
| 14-Pin Plastic DIL | –40°C to +125°C | 74LV04 N | 74LV04 N | SOT27-1 |
| 14-Pin Plastic SO | –40°C to +125°C | 74LV04 D | 74LV04 D | SOT108-1 |
| 14-Pin Plastic SSOP Type II | –40°C to +125°C | 74LV04 DB | 74LV04 DB | SOT337-1 |
| 14-Pin Plastic TSSOP Type I | –40°C to +125°C | 74LV04 PW | 74LV04PW DH | SOT402-1 |

## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|---|---|---|
| 1, 3, 5, 9, 11, 13 | 1A – 6A | Data inputs |
| 2, 4, 6, 8, 10, 12 | 1Y – 6Y | Data outputs |
| 7 | GND | Ground (0 V) |
| 14 | $V_{CC}$ | Positive supply voltage |

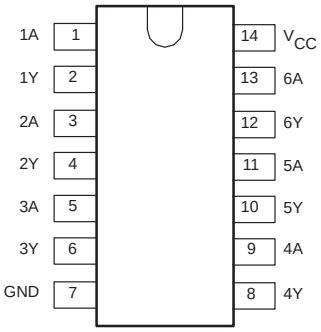
## FUNCTION TABLE

| INPUTS | OUTPUTS |
|---|---|
| **nA** | **nY** |
| L | H |
| H | L |

**NOTES:**

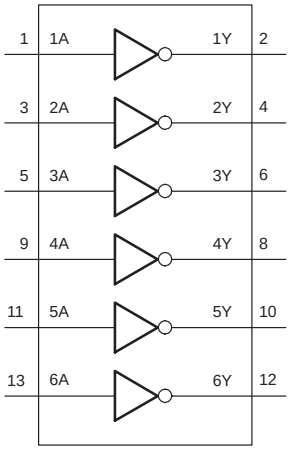
H = HIGH voltage level
L = LOW voltage level

## PIN CONFIGURATION



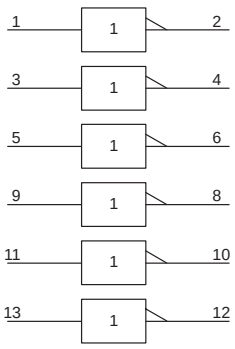

SV00396

## LOGIC SYMBOL




SV00397

## LOGIC SYMBOL (IEEE/IEC)

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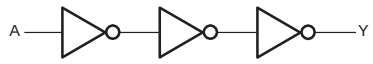
## LOGIC DIAGRAM (ONE INVERTER)




SV00399

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | See Note[NO TAG] | 1.0 | 3.3 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | – | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | – | $V_{CC}$ | V |
| $T_{amb}$ | Operating ambient temperature range in free air | See DC and AC characteristics | –40<br>–40 | | +85<br>+125 | °C |
| $t_r$, $t_f$ | Input rise and fall times | $V_{CC}$ = 1.0V to 2.0V<br>$V_{CC}$ = 2.0V to 2.7V<br>$V_{CC}$ = 2.7V to 3.6V<br>$V_{CC}$ = 3.6V to 5.5V | –<br>–<br>–<br>– | –<br>–<br>–<br>– | 500<br>200<br>100<br>50 | ns/V |

**NOTE:**
1. The LV is guaranteed to function down to $V_{CC}$ = 1.0V (input levels GND or $V_{CC}$); DC characteristics are guaranteed from $V_{CC}$ = 1.2V to $V_{CC}$ = 5.5V.

## ABSOLUTE MAXIMUM RATINGS NO TAG, NO TAG

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | –0.5 to +7.0 | V |
| $\pm I_{IK}$ | DC input diode current | $V_I < –0.5$ or $V_I > V_{CC} + 0.5V$ | 20 | mA |
| $\pm I_{OK}$ | DC output diode current | $V_O < –0.5$ or $V_O > V_{CC} + 0.5V$ | 50 | mA |
| $\pm I_O$ | DC output source or sink current<br>– standard outputs | $–0.5V < V_O < V_{CC} + 0.5V$ | 25 | mA |
| $\pm I_{GND}$,<br>$\pm I_{CC}$ | DC $V_{CC}$ or GND current for types with<br>– standard outputs | | 50 | mA |
| $T_{stg}$ | Storage temperature range | | –65 to +150 | °C |
| $P_{TOT}$ | Power dissipation per package<br>– plastic DIL<br>– plastic mini-pack (SO)<br>– plastic shrink mini-pack (SSOP and TSSOP) | for temperature range: –40 to +125°C<br>above +70°C derate linearly with 12 mW/K<br>above +70°C derate linearly with 8 mW/K<br>above +60°C derate linearly with 5.5 mW/K | <br>750<br>500<br>400 | mW |

**NOTES:**
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | -40°C to +85°C | | | -40°C to +125°C | | |
| | | | MIN | TYP. NO TAG | MAX | MIN | MAX | |
| $V_{IH}$ | HIGH level Input voltage | $V_{CC}$ = 1.2V | 0.9 | | | 0.9 | | V |
| | | $V_{CC}$ = 2.0V | 1.4 | | | 1.4 | | |
| | | $V_{CC}$ = 2.7 to 3.6V | 2.0 | | | 2.0 | | |
| | | $V_{CC}$ = 4.5 to 5.5V | $0.7 * V_{CC}$ | | | $0.7 * V_{CC}$ | | |
| $V_{IL}$ | LOW level Input voltage | $V_{CC}$ = 1.2V | | | 0.3 | | 0.3 | V |
| | | $V_{CC}$ = 2.0V | | | 0.6 | | 0.6 | |
| | | $V_{CC}$ = 2.7 to 3.6V | | | 0.8 | | 0.8 | |
| | | $V_{CC}$ = 4.5 to 5.5 | | | $0.3 * V_{CC}$ | | $0.3 * V_{CC}$ | |
| $V_{OH}$ | HIGH level output voltage; all outputs | $V_{CC}$ = 1.2V; $V_I = V_{IH}$ or $V_{IL}$; $–I_O$ = 100µA | | 1.2 | | | | V |
| | | $V_{CC}$ = 2.0V; $V_I = V_{IH}$ or $V_{IL}$; $–I_O$ = 100µA | 1.8 | 2.0 | | 1.8 | | |
| | | $V_{CC}$ = 2.7V; $V_I = V_{IH}$ or $V_{IL}$; $–I_O$ = 100µA | 2.5 | 2.7 | | 2.5 | | |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $–I_O$ = 100µA | 2.8 | 3.0 | | 2.8 | | |
| | | $V_{CC}$ = 4.5V; $V_I = V_{IH}$ or $V_{IL}$; $–I_O$ = 100µA | 4.3 | 4.5 | | 4.3 | | |
| $V_{OH}$ | HIGH level output voltage; STANDARD outputs | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $–I_O$ = 6mA | 2.40 | 2.82 | | 2.20 | | V |
| | | $V_{CC}$ = 4.5V; $V_I = V_{IH}$ or $V_{IL}$; $–I_O$ = 12mA | 3.60 | 4.20 | | 3.50 | | |
| $V_{OL}$ | LOW level output voltage; all outputs | $V_{CC}$ = 1.2V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 100µA | | 0 | | | | V |
| | | $V_{CC}$ = 2.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 100µA | | 0 | 0.2 | | 0.2 | |
| | | $V_{CC}$ = 2.7V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 100µA | | 0 | 0.2 | | 0.2 | |
| | | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 100µA | | 0 | 0.2 | | 0.2 | |
| | | $V_{CC}$ = 4.5V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 100µA | | 0 | 0.2 | | 0.2 | |
| $V_{OL}$ | LOW level output voltage; STANDARD outputs | $V_{CC}$ = 3.0V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 6mA | | 0.25 | 0.40 | | 0.50 | V |
| | | $V_{CC}$ = 4.5V; $V_I = V_{IH}$ or $V_{IL}$; $I_O$ = 12mA | | 0.35 | 0.55 | | 0.65 | |

## DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | -40°C to +85°C | | | -40°C to +125°C | | |
| | | | MIN | TYP. NO TAG | MAX | MIN | MAX | |
| $I_I$ | Input leakage current | $V_{CC}$ = 5.5V; $V_I$ = $V_{CC}$ or GND | | | 1.0 | | 1.0 | µA |
| $I_{CC}$ | Quiescent supply current; SSI | $V_{CC}$ = 5.5V; $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | | | 20.0 | | 40 | µA |
| $\Delta I_{CC}$ | Additional quiescent supply current | $V_{CC}$ = 2.7V to 3.6V; $V_I$ = $V_{CC}$ – 0.6V | | | 500 | | 850 | µA |

**NOTE:**
1. All typical values are measured at $T_{amb}$ = 25°C.

## AC CHARACTERISTICS

GND = 0V; $t_r$ = $t_f$ ≤ 2.5ns; $C_L$ = 50pF; $R_L$ = 1KΩ

| SYMBOL | PARAMETER | WAVEFORM | CONDITION | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | –40 to +85°C | | | –40 to +125°C | | |
| | | | $V_{CC}$(V) | MIN | TYP NO TAG | MAX | MIN | MAX | |
| $t_{PHL}/t_{PLH}$ | Propagation delay nA to nY | Figure 1 | 1.2 | | 40 | | | | ns |
| | | | 2.0 | | 14 | 20 | | 25 | |
| | | | 2.7 | | 10 | 15 | | 19 | |
| | | | 3.0 to 3.6 | | 8 NO TAG | 12 | | 15 | |
| | | | 4.5 to 5.5 | | | 9 | | 11 | |

**NOTES:**
1. Unless otherwise stated, all typical values are measured at $T_{amb}$ = 25°C
2. Typical values are measured at $V_{CC}$ = 3.3 V.

## AC WAVEFORMS

$V_M$ = 1.5 V at $V_{CC}$ ≥ 2.7 V and ≤ 3.6 V;
$V_M$ = 0.5 × $V_{CC}$ at $V_{CC}$ < 2.7 V and ≥ 4.5 V;
$V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.

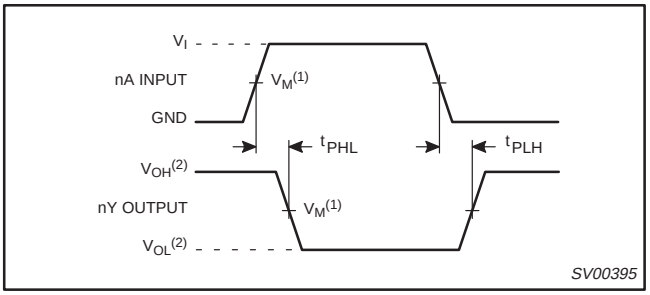
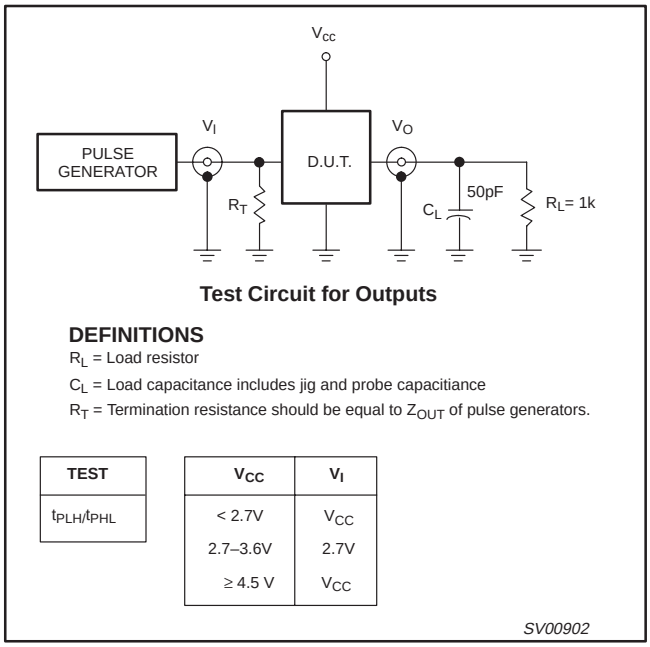



**Figure 1. Input (nA) to output (nY) propagation delays and output transition times.**

## TEST CIRCUIT




**Test Circuit for Outputs**

**DEFINITIONS**

$R_L$ = Load resistor

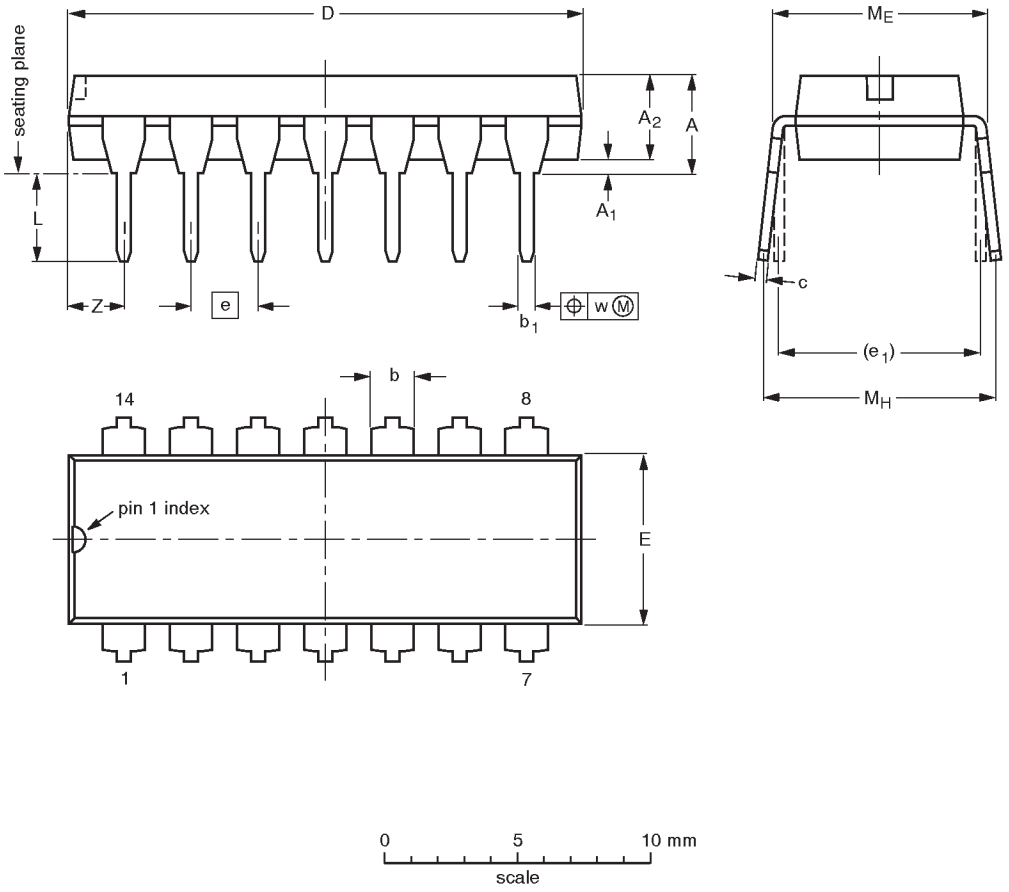
$C_L$ = Load capacitance includes jig and probe capacitiance

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

| TEST | $V_{CC}$ | $V_I$ |
|---|---|---|
| $t_{PLH}/t_{PHL}$ | < 2.7V | $V_{CC}$ |
| | 2.7–3.6V | 2.7V |
| | ≥ 4.5 V | $V_{CC}$ |

**Figure 2. Load circuitry for switching times**

**DIP14: plastic dual in-line package; 14 leads (300 mil)** **SOT27-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

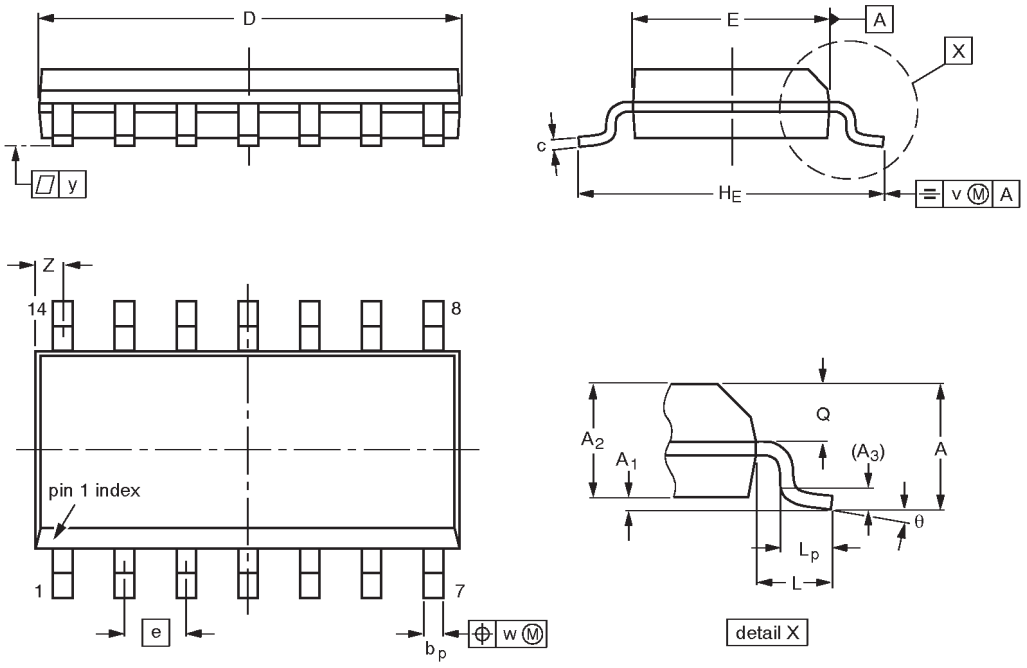
| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.13 | 0.53<br>0.38 | 0.36<br>0.23 | 19.50<br>18.55 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 2.2 |
| inches | 0.17 | 0.020 | 0.13 | 0.068<br>0.044 | 0.021<br>0.015 | 0.014<br>0.009 | 0.77<br>0.73 | 0.26<br>0.24 | 0.10 | 0.30 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.087 |

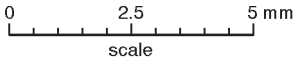
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT27-1 | 050G04 | MO-001AA | | | | ~~92-11-17~~<br>95-03-11 |

**SO14: plastic small outline package; 14 leads; body width 3.9 mm** **SOT108-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

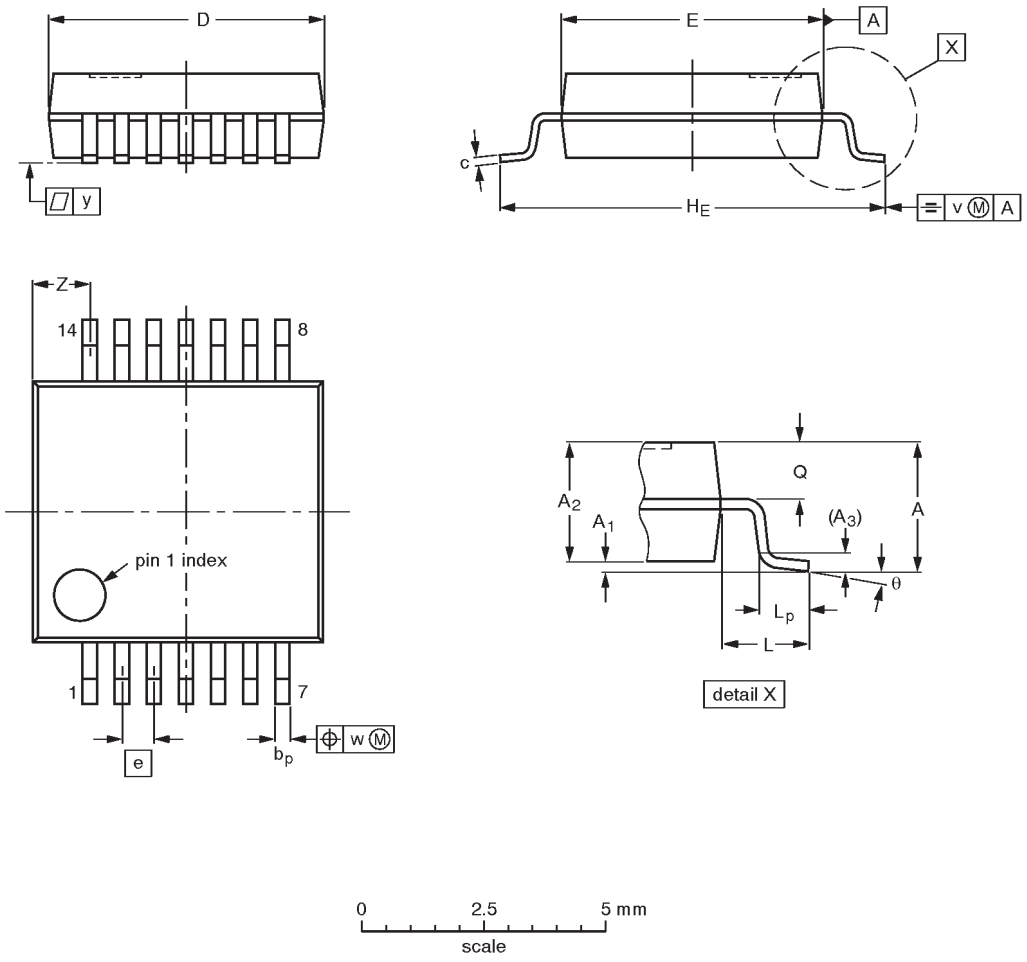
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 8.75<br>8.55 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | 8°<br>0° |
| inches | 0.069 | 0.0098<br>0.0039 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0098<br>0.0075 | 0.35<br>0.34 | 0.16<br>0.15 | 0.050 | 0.24<br>0.23 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT108-1 | 076E06S | MS-012AB | | | | ~~91-08-13~~<br>95-01-23 |

**SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm** **SOT337-1**




**DIMENSIONS (mm are the original dimensions)**

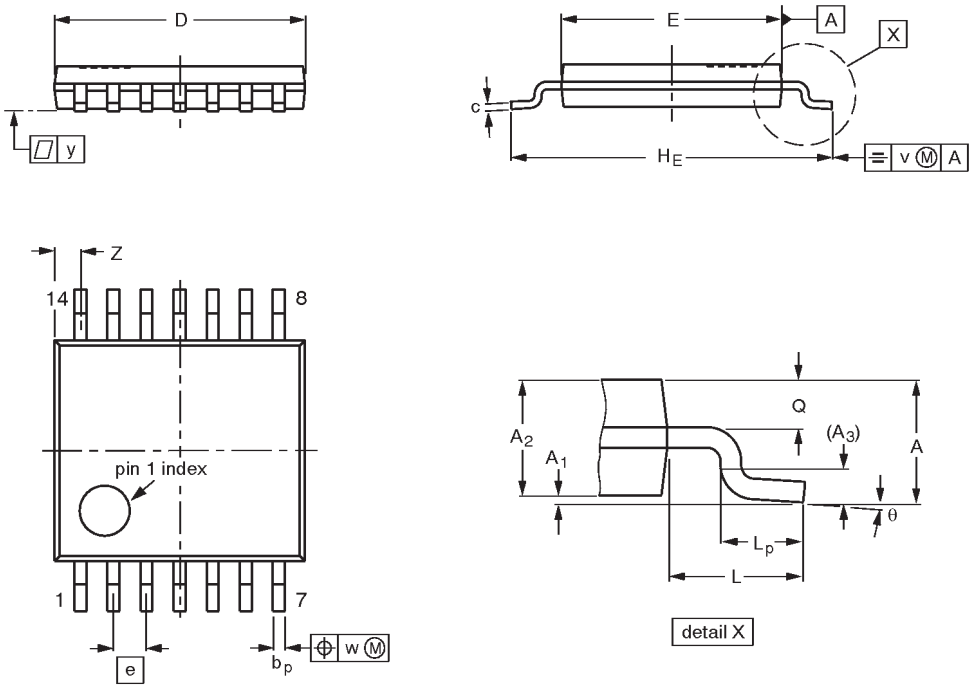
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.0 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 6.4<br>6.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.4<br>0.9 | 8°<br>0° |

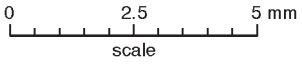
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT337-1 | | MO-150AB | | | | ~~95-02-04~~<br>96-01-18 |

**TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm** **SOT402-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.10 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1.0 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.72<br>0.38 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT402-1 | | MO-153 | | | | ~~94-07-12~~<br>95-04-04 |

## DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|---|---|---|
| *Objective Specification* | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| *Preliminary Specification* | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| *Product Specification* | Full Production | This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product. |



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