

## FSP2161

### FEATURES

- Low-Dropout Regulator Supports Input Voltages Down to 1.4V
- Output Voltage Available in 0.9V, 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 2.85V, 3.0V, 3.3V
- Stable with a Ceramic Output Capacitor of 1.0uF or Higher
- Low Dropout Voltage: 150mV at 1.5A
- Low Quiescent Current
- Over Temperature Shutdown
- Short Circuit Protection
- Low Temperature Coefficient
- Standard TO252 and TO263 Packages

### APPLICATIONS

- DSP, FPGA, and Microprocessor Power Supplies
- 1.2V Core Voltage for DSPs
- SATA Power Supply
- LCD TV/ Monitors
- Wireless Devices
- Communication Devices
- Portable Electronics
- Post Regulator for SMPS

### GENERAL DESCRIPTION

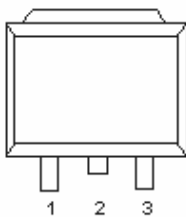
The FSP2161 is a 1.5A CMOS LDO regulator that features a low quiescent current, ultra low input, output and dropout voltages, as well as over temperature shutdown. It is available in TO252 and TO263 packages. The fixed output voltage of the FSP2161 is set at the factory and trimmed to  $\pm 2\%$ . The FSP2161 is stable with a ceramic output capacitor of 1.0uF or higher.

This family of regulators can provide either a stand-alone power supply solution or act as a post regulator for switch mode power supplies. They are particularly well suited for applications requiring low input and output voltage

### PIN CONFIGURATION

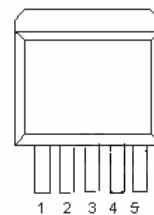
1) TO252

(Top View)



2) TO263

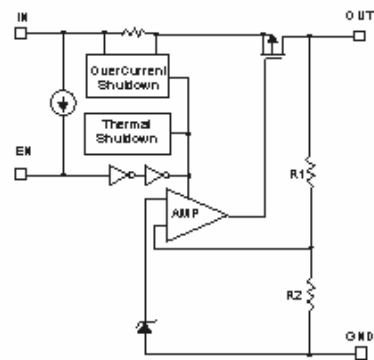
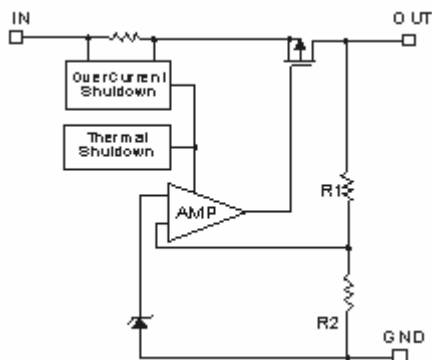
(Top View)



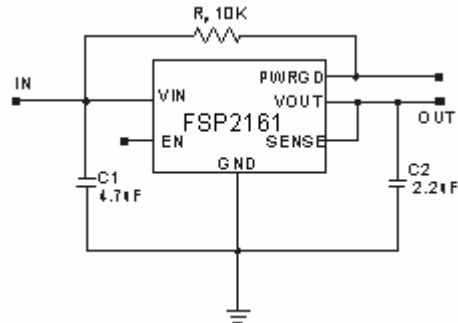
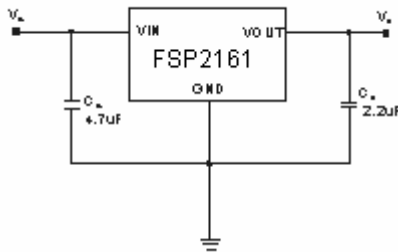
### PIN DESCRIPTION

Pin Number		Pin Name	Pin Function
TO252	TO263		
1	1	VIN	Input
2	3	GND	Ground
3	5	VOUT	Output
	2	EN	Enable pin
	4	PWRGD	Power good

### BLOCK DIAGRAM



### ■ TYPICAL APPLICATIONS CIRCUITS



### ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Input Supply Voltage	+4	V
Maximum Output Current	PD/(VIN-VO)	
Output Pin Voltage	-0.3 to VIN+0.3	V
Internal Power Dissipation	1200	mW
Junction to Case Thermal Resistance ( $\theta_{JC}$ )	7	$^{\circ}\text{C}/\text{W}$
Junction to Ambient Thermal Resistance ( $\theta_{JA}$ )	90	$^{\circ}\text{C}/\text{W}$
Operating temperature	-40 to 85	$^{\circ}\text{C}$
Operating Junction Temperature	-40 to 125	$^{\circ}\text{C}$
Storage Temperature	-65 to 150	$^{\circ}\text{C}$
Maximum Junction Temperature	150	$^{\circ}\text{C}$
Lead Temperature (Soldering, 5 sec)	300	$^{\circ}\text{C}$

Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

### ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Unit
Input Supply Voltage	1.4 to 3.6	V
Operating temperature	-40 to 85	$^{\circ}\text{C}$
Operating Junction Temperature	-40 to 125	$^{\circ}\text{C}$

**■ ELECTRICAL CHARACTERISTICS**

( $V_{OUT} = V_{IN} + 0.5V$ ,  $C_{IN} = 1\mu F$ ,  $C_O = 2.2\mu F$ ,  $T_A = 25^\circ C$  unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Input Voltage	$V_{IN}$		Note1		3.6	V	
Output Voltage Accuracy	$V_O$	$I_O = 100mA$	-2		+2	%	
Short Circuit Current	$I_{SC}$	$V_O < 0.3V$		1.0		A	
Ground Current	$I_{GND}$	$I_O = 1mA$ to 1.5A			600	$\mu A$	
Quiescent Current	$I_Q$	$I_O = 0mA$		90	150	$\mu A$	
Line Regulation	LNR	$I_O = 10mA$ , $V_O \leq 2.5V$ $V_{IN} = V_O + 0.5V$ to $V_O + 1.5V$		0.5	1	%V	
		$I_O = 10mA$ , $V_O > 2.5V$ $V_{IN} = 3.3V$ to 3.6V		0.5	1		
Load Regulation Error	LDR	$I_O = 1mA$ to 1.5A		0.5	2	%/A	
Temperature Coefficient	$T_C$			40		ppm/ $^\circ C$	
Over Temperature Shutdown	OTS			150		$^\circ C$	
Over Temperature Hystersis	OTH			50		$^\circ C$	
Power Supply Ripple Rejection	PSRR	$I_O = 100mA$ $V_O = 1.5V$	f=100Hz		55	dB	
			f= 1KHz		55		
			f= 10KHz		35		
Dropout Voltage	$V_{DROP}$	$I_O = 500mA$	$V_O = 0.9V$		330	500	mV
			$V_O = 1.0V$		220	400	
			$1.2V \leq V_O < 2.5V$		50	200	
			$V_O \geq 2.5V$		40	150	
		$I_O = 1.5A$	$V_O = 0.9V$		330	500	
			$V_O = 1.0V$		220	400	
			$1.2V \leq V_O < 2.5V$		150	350	
			$V_O \geq 2.5V$		120	300	
Output Noise	$V_n$	f = 10Hz to 100kHz		40		$\mu V_{RMS}$	

Note 1: The minimum input voltage of the FSP2161 is determined by output voltage and dropout voltage. The minimum input voltage is defined as:

$$V_{IN(MIN)} = V_O + V_{DROP}$$

### ■ APPLICATION INFORMATION

The FSP2161 family of low-dropout (LDO) regulators have several features that allow them to apply to a wide range of applications. The family operates with very low input voltage (1.4V) and low dropout voltage (typically 150mV at full load), making it an efficient stand-alone power supply or post regulator for battery or switch mode power supplies. The 1.5A output current make the FSP2161 family suitable for powering many microprocessors and FPGA supplies. The FSP2161 family also has low output noise (typically 40µVRMS with 2.2µF output capacitor), making it ideal for use in telecom equipment.

#### External Capacitor Requirements

A 2.2µF or larger ceramic input bypass capacitor, connected between VIN and GND and located close to the FSP2161, is required for stability. A 1.0µF minimum value capacitor from VO to GND is also required. To improve transient response, noise rejection, and ripple rejection, an additional 10µF or larger, low ESR capacitor is recommended at the output. A higher-value, low ESR output capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source, especially if the minimum input voltage of 1.4 V is used.

#### Regulator Protection

The FSP2161 features internal current limiting, thermal protection and short circuit protection. During normal operation, the FSP2161 limits output current to about 3A. When current limiting engages, the output voltage scales back linearly until the over current condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C, thermal-protection circuitry will shut down. Once the device has cooled down to approximately 50°C below the high temp trip point, regulator operation resumes. The short circuit current of the FSP2161 is about 1A when its output pin is shorted to ground.

#### Thermal Information

The amount of heat that an LDO linear regulator generates is:

$$P_D = (V_{IN} - V_O) I_O$$

All integrated circuits have a maximum allowable junction temperature (TJ max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (TJ) does not exceed the maximum junction temperature (TJ max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ( $P_{D(max)}$ ) consumed by a linear regulator is computed as:

$$P_{DMAX} = (V_{I(avg)} - V_{O(avg)}) I_{O(avg)} + I_{(Q)} I_{(Q)}$$

Where:

$V_{I(avg)}$  is the average input voltage.

$V_{O(avg)}$  is the average output voltage.

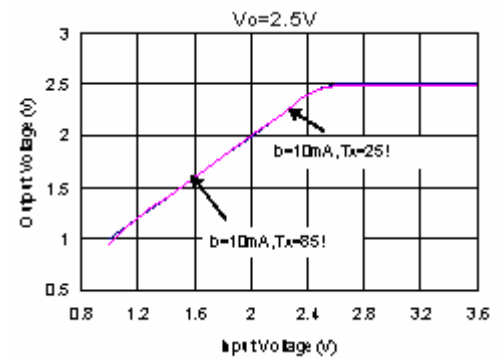
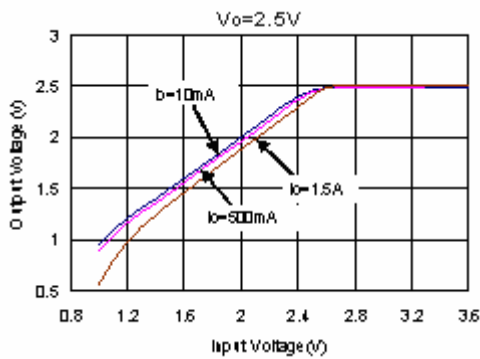
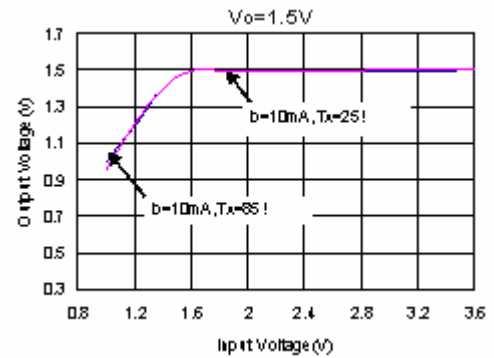
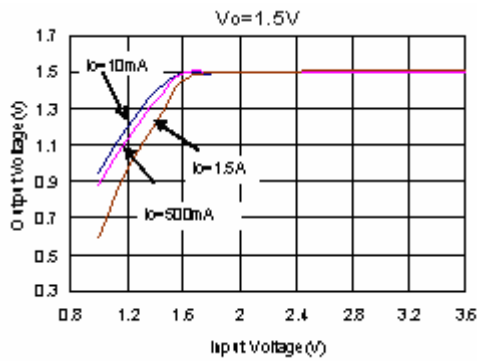
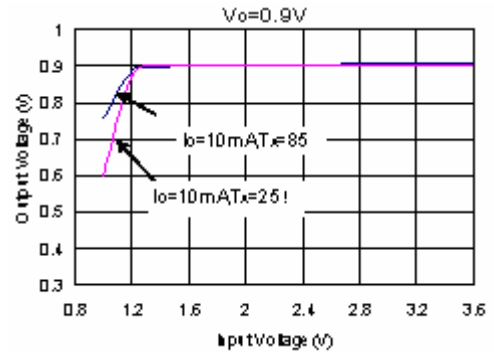
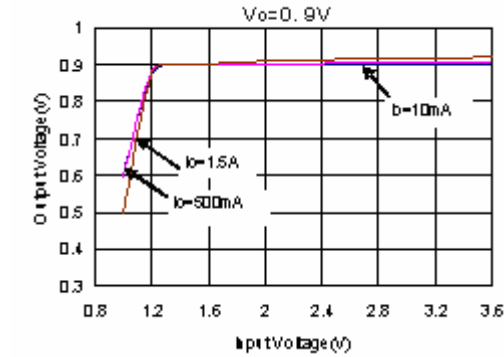
$I_{O(avg)}$  is the average output current.

$I_{(Q)}$  is the quiescent current.

For most LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term  $V_{I(avg)} \times I_{(Q)}$  can be neglected. The operating junction temperature is computed by adding the ambient temperature (TA) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case (RθJC), the case to heatsink (RθCS), and the heatsink to ambient (RθSA). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation so that the object's thermal resistance will be lower.

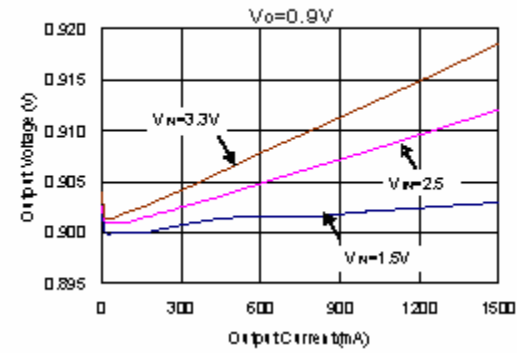
■ TYPICAL PERFORMANCE CHARACTERISTICS

1. Output Voltage vs Input Voltage

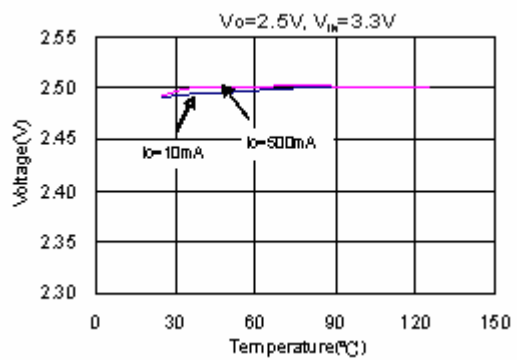
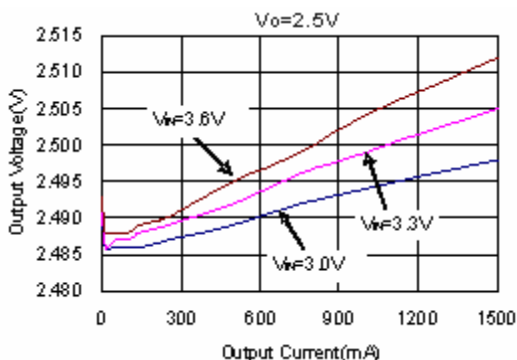
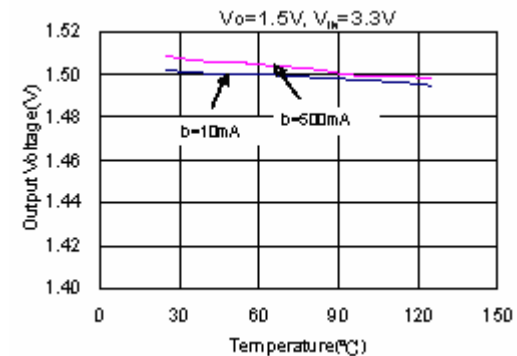
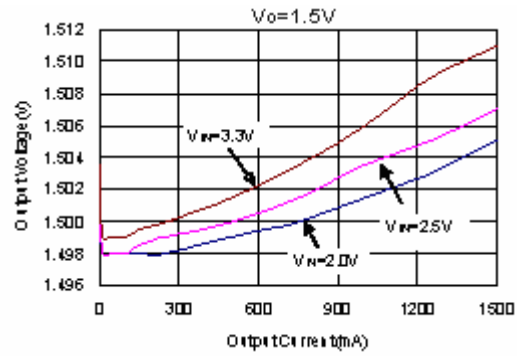
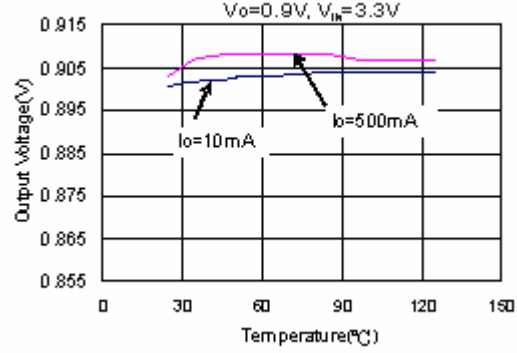


■ TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

2. Output Voltage vs Output Current

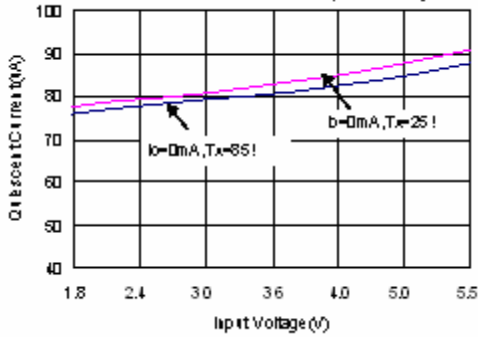


3. Output Voltage vs Temperature

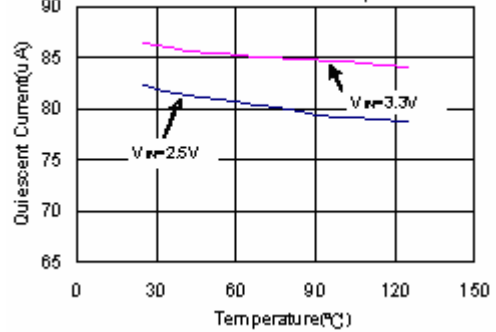


### TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

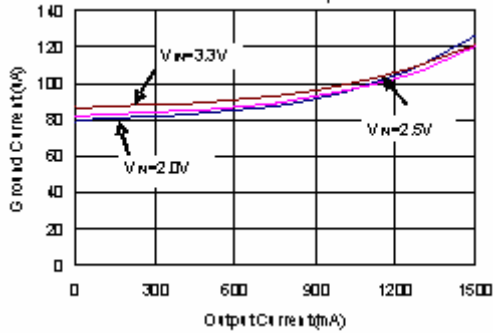
4. Quiescent Current vs Input Voltage



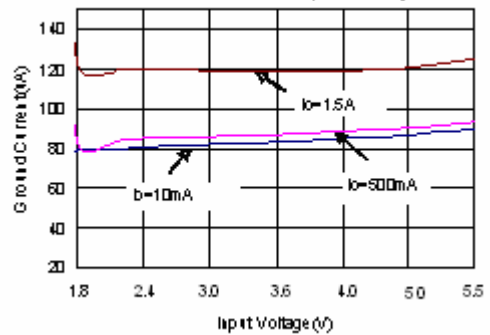
5. Quiescent Current vs Temperature



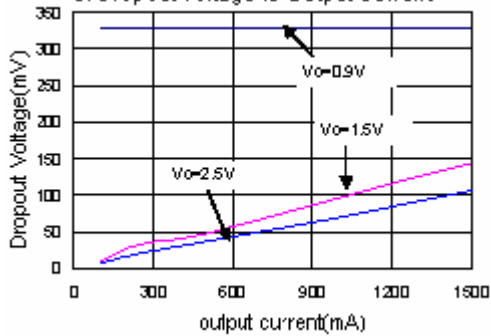
6. Ground Current vs Output Current



7. Ground Current vs Input Voltage

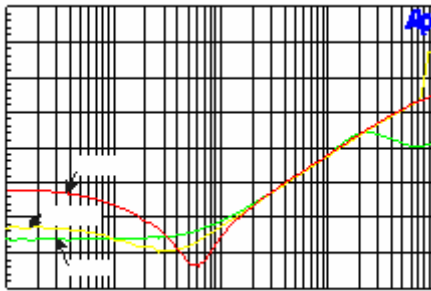


8. Dropout Voltage vs Output Current

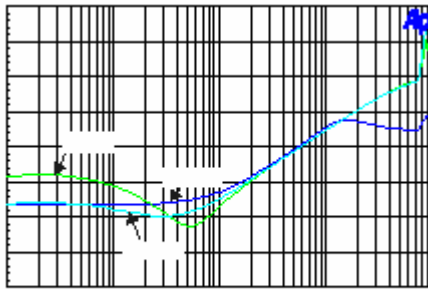


### ■ TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

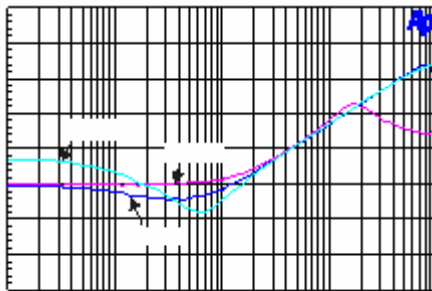
9. Ripple Rejection vs Frequency



$V_o=0.9V, V_{in}=2.5V, V_{pp}=1V$

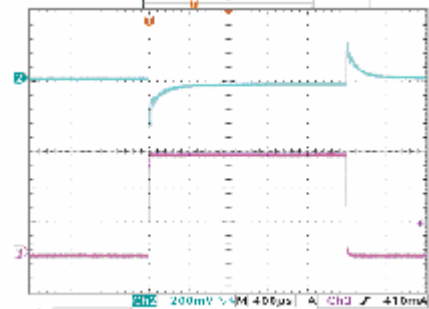


$V_o=1.5V, V_{in}=2.5V, V_{pp}=1V$

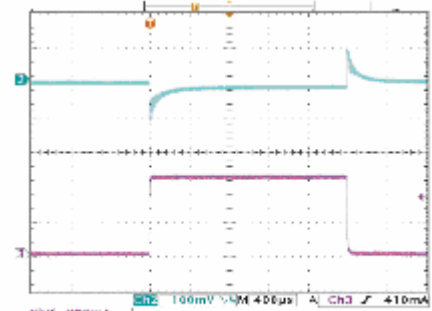


$V_o=2.5V, V_{in}=3.3V, V_{pp}=0.3V$

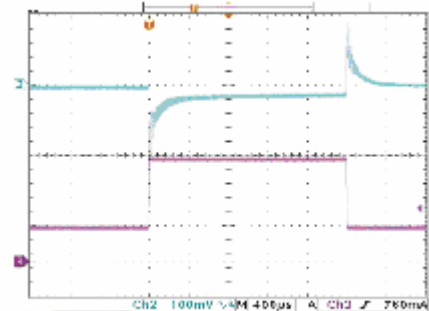
10. Load Transient Response



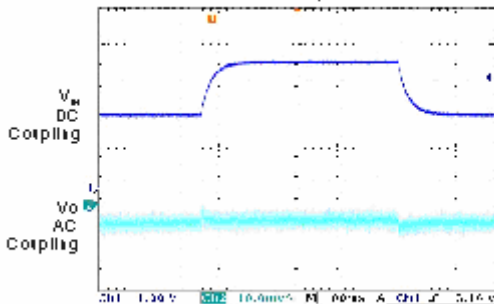
$V_o=1.5V, V_{in}=3.3V, I_o=10mA \text{ to } 1.5A$



$V_o=1.5V, I_o=10mA \text{ to } 500mA$



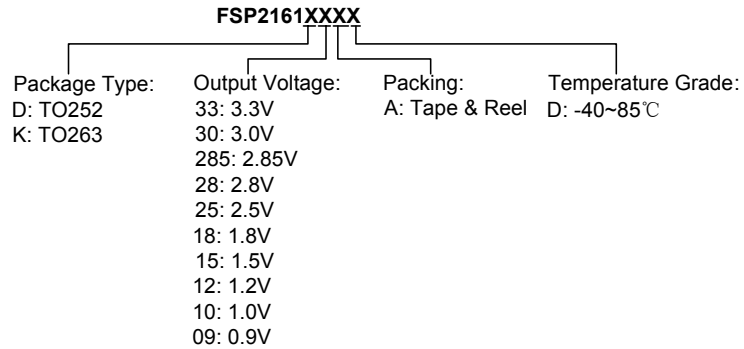
11. Line Transient Response



$V_o=1.5V, V_{in}=2V \text{ to } 3.3V, I_o=1mA$



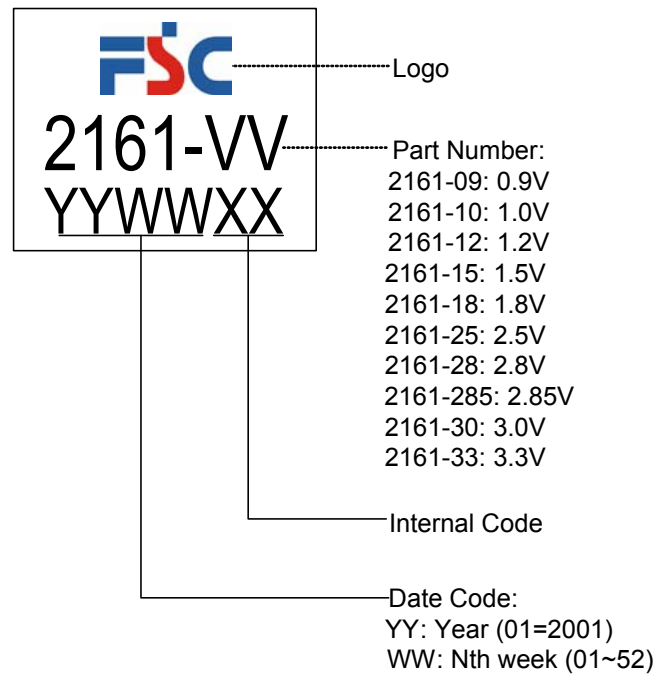
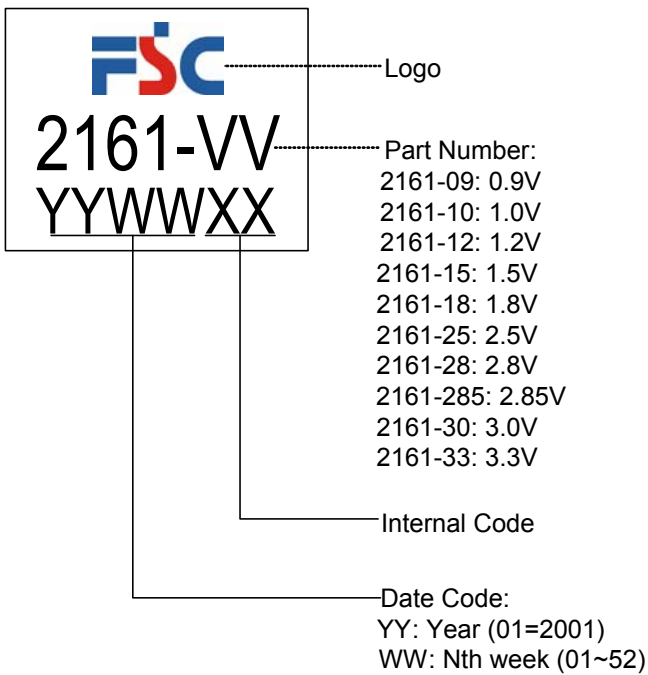
### ORDERING INFORMATION



### MARKING INFORMATION

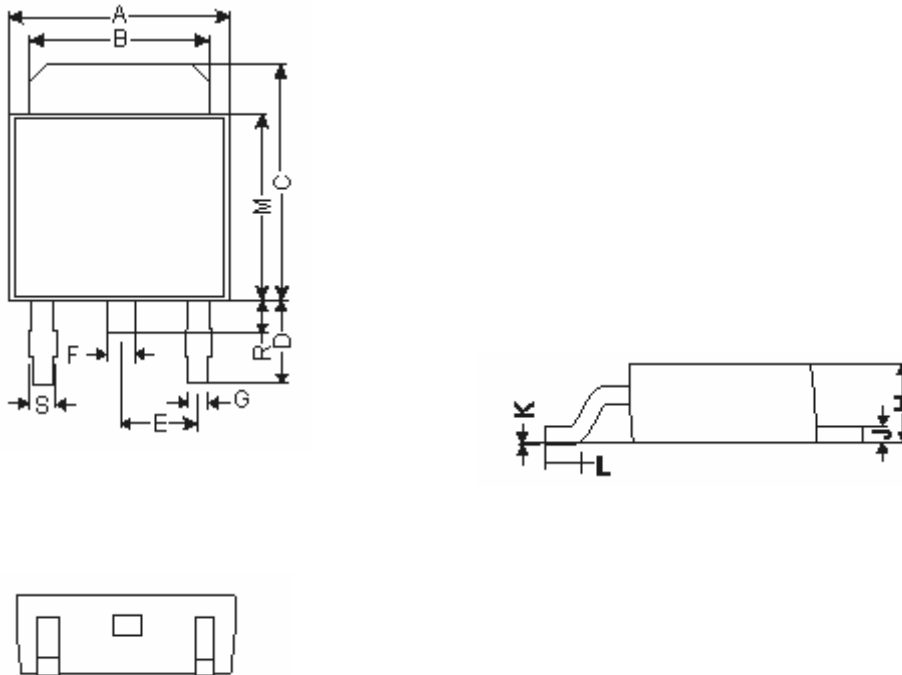
(1) TO252

(2) TO263



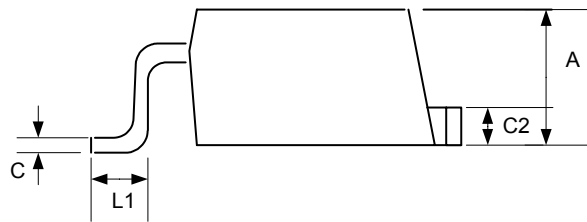
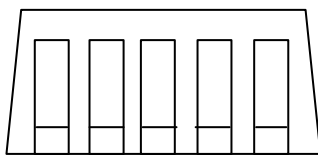
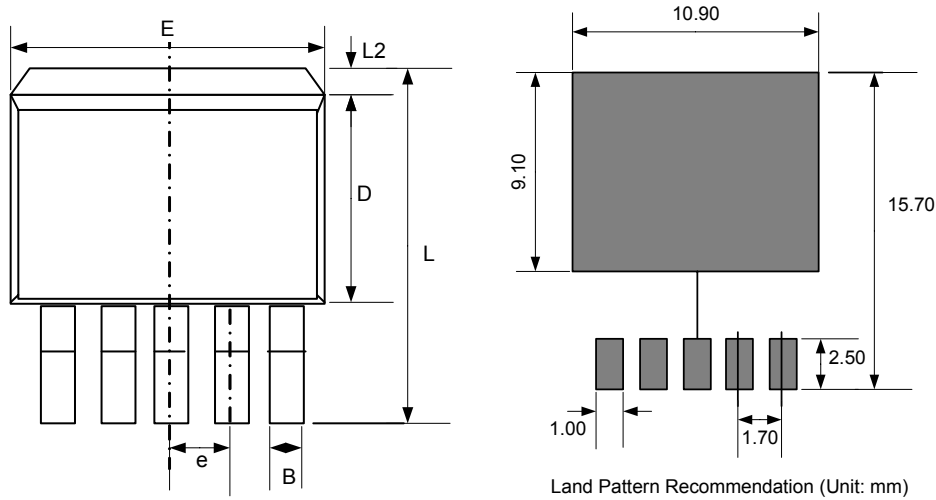
### ■ PACKAGE INFORMATION

(1) TO252



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	6.40	6.60	6.80	0.256	0.264	0.272
B	5.20	5.35	5.50	0.208	0.214	0.220
C	6.80	7.00	7.20	0.272	0.280	0.288
D	2.20	2.50	2.80	0.088	0.100	0.112
E	2.30REF			0.092REF		
F	0.70	0.80	0.90	0.028	0.032	0.036
S	0.60	0.75	0.90	0.024	0.030	0.036
G	0.50	0.60	0.70	0.020	0.024	0.028
H	2.20	2.30	2.40	0.088	0.092	0.096
J	0.45	0.50	0.55	0.018	0.020	0.022
K	0	0.07	0.15	0	0.003	0.006
L	0.90	1.20	1.50	0.036	0.048	0.060
M	5.40	5.60	5.80	0.216	0.224	0.232
R	0.80	1.00	1.20	0.032	0.040	0.048

### 2) TO263



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	4.07	4.46	4.85	0.163	0.176	0.194
B	0.51	0.84	1.02	0.020	0.033	0.041
C	0.36	0.50	0.74	0.014	0.020	0.030
C2	1.14	1.27	1.65	0.046	0.050	0.066
D	8.20	9.15	9.65	0.328	0.360	0.380
E	9.65	10.16	10.67	0.386	0.400	0.427
e	1.57	1.71	1.85	0.063	0.068	0.074
L	14.45	15.24	15.88	0.578	0.600	0.635
L1	1.78	2.54	2.79	0.071	0.100	0.110
L2			2.92			0.115

