SY89831U

Ultra-Precision 1:4 LVPECL Fanout Buffer/Translator with Internal Termination

Precision Edge®

General Description

The SY89831U is a high-speed, 2GHz differential LVPECL 1:4 fanout buffer optimized for ultra-low skew applications. Within-device skew is guaranteed to be less than 20ps (5ps typ.) over supply voltage and temperature. The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A VREF-AC reference output is included for AC-coupled applications.

The SY89831U is a part of Micrel's high-speed clock synchronization family. For applications that require a different I/O combination, consult Micrel's website at: www.micrel.com, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators, and clock generators.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Precision Edge®

Features

- Guaranteed AC performance over temperature and voltage
  - DC-to 2.5GHz throughput (typical)
  - 350ps propagation delay (IN-to-Q) (typical)
  - 5ps within-device skew (typical)
  - 150ps rise/fall time (typical)
- Ultra-low jitter design
  - 62fs RMS phase jitter (typical)
- Unique patent-pending input termination and VT pin accepts DC- and AC-coupled differential inputs
- 800mV, 100K LVPECL typical output swing
- Power supply 2.5V ±5% or 3.3V ±10%
- Industrial temperature range: –40°C to +85°C
- Available in 16-pin (3mm x 3mm) MLF® package

Applications

- Processor clock distribution
- SONET clock distribution
- Fibre Channel clock distribution
- Gigabit Ethernet clock distribution

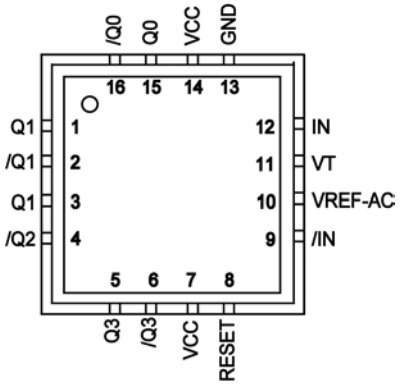
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89831UMG[2]	MLF-16	Industrial	831U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89831UMGTR[2, 3]	MLF-16	Industrial	831U with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Pb-Free package is recommended for new designs.
3. Tape and Reel.

Pin Configuration



16-MLF (MLF-16)

Pin Description

Pin #	Pin Name	Functional Description
15, 16 1, 2 3, 4 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	Differential 100K LVPECL Outputs: These LVPECL outputs are the precision, low-skew copies of the inputs. Please refer to the "Truth Table" section for details. Unused output pairs may be left open. Terminate with 50Ω to V_{CC} – 2V. See the "Output Termination Recommendations" section for more details.
8	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable only occurs when the outputs are in a logic low state. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic high state (enabled) if left open.
9, 12	/IN, IN	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled differential signs as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs default to an intermediate state if left open. Please refer to the "Input Interface Applications" section for more details.
10	VREF-AC	Reference Voltage: These outputs bias to VCC – 1.4V. They are used when AC coupling the inputs (IN, /IN). For AC-coupled applications, connect VREF-AC to the VT pin and bypass with a 0.01µF low-ESR capacitor to V_{CC}. See the "Input Interface Applications" section for more details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, each VREF-AC pin should only drive its respective VT pin. If VREF-AC is used with a 2.5V supply, make sure the input swing is large enough to comply with the V_{IH} min. spec.

Pin #	Pin Name	Functional Description
11	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See the "Input Interface Applications" section for more details.
13	GND	Ground. GND pins and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with 0.1µF/0.01µF low-ESR capacitors placed as close as possible to each VCC pin.

Truth Table

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0[4]	1[4]

Note:

4. On the next negative transition of the input signal (IN).

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Absolute Maximum Ratings[5]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} + 0.5V
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current
  Source or Sink Current on (IN, /IN) ..... ±50mA
VREF-AC Current
  Source or Sink Current on (I_{VT}) ..... ±2mA
Lead Temperature (soldering, 20s) ..... 260°C
Storage Temperature (Ts) ..... –65°C to +150°C

Operating Ratings[6]

Supply Voltage Range ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[7]
  (θ_{JA}) Still Air ..... 60°C/W
  (θ_{JA}) Junction to Board ..... 32°C/W

DC Electrical Characteristics[8]

T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply		2.375 3.0		2.625 3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		47	70	mA
R_{IN}	Input Resistance (IN-to-VT)		45	50	55	Ω
$R_{DIFF-IN}$	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)		1.2		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)		0		V_{IH} – 0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN – /IN|	See Figure 2.	0.2			V
$V_{REF–AC}$	Output Reference Voltage		V_{CC} – 1.525	V_{CC} – 1.425	V_{CC} – 1.325	V

LVTTL/LVCMOS Input DC Electrical Characteristics

V_{CC} = 2.375V to 3.60V; V_{EE} = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		–125		20	µA
I_{IL}	Input LOW Current		–300			µA

Notes:

5. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this datasheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
6. The datasheet limits are not guaranteed if the device is operated beyond the operating ratings.
7. Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. Ψ_{JB} and θ_{JA} values are determined for a 4-layer board at the still-air package thermal resistance, unless otherwise stated.
8. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

LVPECL Output DC Electrical Characteristics[8]

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC} – 2V; T_A = –40°C to + 85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage (Q, /Q)		V_{CC} – 1.145		V_{CC} – 0.895	V
V_{OL}	Output LOW Voltage (Q, /Q)		V_{CC} – 1.945		V_{CC} – 1.695	V
V_{OUT}	Output Voltage Swing (Q, /Q)	See Figure 1.	550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing (Q, /Q)	See Figure 2.	1100	1600		mV

LVTTL/LVCMOS DC Electrical Characteristics[8]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to + 85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current		–300			µA

AC Electrical Characteristics[9]

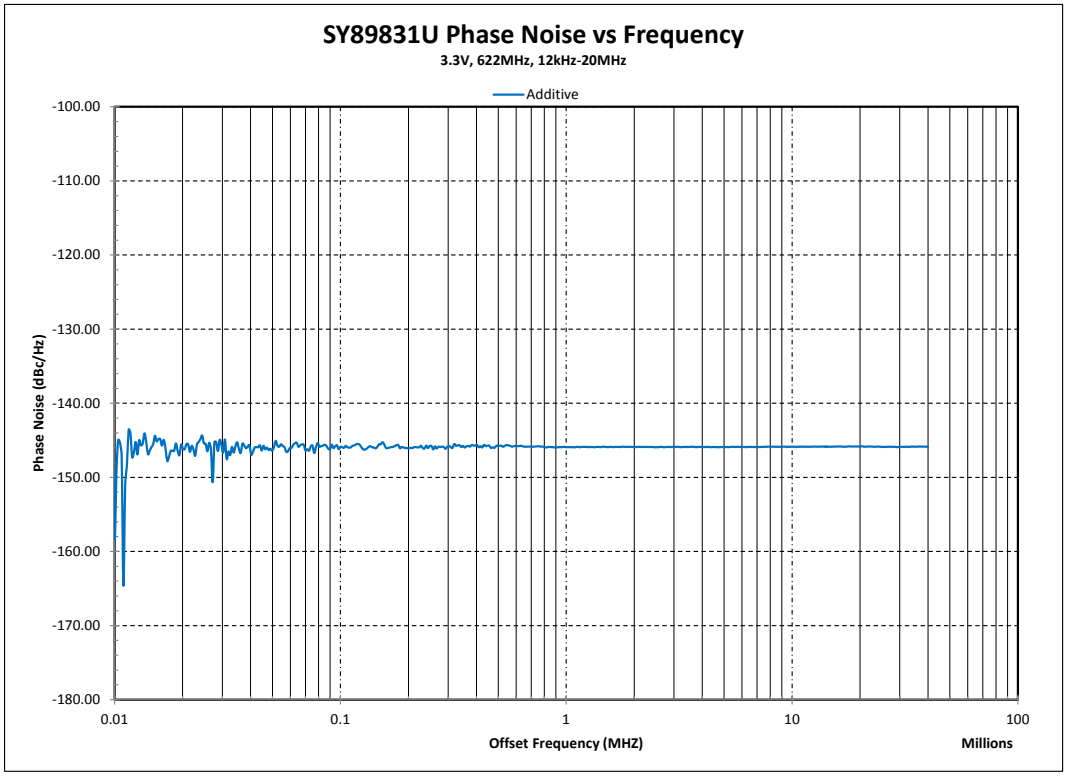
V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC} – 2V; T_A = –40°C to + 85°C, unless otherwise noted.

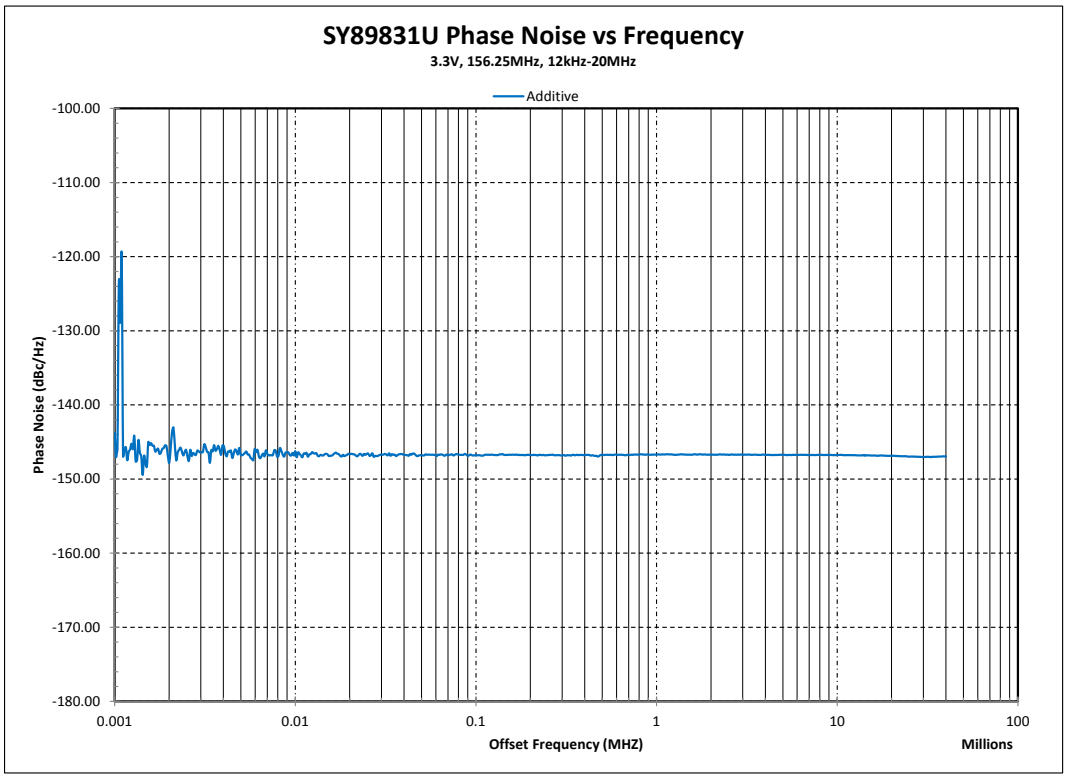
Symbol	Parameter		Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum Frequency		V_{OUT} ≥ 450mV	2.0	2.5		GHz
t_{pd}	Propagation Delay	IN-to-Q	V_{IN} ≥ 100mV		390		ps
		IN-to-Q	V_{IN} ≥ 800mV	250	350	450	ps
t_{SKEW}	Within-Device Skew		Note 10		5	20	ps
	Part-to-Part Skew		Note 11			150	ps
t_S	Set-Up Time	EN to IN, /IN	Note 12	300			ps
t_H	Hold Time	EN to IN, /IN	Note 12	300			ps
t_{JITTER}	RMS Phase Jitter		Output = 622MHz Integration Range 12kHz–20MHz		62		fs
t_r, t_f	Output Rise/Fall Times (20% to 80%)		At full output swing	70	150	225	ps
	Duty Cycle		Freq. < 630MHz	48	50	52	%

Notes:

9. High-frequency AC parameters are guaranteed by design and characterization.
10. Within-device skew is measured between two different outputs under identical input transitions.
11. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
12. Set-up and hold times apply to synchronous applications that will enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.

Typical Phase Noise





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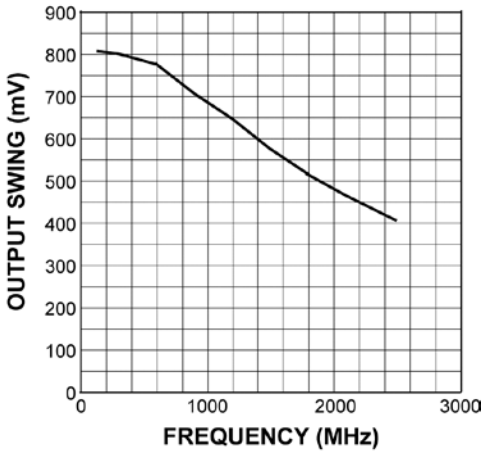
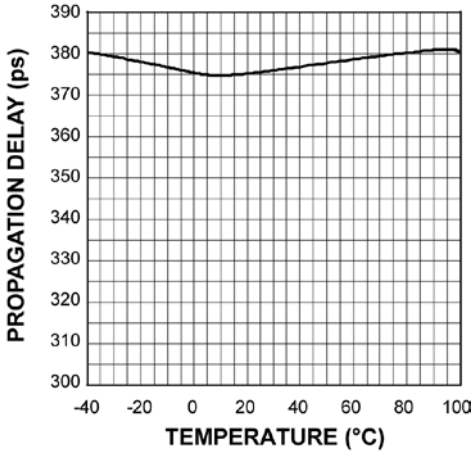
Typical Characteristics

V_{CC} = 3.3V; GND = 0V; R_L = 50Ω to V_{CC} – 2V; T_A = 25°C, unless otherwise noted.

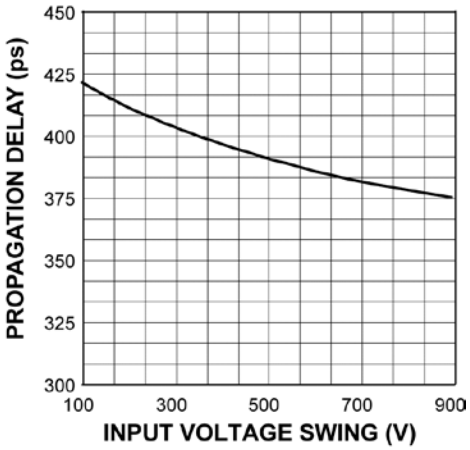
Output Swing vs. Frequency



Propagation Delay vs. Temperature



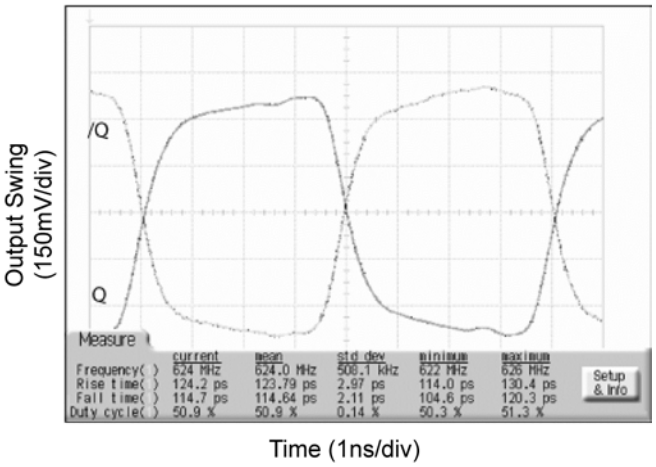
Propagation Delay vs. Input Voltage Swing



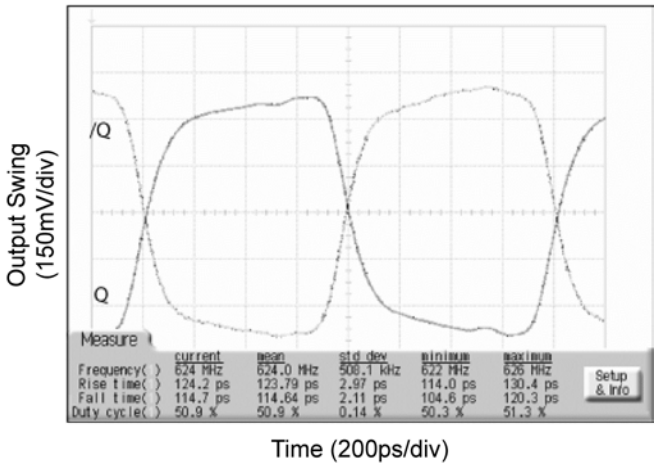
Typical Output Waveforms

V_{CC} = 3.3V; GND = 0V; V_{IN} = 800mV; R_L = 50Ω to V_{CC} – 2V; T_A = 25°C, unless otherwise noted.

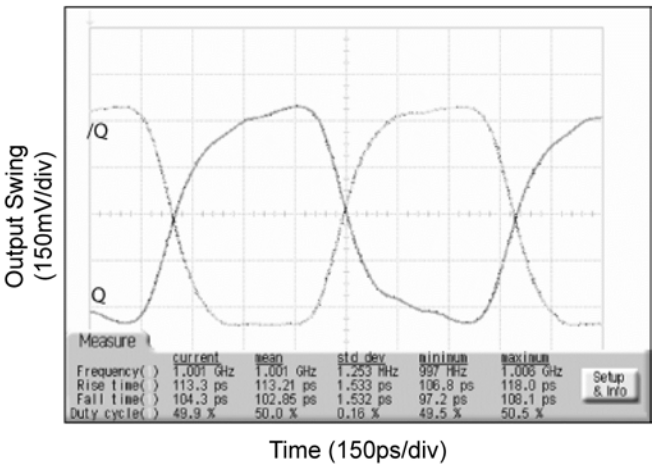
155MHz Output



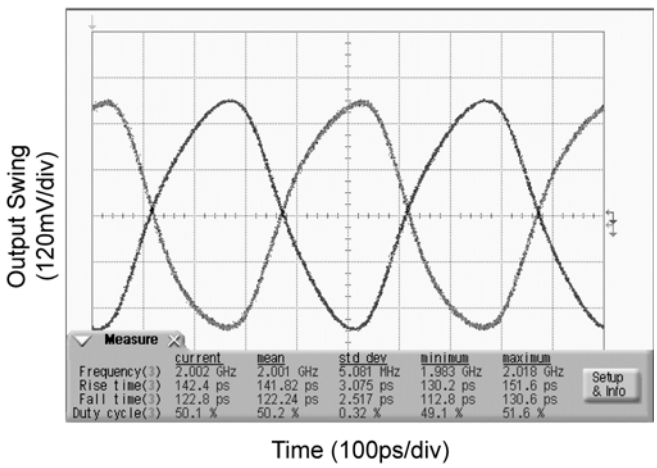
622MHz Output



1GHz Output



2GHz Output



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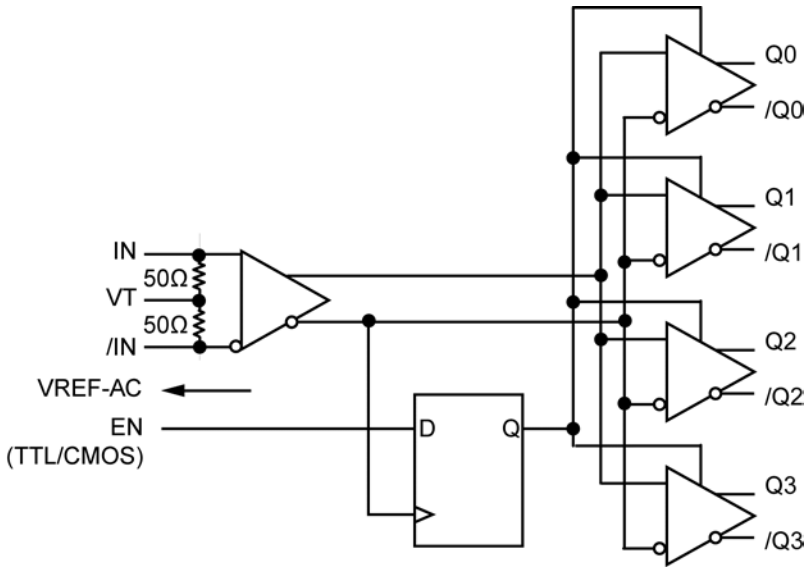
Functional Block Diagram



Single-Ended and Differential Swings

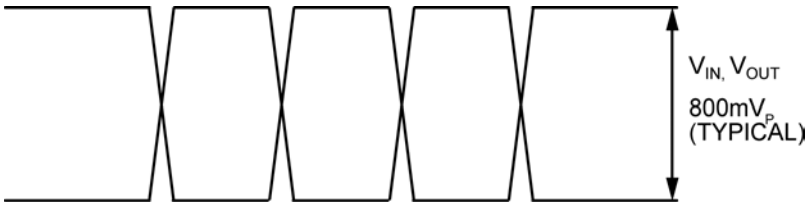


Figure 1. Single-Ended Swing

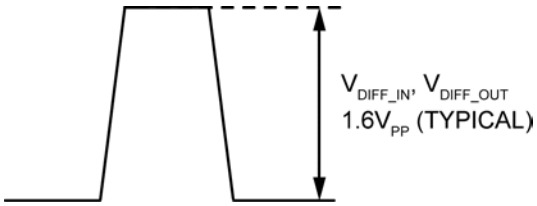


Figure 2. Differential Swing

Input and Output Stages

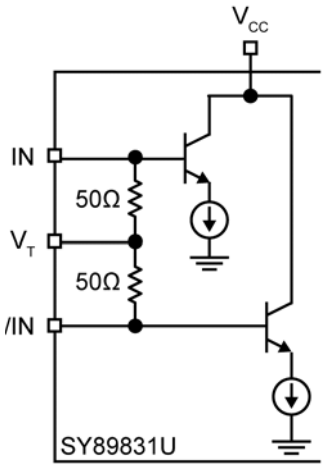


Figure 3. Simplified Differential

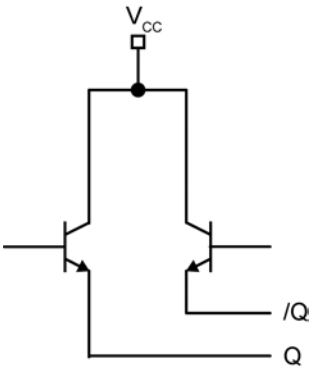


Figure 4. Simplified LVPECL Output Stage

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Input Interface Applications

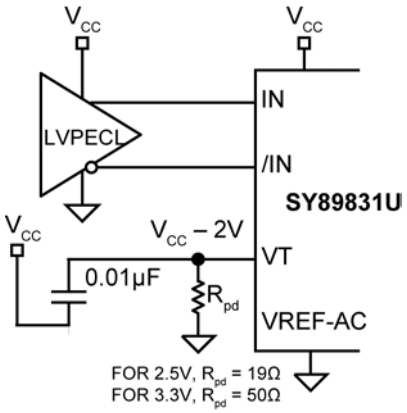

Figure 5. DC-Coupled LVPECL Input Interface

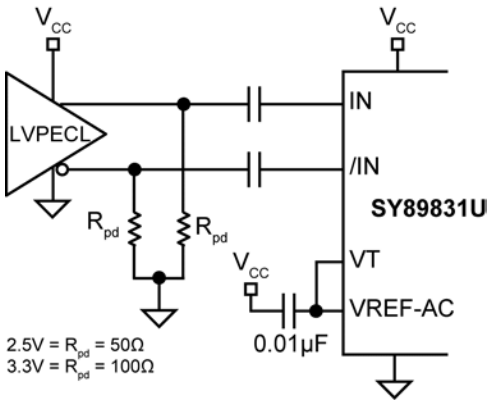

Figure 6. AC-Coupled LVPECL Input Interface

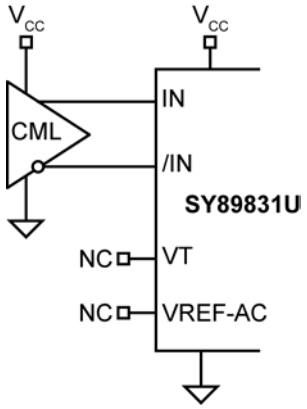

Figure 7. DC-Coupled CML Input Interface

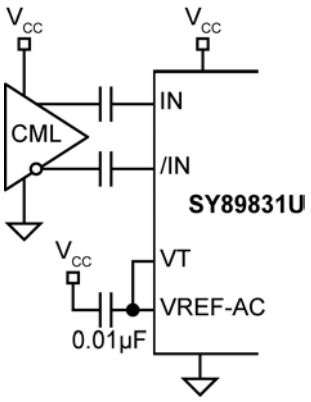

Figure 8. AC-Coupled CML Input Interface

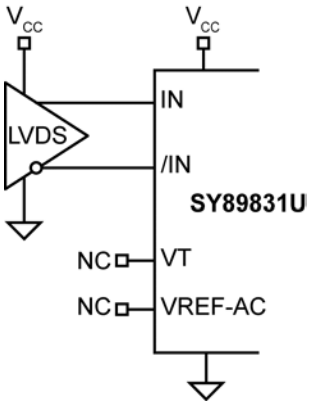

Figure 9. DC-Coupled LVDS Input Interface

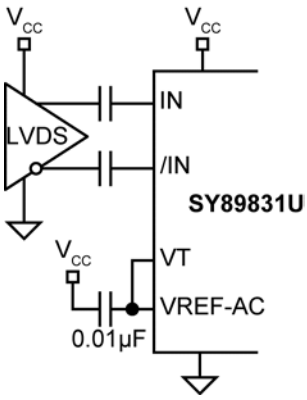

Figure 10. AC-Coupled LVDS Input Interface

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Output Termination Recommendations

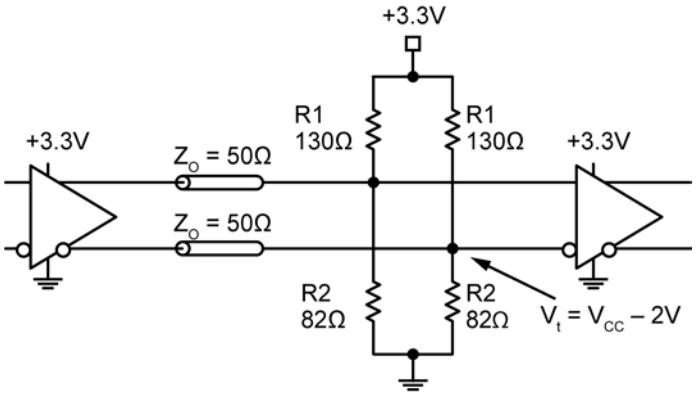


Figure 11. Parallel Termination – Thevenin Equivalent

Note:

13. For +2.5V Systems: R1 = 250Ω, R2 = 62.5Ω.

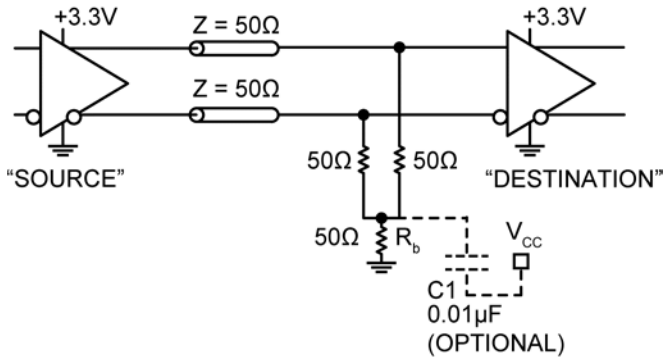


Figure 12. Three-Resistor "Y-Termination"

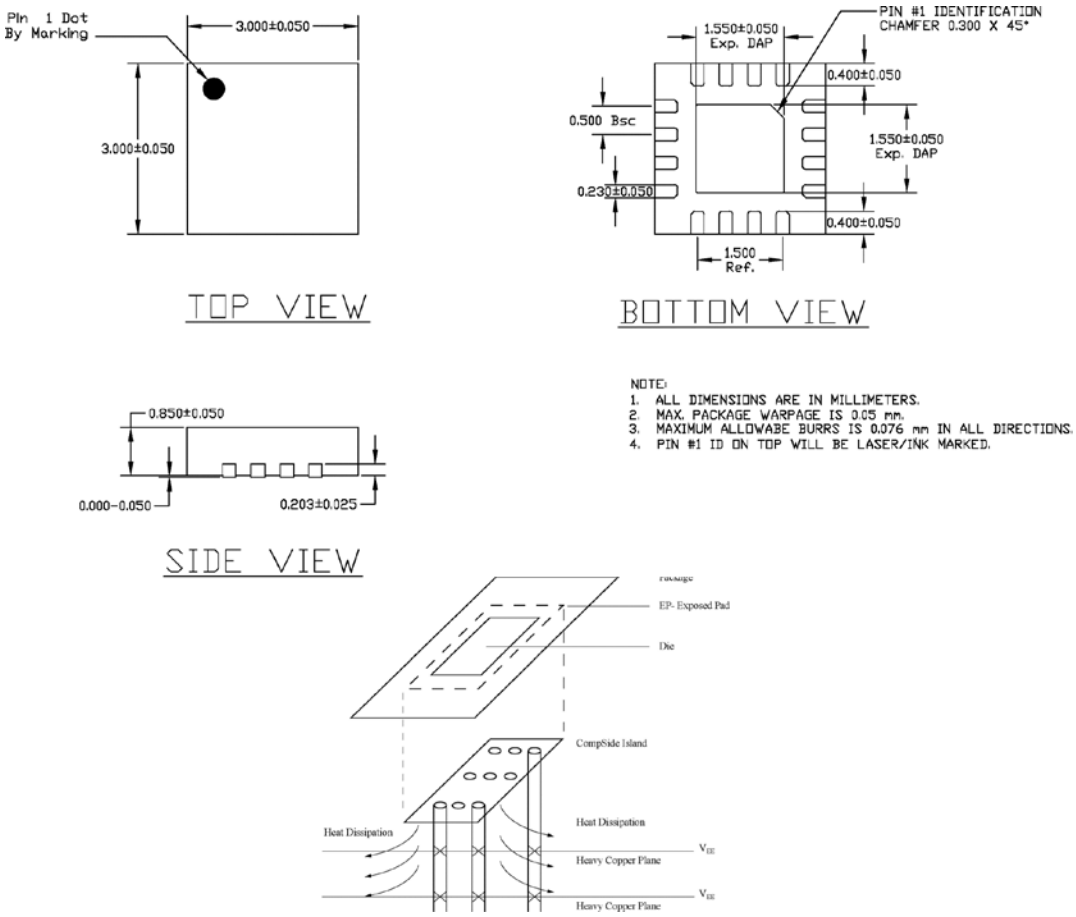
Notes:

14. Power-saving alternative to Thevenin termination.
15. Place termination resistors as close to destination inputs as possible.
16. The R_b resistor sets the DC bias voltage equal to V_t. For +2.5V systems, R_b = 19Ω.
17. C1 is an optional bypass capacitor that compensates for any t_r/t_f mismatches.

Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY89830U	1:4 LVPECL Fanout Buffer w/2:1 MUX Input	http://www.micrel.com/index.php/en/products/clock-timing/clock-data-distribution/fanout-buffers/article/51-sy89830u.html
SY89832U	2.5V Ultra-Precision 1:4 LVDS Fanout Buffer/ Translator with Internal Termination	http://www.micrel.com/index.php/en/products/clock-timing/clock-data-distribution/fanout-buffers/article/38-sy89832u.html
SY89833AL	3.3V Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination	http://www.micrel.com/index.php/en/products/clock-timing/clock-data-distribution/fanout-buffers/article/39-sy89833al.html
SY89834U	2.5/3.3V Two Input, 1GHz LVTTL/CMOS-to-LVPECL 1:4 Fanout Buffer/Translator	http://www.micrel.com/index.php/en/products/clock-timing/clock-data-distribution/fanout-buffers/article/50-sy89834u.html
	16-MLF® Manufacturing Guidelines Exposed Pad Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0301.pdf

Package Information[18]



PCB Thermal Consideration for 16-Pin MLF Package
(Always solder, or equivalent, the exposed pad to the PCB)

16-Pin EPAD MicroLeadFrame® (MLF-16)

Notes:

18. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.
19. Package meets Level 2 moisture sensitivity classification, and is shipped in dry-pack.
20. Exposed pads must be soldered to a ground for proper thermal management.

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