

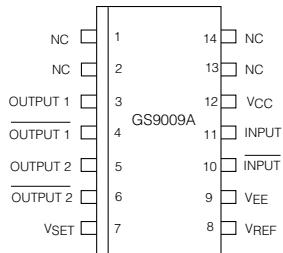
KEY FEATURES

- two output pairs, adjustable from 0 to 1100mVp-p into 75 Ω loads
- nominal 600 ps rise and fall times
- accepts SMPTE and standard ECL input levels
- operates from a single +5 or -5 volt supply
- on-chip DC restoration for low jitter
- 250 mW power dissipation
- interfaces with GENLINX™ GS9002, GS9004A, GS9005A and GS9015A
- Pb-free and Green

APPLICATIONS

- SMPTE 259M Serial Digital Systems (4:2:2 & 4fsc)
- Other Serial Digital Video Interfaces — 360Mb/s
- General purpose high speed driver applications

PIN CONNECTIONS



DESCRIPTION

The GENLINX™ GS9009A is a bipolar integrated circuit designed to drive four 75 Ω co-axial cables at data rates exceeding 400Mb/s. It directly interfaces with other GENLINX™ devices and can also be used as a general purpose high speed cable driver.

The differential inputs are AC-coupled and internally DC-restored which allows correct passage of pathological check codes associated with the serial digital standards. Even though the inputs are AC coupled, static protection diodes at each input restrict the DC differential so that if the driving source uses the opposite polarity power supply, external DC blocking capacitors must be used.

Correctly terminated output signal levels are adjustable from as low as 0mV to as high as 1100mV with little change in other performance parameters. Performance is guaranteed for output levels between 600 mV and 1000 mV. The gain of the output stages is varied by adjusting the V_{SET} voltage with respect to an internal bandgap reference voltage V_{REF} .

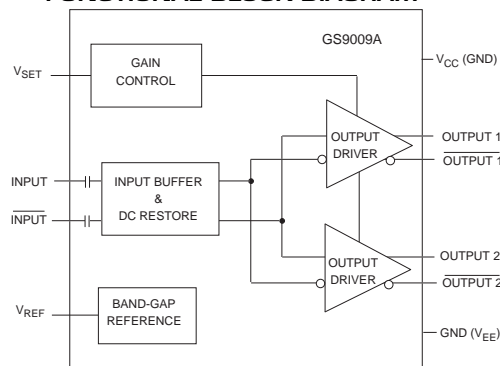
Pinout is compatible with the GS9007A by interchanging pins 3,4,5,6,9,10,11,12 on the GS9009A with pins 1,2,3,4,5,6,7,8 on the GS9007A. In this way, a layout can be made for either device depending on whether adjustability is desired or not.

The GS9009A is packaged in a 14 pin SOIC, and operates from a single +5 or -5 volt supply consuming typically only 250mW of power.

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	TEMPERATURE RANGE	Pb-FREE AND GREEN
GS9009ACKB	14 Pin SOIC	0° to 70°C	No
GS9009ACKBE3	14 Pin SOIC	0° to 70°C	Yes

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage (V_S)	5.5V
Input Voltage Range (any input)	$V_S - 0.5V$
Power Dissipation	300mW
Operating Temperature Range	$0^{\circ}C \leq T_A \leq 70^{\circ}C$
Storage Temperature Range	$-65^{\circ}C \leq T_S \leq 150^{\circ}C$
Lead Temperature (soldering, 10 sec)	260°C

GS9009A CABLE DRIVER — DC ELECTRICAL CHARACTERISTICS

Conditions: $V_S = 5V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$, $R_L = 150 \Omega$ to GND and 144Ω AC coupled unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_S		4.5	5.0	5.5	volts	
Power Consumption	P_D	4 x 150 Ω Loads DC 1% Accuracy, $T_A = 25^{\circ}C$ $V_{SET} = (0.667) V_{REF}$	-	250	290	mW	
Supply Current	I_{S1}		-	105	110	mA	
Supply Current	I_{S2}	DC No Loads, $T_A = 25^{\circ}C$	-	16	20	mA	
Reference Voltage	V_{REF}	10 k Ω to ground	-	1.2	-	volts	

GS9009A CABLE DRIVER — AC ELECTRICAL CHARACTERISTICS

Conditions: $V_S = 5V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$, $R_L = 150 \Omega$ to GND and 144Ω AC coupled unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Signal Amplitude	V_{IN}		700	800	1000	mVp-p	
Input Signal Rise/Fall Times	t_R, t_F		-	-	750	ps	
Output Amplitudes across 75 Ω Load (See Note 1)	V_{OUT}	$V_{SET} = (0.5) V_{REF}$	540	600	660	mVp-p	Note 1 & 2
		$V_{SET} = (0.667) V_{REF}$	720	800	880	mVp-p	Note 1 & 2
		$V_{SET} = (0.833) V_{REF}$	900	1000	1100	mVp-p	Note 1 & 2
Output Amplitude Temperature Coefficient (See Note 2)	T_C	$V_{SET} = (0.5) V_{REF}$	-	25	100	ppm/ $^{\circ}C$	
		$V_{SET} = (0.667) V_{REF}$	-	-12	80	ppm/ $^{\circ}C$	
		$V_{SET} = (0.833) V_{REF}$	-	-45	80	ppm/ $^{\circ}C$	
Output Rise/Fall Times (20% to 80%)	t_R, t_F	$V_{SET} = (0.5) V_{REF}$	400	630	800	ps	
		$V_{SET} = (0.667) V_{REF}$	400	575	800	ps	
		$V_{SET} = (0.833) V_{REF}$	400	530	800	ps	
Output Overshoot		$t_R = t_F = 600$ ps	-	0	-	%	See Figure 3
Jitter	t_J	at 270Mb/s	-	-	± 25	ps	
Propagation Delay	t_P		-	1	-	ns	

- V_{OUT} is measured across a correctly terminated load, back matched to the device. The peak to peak voltage of the device itself is $2 \times V_{OUT}$.
- V_{OUT} is proportional to V_{SET} and V_{SET} may be an external low impedance, high stability supply. In this case the amplitude temperature coefficient will not be guaranteed.

INPUT/OUTPUT CIRCUITS

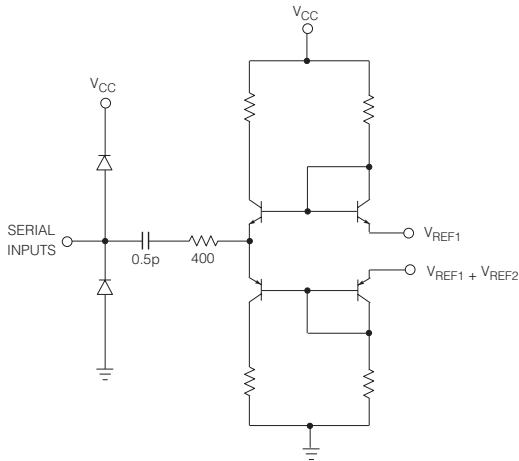


Figure 1 Input Circuit (Pins 11 and 12)

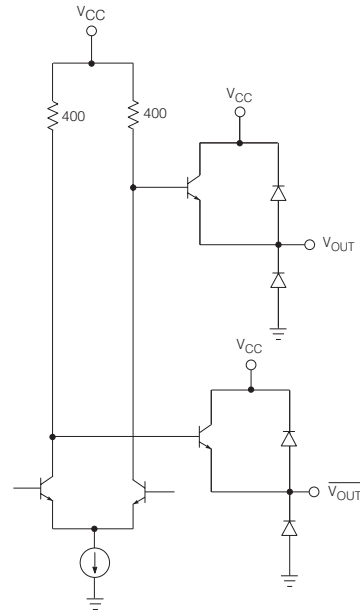
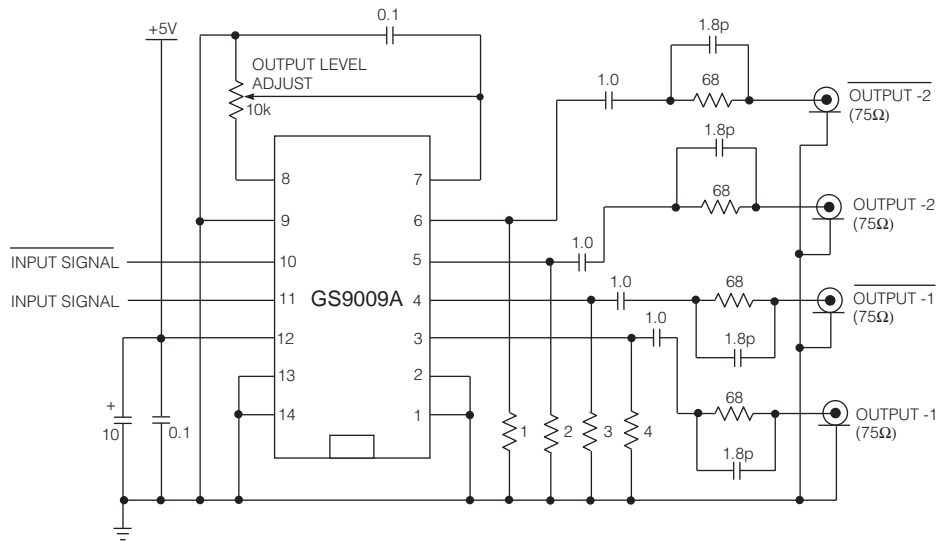
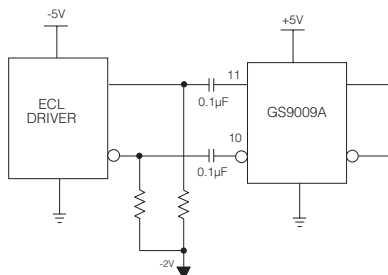


Figure 2 Output Circuit (Pins 3, 4 and 5, 6)



All resistors in ohms, all capacitors in microfarads unless otherwise stated.
Resistors marked 1, 2, 3 and 4 are 150 Ω each.

Figure 3 Typical Application Circuit



All resistors in ohms, all capacitors in microfarads unless otherwise stated.

Figure 4 Split Supply Interfacing

REVISION HISTORY

VERSION	ECR	DATE	CHANGES AND/OR MODIFICATIONS
0	132428	October 2003	New Document
1	134031	June 2004	Added lead-free and green information.

DOCUMENT IDENTIFICATION

PRELIMINARY DATA SHEET

The product is in a preproduction phase and specifications are subject to change without notice.

CAUTIONELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

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