HM-65642/883

8K x 8 Asynchronous CMOS Static RAM

May 2002

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Full CMOS Design**
- **Six Transistor Memory Cell**
- **Low Standby Supply Current 100µA**
- **Low Operating Supply Current. 20mA**
- **Fast Address Access Time 150ns**
- **Low Data Retention Supply Voltage 2.0V**
- **CMOS/TTL Compatible Inputs/Outputs**
- **JEDEC Approved Pinout**
- **Equal Cycle and Access Times**
- **No Clocks or Strobes Required**
- **Gated Inputs**
  - **No Pull-Up or Pull-Down Resistors Required**
- **Temperature Range -55°C to +125°C**
- **Easy Microprocessor Interfacing**
- **Dual Chip Enable Control**

Description

The HM-65642/883 is a CMOS 8192 x 8-bit Static Random Access Memory. The pinout is the JEDEC 28 pin, 8-bit wide standard, which allows easy memory board layouts which accommodate a variety of industry standard ROM, PROM, EPROM, EEPROM and RAMs. The HM-65642/883 is ideally suited for use in microprocessor based systems. In particular, interfacing with the Intersil 80C86 and 80C88 microprocessors is simplified by the convenient output enable ($\overline{G}$) input.

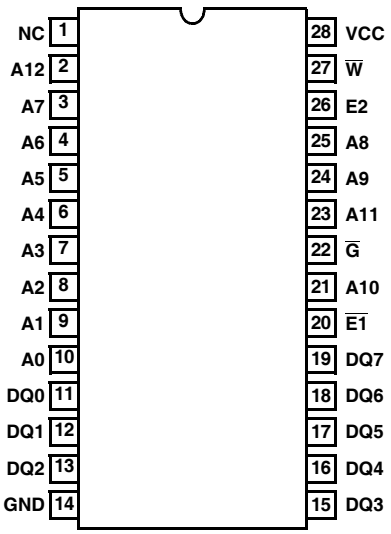
The HM-65642/883 is a full CMOS RAM which utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range.

Ordering Information

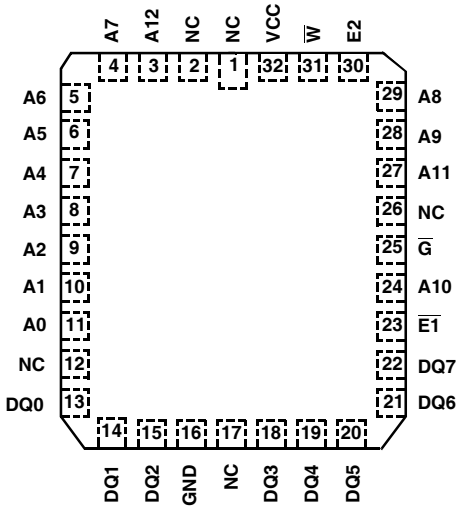
PACKAGE	TEMPERATURE RANGE	150ns/75µA	150ns/150µA	200ns/250µA	PKG. NO.
CERDIP	-55°C to +125°C	HM1-65642B/883	HM1-65642/883	HM1-65642C/883	F28.6
CLCC	-55°C to +125°C	HM4-65642B/883	HM4-65642/883	-	J32.A

Pinouts

HM-65642/883 (CERDIP)
TOP VIEW



HM4-65642/883 (CLCC)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
DQ	Data Input/Output
$\overline{E1}$	Chip Enable
E2	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
NC	No Connections
GND	Ground
VCC	Power

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage Applied for all Grades. . . . . GND -0.3V to VCC +0.3V
Typical Derating Factor . . . . . 5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	$45^oC/W$	$8^oC/W$
CLCC Package	$55^oC/W$	$10^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature. . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s). . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 101,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range. . . . . -55^oC to $+125^oC$
Input Low Voltage. . . . . -0.3V to +0.8V
Input High Voltage. . . . . +2.2V to VCC +0.3V
Data Retention Supply Voltage 2.0V
Input Rise and Fall Time . . . . . 40ns Max.

TABLE 1. HM-65642/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH 1	VCC = 4.5V, IO = -1.0mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 4.0mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	HM-65642B/883, HM-65642/883 VCC = 5.5V, $\overline{G}$ = 2.2V, VI/O = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	+1.0	µA
		HM-65642C/883 VCC = 5.5V, $\overline{G}$ = 2.2V, VI/O = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-2.0	+2.0	µA
Input Leakage Current	II	HM-65642B/883, HM-65642/883 VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	+1.0	µA
		HM-65642C/883 VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-2.0	+2.0	µA
Standby Supply Current	ICCSB1	HM-65642B/883 VCC = 5.5V, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	100	µA
		HM-65642/883 VCC = 5.5V, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	250	µA
		HM-65642C/883 VCC = 5.5V, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	400	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E1}$ = 2.2V or E2 = 0.8V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	5	mA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E1}$ =0.8V, E2 = 2.2V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	5	mA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = 5.5V, (Note 2), f = 1MHz, $\overline{E1}$ = 0.8V, E2 = 2.2V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	20	mA

TABLE 1. HM-65642/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Data Retention Supply Current	ICCDR	HM-65642B/883 VCC = 2.0V, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	75	µA
		HM-65642/883 VCC = 2.0V, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	150	µA
		HM-65642C/883 VCC = 2.0V, $\overline{E1}$ = VCC -0.3V or E2 = GND +0.3V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	250	µA
Functional Test	FT	VCC = 4.5V (Note 3)	7, 8A, 8B	$-55^oC \le T_A \le +125^oC$	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 5mA/MHz increase in ICCOP.
3. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH ≥ 1.5V, and VOL ≤ 1.5V.

TABLE 2. HM-65642/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS HM-65642B/883 MIN	LIMITS HM-65642B/883 MAX	LIMITS HM-65642/883 MIN	LIMITS HM-65642/883 MAX	LIMITS HM-65642C/883 MIN	LIMITS HM-65642C/883 MAX	UNITS
Read/Write/ Cycle Time	TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	150	-	200	-	ns
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	150	-	150	-	200	-
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	70	-	70	-	70	ns
Chip Enable Access Time	TE1LQV TE2HQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	150	-	150	-	200	ns
Write Recovery Time	TWHAX TE1HAX TE2LAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	10	-	10	-	ns
Chip Enable to End-of-Write	TE1LE1H TE2HE2L	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	90	-	90	-	120	-	ns
Address Setup Time	TAVWL TAVE1L TAVE2H	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Write Enable Pulse Width	TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	90	-	90	-	120	-	ns
Data Setup Time	TDVWH TDVE1H TDVE2L	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	60	-	60	-	80	-	ns

TABLE 2. HM-65642/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS						UNITS
					HM-65642B/883		HM-65642/883		HM-65642C/883		
					MIN	MAX	MIN	MAX	MIN	MAX	
Data Hold Time	TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	5	-	5	-	5	-	ns
	TE1HDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	10	-	10	-	ns
	TE2LDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	10	-	10	-	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1TTL equivalent load and CL ≥ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.

TABLE 3. HM-65642/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		
					MIN	MAX	UNITS
Output High Voltage	VOH2	VCC = 4.5V, IO = -100µA	1	$-55^oC \le T_A \le +125^oC$	VCC -0.4	-	V
Input Capacitance	CIN	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	12	pF
		VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	10	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1, 2	$T_A = +25^oC$	-	14	pF
		VCC = 4.5V, VI/O = GND or VCC, All Measurements Referenced to Device Ground	1, 3	$T_A = +25^oC$	-	12	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	50	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	ns
Chip Enable to Output ON	TE1LQX TE2HQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	10	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	ns
Chip Enable to Output in High Z	TE1HQZ	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	50	ns
	TE2LQZ		1	$-55^oC \le T_A \le +125^oC$	-	60	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	-	50	ns
Output Hold from Address Change	TAXQX	VCC = 4.5V and 5.5V	1	$-55^oC \le T_A \le +125^oC$	10	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only. For design purposes CIN = 6pF typical and CI/O = 7pF typical.
3. Applies to LCC device types only. For design purposes CIN = 4pF typical and CI/O = 5pF typical.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	GROUPS METHOD	SUBGROUPS
Interim Test 1	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test 1	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

Low Voltage Data Retention

Intersil CMOS RAMs are designed with battery backup in mind. Data Retention voltage and supply current are guaranteed over the operating temperature range. The following rules ensure data retention:

1. The RAM must be kept disabled during data retention. This is accomplished by holding the E2 pin between -0.3V and GND.
2. During power-up and power-down transitions, E2 must be held between -0.3V and 10% of VCC.
3. The RAM can begin operating one TAVAX after VCC reaches the minimum operating voltage of 4.5V.

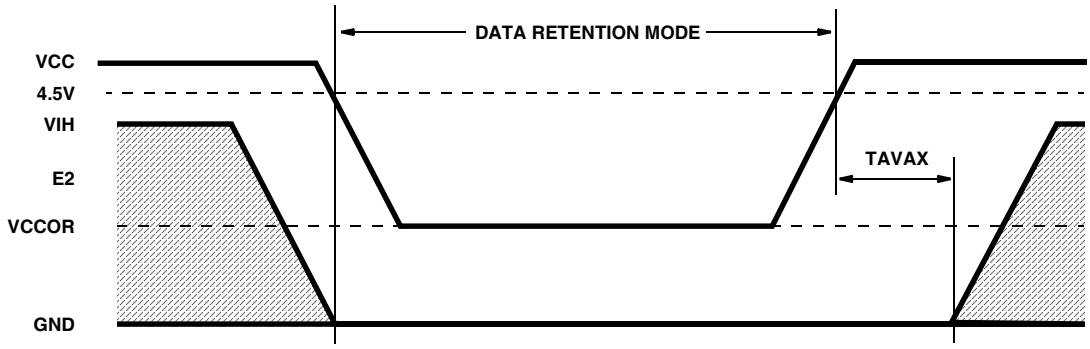


FIGURE 1. DATA RETENTION

Read Cycles

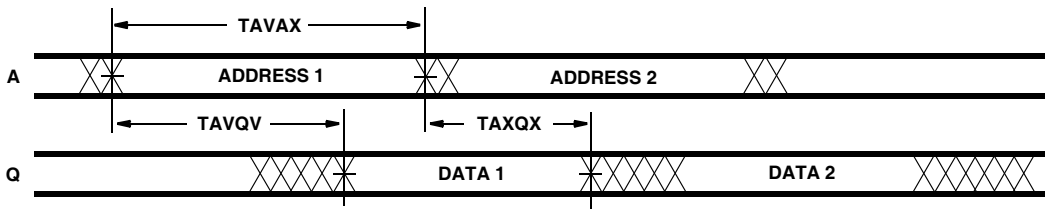


FIGURE 2. READ CYCLE I: $\overline{W}$, E2 HIGH; $\overline{G}$, $\overline{E1}$ LOW

Read Cycles

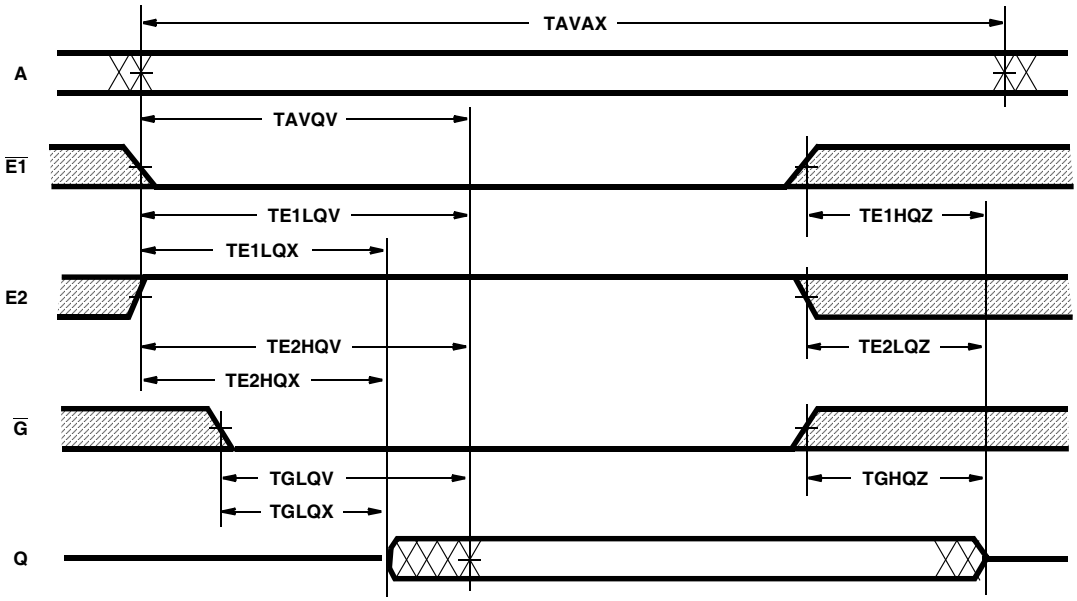


FIGURE 3. READ CYCLE II: $\overline{W}$ HIGH

Write Cycles

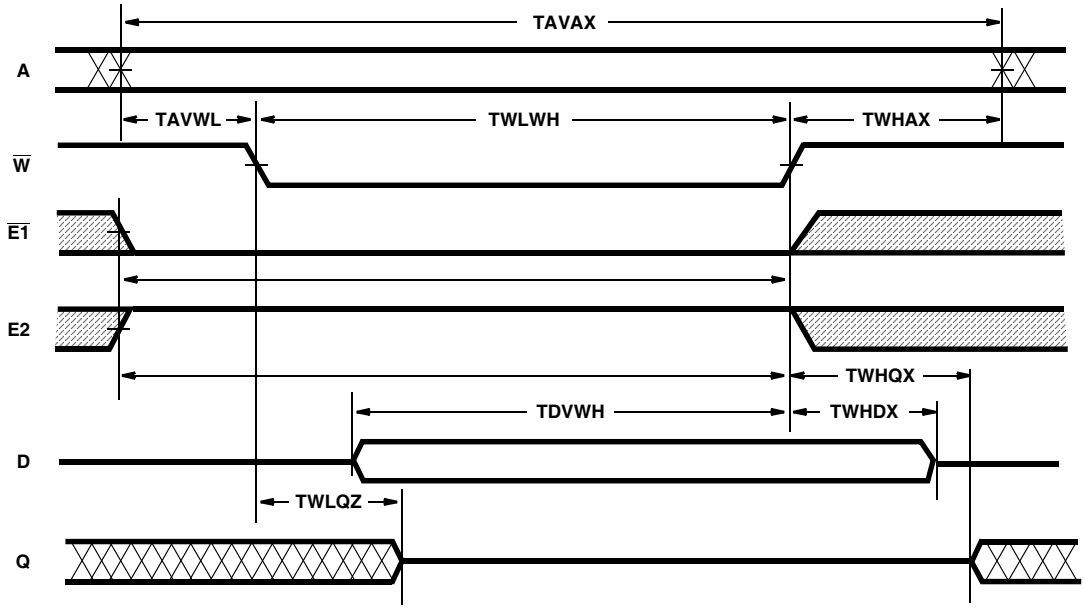


FIGURE 4. WRITE CYCLE I: LATE WRITE

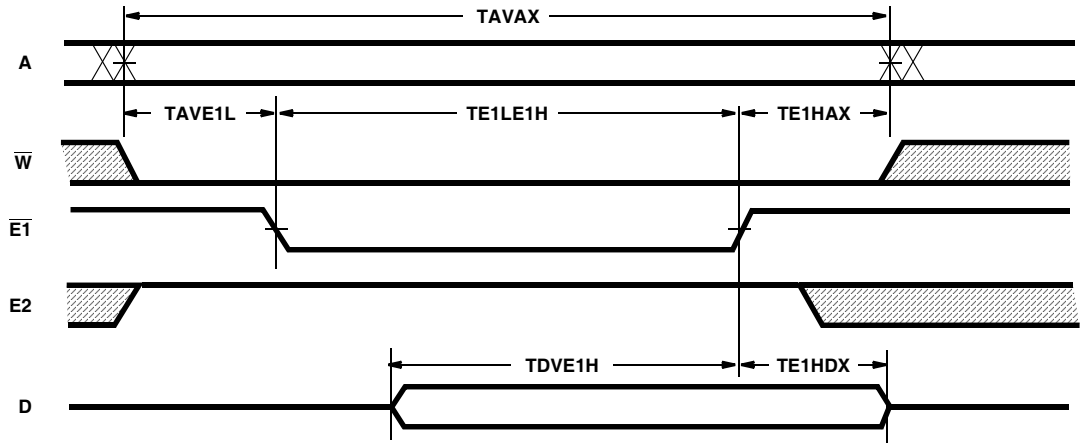


FIGURE 5. WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E1}$

Write Cycles

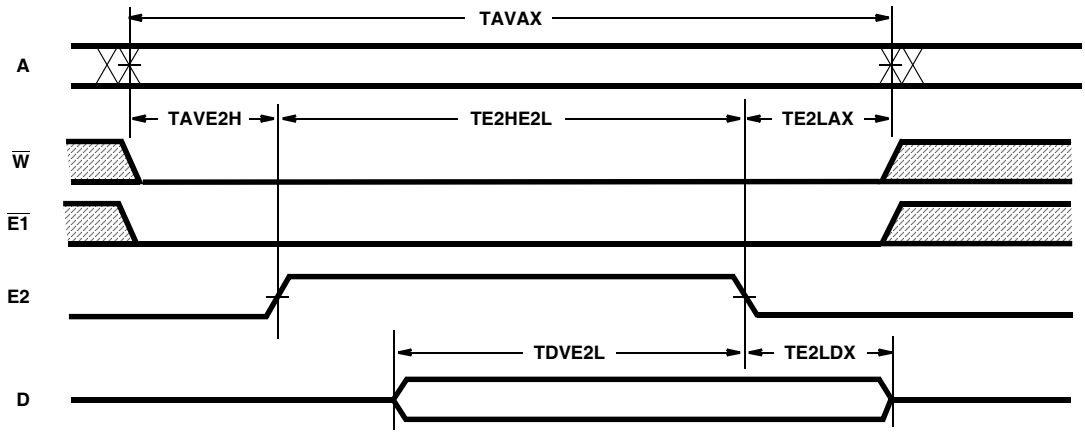
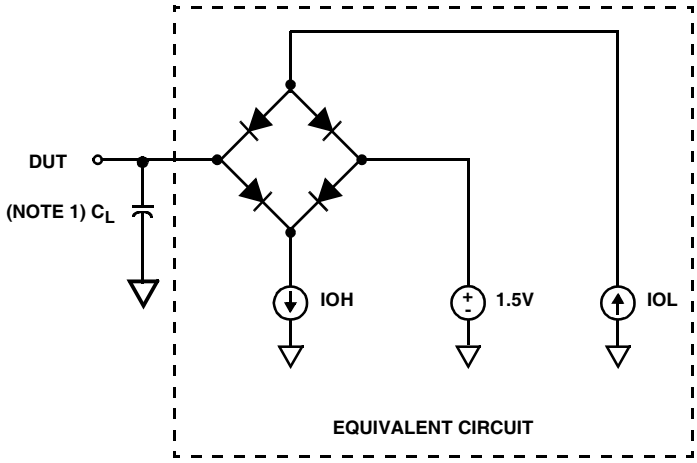


FIGURE 6. WRITE CYCLE III: EARLY WRITE - CONTROLLED BY E2

Test Circuit

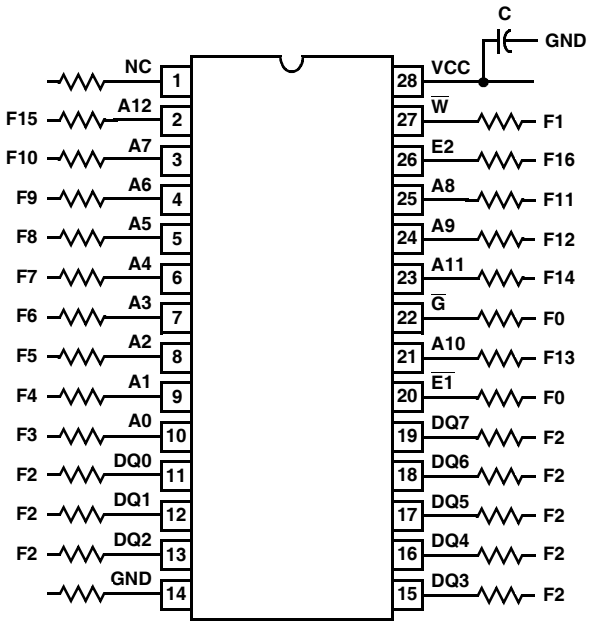


NOTE:

1. Test head capacitance.

Burn-In Circuits

HM-65642/883
CERDIP
TOP VIEW



NOTES:

F0 = 100kHz ±10%.

All resistors 47kΩ ±5%.

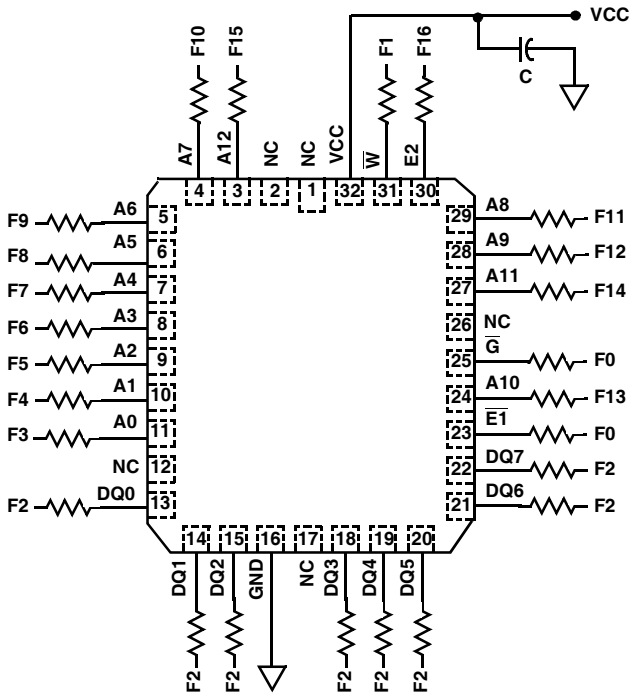
C = 0.01μF Min.

VCC = 5.5V ±0.5V.

VIH = 4.5V ±10%.

VIL = -0.2V to +0.4V.

HM-65642/883
CLCC
TOP VIEW



NOTES:

F0 = 100kHz ±10%.

C = 0.01μF Min.

VCC = 5.5V ±0.5V.

VIH = 4.5V ±10%.

VIL = -0.2V to +0.4V.

Die Characteristics

DIE DIMENSIONS:
274.0 x 302.8 x 19 ±1mils

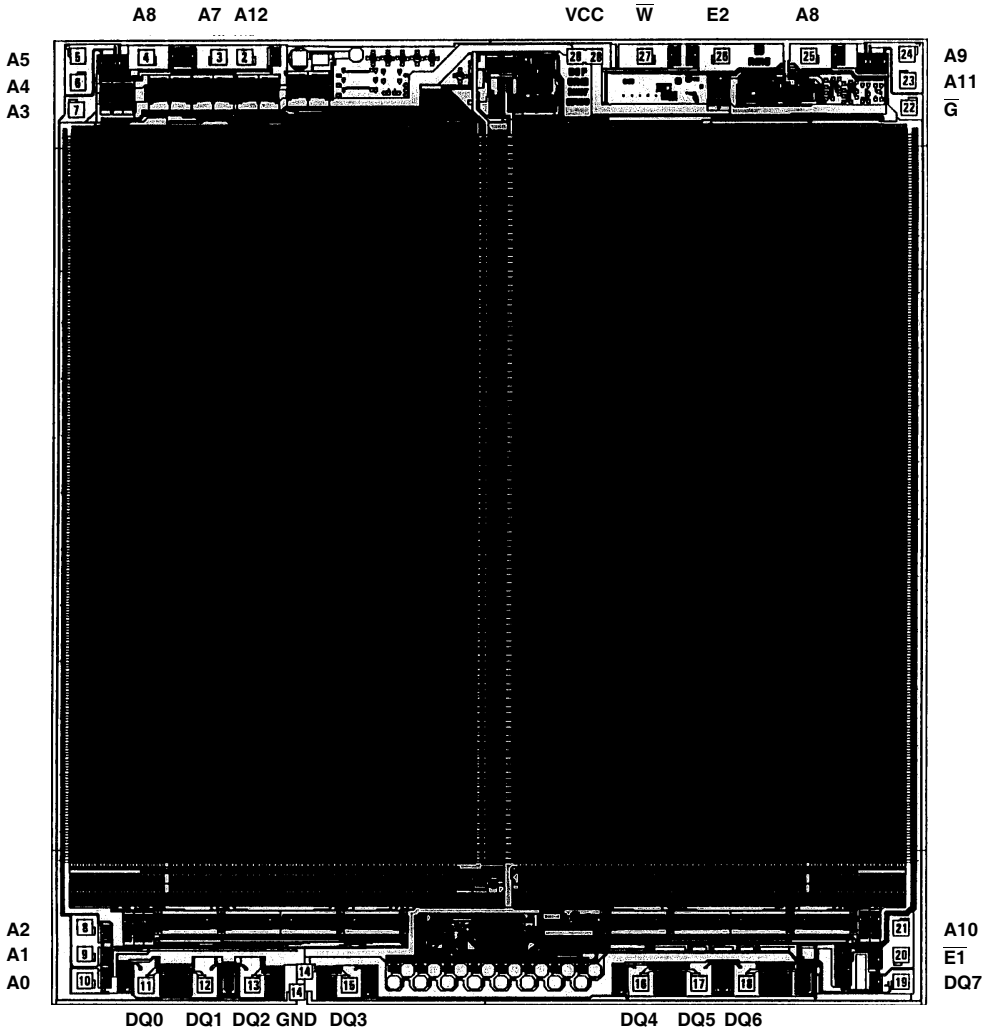
METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
0.9 x 10^5 A/cm^2

Metallization Mask Layout

HM-65642/883



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