MLX90323

4 – 20 mA Loop Sensor Interface with Signal Conditioning and EEPROM

Features and Benefits

- Programmable Sensor Interface IC with 4 to 20 mA current loop output
- Power supply from 6 to 35V_{DC}
- External or internal temperature sensor for compensating temperature errors

Application Examples

- Industrial pressure transducers.
- Strain gauges, accelerometers, position sensors, etc.
- Any bridge type sensor with current loop output.

Ordering code

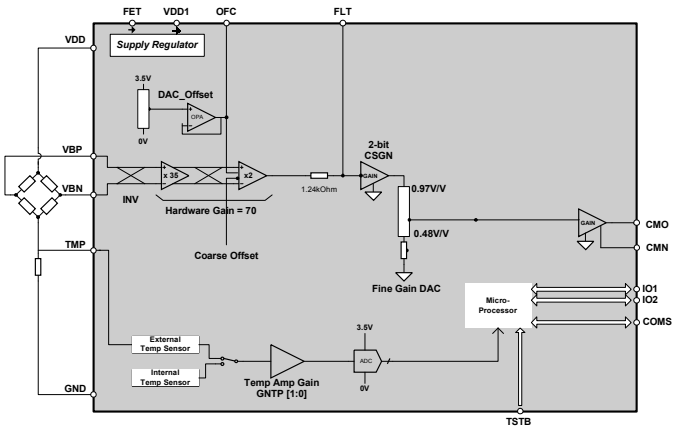
Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX90323	K	DF	AAA-000	TU
MLX90323	K	DF	AAA-000	RE

Legend:

Temperature Code: K for Temperature Range -40°C to +125°C
Package Code: DF for SOIC300Mil
Packing Form: RE for Reel, TU for Tube

Ordering example: MLX90323KDF-AAA-000-TU

1 Functional Diagram



2 General Description

The IC converts small changes of output voltage of full Wheatstone resistive bridge (caused by mechanical stimulus such as pressure, force, torque, light or magnetic field) to large changes of the IC output current.

It removes parasitic DC level (Offset) from the output bridge voltage and amplifies this signal certain times (Gain). Offset and Gain are temperature dependant, so the IC allows temperature compensation of bridge parasitic DC shift and sensitivity. Temperature can be measured either by internal or external (resistor) temperature sensor. The values of Offset and Gain and their temperature dependency are gotten during the calibration process and are stored in the EEPROM..

The IC has industry standard 4 – 20 mA current loop output interface and takes power directly from 2-wire signal line. The MLX90323 works properly over wide voltage range (from 6 to 35 V) at the signal line.

Table of Contents

3 Glossary of Terms

CMN	Current Mode Negative (supply connection)
CMO	Current Output
COMS	Communication, Serial
CR	Carriage Return
CSGN	Coarse Gain
CSOF	Coarse Offset
DACFnew	Filtered DAC value, new
DACFold	Filtered DAC value, old
DARDIS	DAC Resistor Disable
EOC	End Of Conversion flag bit
ETMI	Timer Interrupt Enable
ETPI	Enable Temperature Interrupt
FET	Field Effect Transistor
FG	Fixed Gain
FLT	Filter Pin
GNO	Gain and Offset adjusted digitized signal
GNOF	Gain, Offset
GNTP	Temperature Gain / Offset Coarse adjustment
HS	Hardware / Software limit
IFIX	fixed current output value
IINV	input signal invert command bit
ILIM	current limit
MODSEL	Mode Select
MUX	multiplexer
OFC	Offset Control
PLL	Phase Locked Loop
POR	Power On Reset
RX	receive
SAR	Successive Approximation Register
STC	start A/D conversion
Tdiff	temperature difference
Text	temperature, external
TMI	timer Interrupt
TMP	temperature signal
TPI	temperature interrupt
Tref	temperature reference
TSTB	test mode pin
TX	transmit
UART	Universal Asynchronous Receiver / Transmitter
VBN	bridge, positive, input
VBP	bridge, negative, input
V_{DD}	supply voltage
WCB	warn / cold boot
WDC	watch dog counter

4 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings

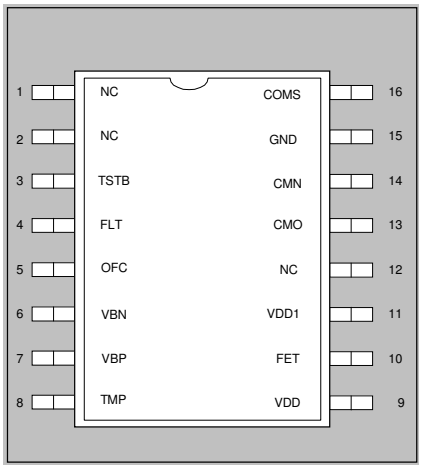
Supply voltage V_{DD} Max	6V
Supply voltage V_{DD} Min	4.5V
Supply voltage (operating), V_{DD1} Max	35V
Supply current, I_{DD}	3.5mA
Reverse voltage protection	-0.7V
Power dissipation, P_D	71mW
Operating temperature range, T_A	-40 to +125°
Storage temperature range, T_S	-55 to +150°C
Maximum junction temperature, T_J	150°C

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5 Pin Definitions and Descriptions

Table 2. Pin Description

Pin	Signal Name	Description
1,2	NC	Do not connect
3	TSTB	Test pin for Melexis production testing. (in normal application connected to VDD)
4	FLT	Filter pin; allows for connection of a capacitor to the internal analog path.
5	OFC	Offset control output. Provides access to the internal programmed offset control voltage for use with external circuitry. (unconnected when not used)
6,7	VBN,VBP	Bridge inputs, negative and positive.
8	TMP	Temperature sensor input. An external temperature sensor can be used in conjunction with the internal one. The external sensor can provide a temperature reading at the location of the bridge sensor.
9	V_{DD}	Regulated supply voltage. Used for internal analog circuitry to ensure accurate and stable signal manipulation.
10	FET	Regulator FET gate control. For generating a stable supply for the bridge sensor and internal analog circuitry (generates regulated voltage for VDD).
11	V_{DD1}	Unregulated supply voltage. Used for digital circuitry and to generate FET output.
12	NC	Do not connect
13	CMO	Current output.
14	CMN	Current negative rail. Current return path.
15	GND	Power supply return.
16	COMS	Serial communications pin. Bi-directional serial communication signal for reading and writing to the EEPROM.



6 General Electrical Specifications

Table 3. MLX90323 Electrical Specifications
DC operating parameters: T_A = -40 to 125°C, V_{DD1} = 6 to 35V_{DC} (unless otherwise specified).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Regulator & Consumption						
Input voltage range	V_{IN}	V_{DD1} (Regulator connected)	6		35	V
Supply current	I_{DD}	@ T_A = 100ºC		2.1		mA
Regulated supply voltage	V_{REG}		4.5	4.75	5.2	V
Regulated voltage temperature coefficient				-600		uV / °C
Supply rejection ratio	PSRR	V_{DD1} > 6V	90			dB
Instrumentation Amplifier						
Differential input range	VBP-VBN	IINV = 0	-2.88		8.38	$mV/V_{(VDD)}$
Differential input range	VBP-VBN	IINV = 1	-8.38		2.88	$mV/V_{(VDD)}$
Common mode input range		1/2(VBP+VBN)	38.0		65.0	%VDD
Common mode rejection Ratio	CMRR		60			dB
Hardware gain			69		84	V/V
Coarse offset control Range		CSOF[1:0] = 00	-4.37		-3.97	mV/V
		CSOF[1:0] = 01	-1.46		-1.09	mV/V
		CSOF[1:0] = 10	1.09		1.46	mV/V
		CSOF[1:0] = 11	3.97		4.37	mV/V
Fixed offset control range		High	1.71		2.29	mV/V
		Low	-2.00		-1.43	mV/V
IA chopper frequency				300		kHz
Gain Stage						
Coarse Gain Stage						
Coarse Gain (Fixed Gain = 1023)		CSGN = 00	1.05		1.17	V/V
		CSGN = 01	1.71		1.89	V/V
		CSGN = 10	2.77		3.06	V/V
		CSGN = 11	4.48		4.95	V/V

Fixed gain control range		0.480		0.970	V/V

Table 3. MLX90323 Electrical Specifications (continued)

Output Stage					
Fixed gain	R_{SENSE} = 24 ohm	8.4		9.3	mA/V
Output current CMO pin			27		mA
Current sense resistor			24		Ohms
Signal Path (General)					
Overall gain	Current sense res = 24Ω	284		2625	mA/V
Overall non-linearity		-0.25		0.25	%
Bandwidth (-3dB)	39 nF (FLT to GND)	2.8	3.5	4.2	KHz
Temperature Sensor & Amplifier					
Temperature sensor sensitivity			390		uV/ºC
Temperature sensor output voltage		70		380	mV
Input voltage range TMP pin	GNTP[1,0] = 00	207		517	mV
@ V_{DD} = 5.0V	GNTP[1,0] = 01	145		367	mV
	GNTP[1,0] = 10	101		263	mV
	GNTP[1,0] = 11	71		186	mV
DAC / ADC					
Resolution			10		Bit
On-Chip RC Oscillator and Clock					
Trimmed RC oscillator frequency		86.9	87.8	88.7	kHz
Frequency temperature coefficient			26		Hz/ºC
Clock Stability with temperature compensation over full temperature range		-3		+3	%
Ratio of f (microcontroller main clock and (RC oscillator)	TURBO = 0		7		
	TURBO = 1		28		

UART & COMS Pin					
UART baud rate	TURBO = 0		2400		Baud
	TURBO = 1		9600		Baud
COMS pin input levels	Low	0.3*V_{DD}			V
	High			0.7*V_{DD}	V
COMS Pin Output Resistance	Low		100		Ohms
	High		100		kOhms

7 Detailed General Description

7.1 Understanding 4-20mA current loop interface

MLX90323 IC is optimized for 4 - 20 mA industry standard current loop interface. The 4 - 20mA current loop shown in Figure 1 is a common method of transmitting sensor information in many industrial applications. Transmitting sensor information via a current loop is particularly useful when the information has to be sent to a remote location over long distances. The loop operation is straightforward: a sensor's output voltage is first converted to a proportional current, with 4mA normally representing the sensor's zero-level output, and 20mA representing the sensor's full-scale output. Then, a receiver at the remote end converts the 4-20mA current back into a voltage which in turn can be further processed by a controller module.

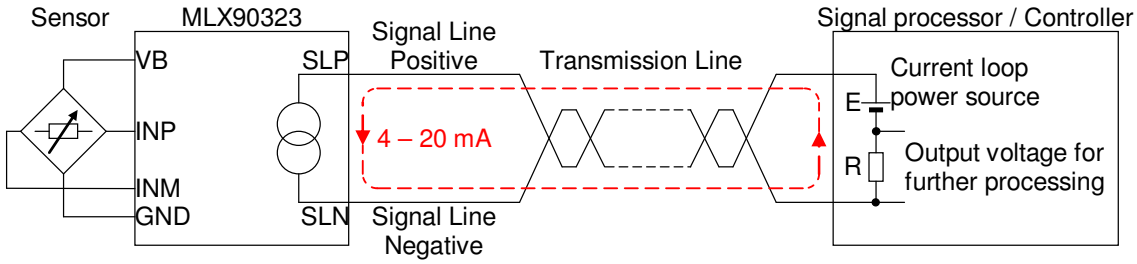


Figure 1. Current loop interface diagram

7.2 Analog features

Supply Regulator

A bandgap-stabilized supply-regulator is on-chip while the pass-transistor is external. The bridge-type sensor is typically powered by the regulated supply (typically 4.75V).

Oscillator

The MLX90323 contains a programmable on-chip RC oscillator. No external components are needed to set the frequency (87.8 kHz +/-1%). The MCU-clock is generated by a PLL (phase locked loop tuned for 614 kHz or 2.46 MHz) which locks on the basic oscillator.

The frequency of the internal clock is stabilized over the full temperature range, which is divided into three regions, each region having a separate digital clock setting. All of the clock frequency programming is done by Melexis during final test of the component. The device uses the internal temperature sensor to determine which temperature range setting to use.

Power-On Reset

The Power-On Reset (POR) initializes the state of the digital part after power up. The reset circuitry is completely internal. The chip is completely reset and fully operational 3.5 ms from the time the supply crosses 3.5 volts. The POR circuitry will issue another POR if the supply voltage goes below this threshold for 1.0 us.

Temperature Sensor

The temperature measurement, TPO, is generated from the external or internal temperature sensor. This is converted to a 10-bit number for use in calculating the signal compensation factors. A 2-bit coarse adjustment GNTP[1:0] is used for the temperature signal gain & offset adjustment.

7.3 Digital features

UART

The serial link is a potentially full-duplex UART. It is receive-buffered, in that it can receive a second byte before a previously received byte has been read from the receiving register. However, if the first byte is not read by the time the reception of the second byte is completed, the first byte will be lost. The UART's baud rate depends on the RC-oscillator's frequency and the "TURBO"-bit (see output port). Transmitted and received data has the following structure: start bit = 0, 8 bits of data, stop bit = 1.

Sending Data

Writing a byte to port 1 automatically starts a transmission sequence. The TX Interrupt is set when the STOP-bit of the byte is latched on the serial line.

Receiving Data

Reception is initialized by a 1 to 0 transition on the serial line (i.e., a START-bit). The baud rate period (i.e., the duration of one bit) is divided into 16 phases. The first six and last seven phases of a bit are not used. The decision on the bit-value is then the result of a majority vote of phase 7, 8 and 9 (i.e., the center of the bit).
Spike synchronization is avoided by de-bouncing on the incoming data and a verification of the START-bit value. The RX Interrupt is set when the stop bit is latched in the UART.

Timer

The clock of the timers TMI and TPI is taken directly from the main oscillator. The timers are never reloaded, so the next interrupt will take place 2x oscillator pulses after the first interrupt.

Watch Dog

An internal watch dog will reset the whole circuit in case of a software crash. If the watch dog counter is not reset at least once every 26 milliseconds (@ 2.46 MHz main clock), the microcontroller and all the peripherals will be reset.

Temperature Processing

Temperature reading controls the temperature compensation. This temperature reading is filtered as designated by the user. The filter adjusts the temperature reading by factoring in a portion of the previous value. This helps to minimize the effect of noise when using an external temperature sensor. The filter equation is:

If measured_temp > Temp_f(n) then
Temp_f(n+1) = Temp_f(n) + [measured_temp - Temp_f(n)] / [2^{n_factor}]
If measured_temp < Temp_f(n), then
Temp_f(n+1) = Temp_f(n) - [measured_temp - Temp_f(n)] [2^{n_factor}]

Temp_f(n+1) = new filtered temperature value
Temp_f(n) = previous filtered temperature value
Measured_temp = Value from temperature A to D
n_factor = Filter value set by the user (four LSB's of byte 25 of EEPROM), range 0-6.

The filtered temperature value, Temp_f, is stored in RAM bytes 58 and 59. The data is a 10 bit value, left justified in a 16 bit field.

7.4 Parameters calculation

The parameters OF and GN represent, respectively, offset correction and span control, while OFTCi and GNTCi represent their temperature coefficients (thermal zero shift and thermal span shift). After reset, the firmware continuously calculates the offset and gain DAC settings as follows: The EEPROM holds parameters GN, OF, OFTCi and GNTCi, where "i" is the gap number and can be $1 \leq i \leq 4$. The transfer function is described below.

GAIN
I_{out} = *FG * DAC_GAIN * CSGN[1:0] * {Vin+DAC_OFFSET+CSOF} * 8.85mA/V*

FG = Hardware Gain (~72V/V). Part of the hardware design, and not changeable
CSGN = Course Gain, part of byte 2 in EEPROM.
CSOF = Coarse Offset, part of byte 2 in EEPROM.
DAC_GAIN (new value) ~ GN[9:0] + [GNTCi * dT]
GN[9:0] = Fixed Gain, bytes 3 and 17 in EEPROM.
GNTCi = Gain TC for a given temperature segment I. GNTCiL and GNTCiH in EEPROM table.
dT = Temp. change within the appropriate gap

How to calculate gain in the first temp. gap?:

*DAC_GAIN = GN[9:0] - GNTC1 * (T1 – Temp_f1)*

How to calculate gain in the other temp. gaps?:

2nd gap: *DAC_GAIN = GN[9:0] + GNTC2 * (Temp_f2 – T1)*
3rd gap: *DAC_GAIN = DAC_GAIN2 + GNTC3 * (Temp_f3 – T2)*
4th gap: *DAC_GAIN = DAC_GAIN3 + GNTC4 * (Temp_f4 – T3)*

Where:
Temp_f = Filtered temp (previously described)

If GNTC1 > 2047 => DAC_GAIN
If GNTC2,3,4 > 2047 => DAC_GAIN ↓

[V/V]

$$(0.97-0.48)*\frac{GN[9:0]}{1023}+0.48 = DAC\_GAIN$$

OFFSET
DAC_OFFSET (new value) ~ OF[9:0]+[OFTCi* dT]
OF[9:0] = Fixed Gain, bytes 4 and 17 in EEPROM.
OFTCi = Offset for a given temperature segment I. OFTCiL and OFTCiH in EEPROM table.
dT = Temp. change within the appropriate gap.

Calculation of the offset for a given temperature segment is performed the same way as for the gain.

$$(1.83--1.57)*\frac{OF[9:0]}{1023}-1.57 = DAC\_OFFSET \quad \text{[mV/V]}$$

7.5 Communications

The MLX90323 firmware transfers a complete byte of data into and from the memory based on a simple command structure. The commands allow data to be read and written to and from the EEPROM and read from the RAM. RAM data that can be read includes the current digitized temperature. The commands are described below. Melexis provides setup software for programming the MLX90323.

UART Commands

The commands can be divided into three parts: (1) downloading of data from the ASIC, (2) uploading of data to the ASIC and (3) the reset command. UART configuration: start bit, 8 data bits, stop bit.
All the commands have the same identification bits. The two MSB's of the sent byte indicate the command while the last six MSB's designate the desired address. The commands are coded as followed:

Command	*Start bit*	*Bit7*	*Bit6*	*Bit5*	*Bit4*	*Bit3*	*Bit2*	*Bit1*	*Bit0*	*Stop Bit*
Read RAM	0	1	1	AD5	AD4	AD3	AD2	AD1	AD0	1
Write RAM	0	0	0	AD5	AD4	AD3	AD2	AD1	AD0	1
Read EEPROM	0	1	0	AD5	AD4	AD3	AD2	AD1	AD0	1
Write EEPROM	0	0	1	AD5	AD4	AD3	AD2	AD1	AD0	1
Reset	0	1	0	1	1	1	1	1	1	1

The addresses can include 0-63 for the RAM, 0-47 for the EEPROM, and 63 for the EEPROM, RESET Command (read).

Downloading Command

With one byte, data can be downloaded from the ASIC. The ASIC will automatically send the value of the desired byte.

Uploading Command

Writing to the RAM or EEPROM involves a simple handshaking protocol in which each byte transmitted is acknowledged by the firmware. The first byte transmitted to the firmware includes both command and address. The firmware acknowledges receipt of the command and address byte by echoing the same information back to the transmitter. This "echo" also indicates that the firmware is ready to receive the byte of data to be stored in RAM or EEPROM. Next, the byte of value to be stored is transmitted and, if successfully received and stored by the firmware, is acknowledged by a "data received signal," which is two bytes of value BCh. If the "data received signal" is not observed, it may be assumed that no value has been stored in RAM or EEPROM.

Reset Command

Reading the address 63 of the EEPROM resets the ASIC and generates a received receipt indication. Immediately before reset, the ASIC sends a value of BCh to the UART, indicating that the reset has been received.

EEPROM Data

All user-settable variables are stored in the EEPROM within the MLX90323. The EEPROM is always re-programmable. Changes to data in the EEPROM do not take effect until the device is reset via a soft reset or power cycle. 12 bit variables are stored on 1.5 bytes. The 4 MSB's are stored in a separate byte and shared with the four MSB's of another 12-bit variable.

Clock Temperature Stabilization

To provide a stable clock frequency from the internal clock over the entire operating temperature range, three separate clock adjust values are used. Shifts in operating frequency over temperature do not effect the performance but do, however, cause the communications baud rate to change.
The firmware monitors the internal temperature sensor to determine which of three temperature ranges the device currently is in. Each temperature range has a factory set clock adjust value, ClkTC1, ClkTC2, and ClkTC3. The temperature ranges are also factory set. The Ctemp1 and Ctemp2 values differentiate the three ranges. In order for the temperature A to D value to be scaled consistently with what was used during factory programming, the CLKgntp (temperature amplifier gain) valued is stored. The Cadj value stored in byte 1 of the EEPROM is used to control the internal clock frequency while the chip boots.

Unused Bytes

There are eight unused bytes in the EEPROM address map. These bytes can be used by the user to store information such as a serial number, assembly date code, production line, etc. Melexis doesn't guarantee that these bytes will be available to the user in future revisions of the firmware.

EEPROM Checksum

A checksum test is used to ensure the contents of the EEPROM. The eight bit sum of all of the EEPROM addresses should have a remainder of 0FFh when the checksum test is enabled (mode byte). Byte 47 is used to make the sum remainder totals 0FFh. If the checksum test fails, the output will be driven to a user defined value, Faultval. When the checksum test is enabled, the checksum is verified at initialization of RAM after a reset.

RAM Data

All the coefficients are compacted in a manner similar to that used for the EEPROM. They are stored on 12 bits (instead of keeping 16 bits for each coefficient). All the measurements are stored on 16 bits. The user must have access to the RAM and the EEPROM, while interrupt reading of the serial port. Therefore, bytes must be kept available for the return address, the A-accu and the B-accu, when an interrupt occurs. The RAM keeps the same structure in the both modes.

Table 4. Examples of Fixed Point Signed Numbers

Decimal Value	Hexadecimal Equivalent	Fixed Point Signed Number Equivalent
0	0000h	+0.00
1023	3FFh	+0.9990234
1024	400h	+1.000
2047	7FFh	+1.9990234
2048	800h	-0.000
3071	0BFFh	-0.9990234
3072	0C00h	-1.000
4095	0FFFh	-1.9990234

Data Range

Various data are arranged as follows:
Temperature points: 10 bits, 0-03FF in high-low order.
GN1: 10 bits, 0-03FF in high-low order.
OF1: 10 bits, 0-03FF in high-low order.
GNTCi: signed 12 bits (with MSB for the sign), [-1.9990234, +1.9990234].
OFTCi: signed 12 bits (with MSB for the sign), [-1.9990234, +1.9990234].

8 Temperature compensation

The MLX90323's temperature compensation algorithm is piece-wise with up to 4 temperature segments, see figure 2. Within each temperature segment ('gap'), the correction is a first order calculation. There are separate temperature coefficients for gain and offset. The first temperature gap is slightly different than the other three. The compensation is based on the temperature difference between the current temp and the T1 point (the upper end of the gap). The other gaps use the lower end of the gap to measure the temperature difference. For instance in the second gap, the temperature difference is current temperature minus T1. This difference has to be accounted for in the compensation procedure.

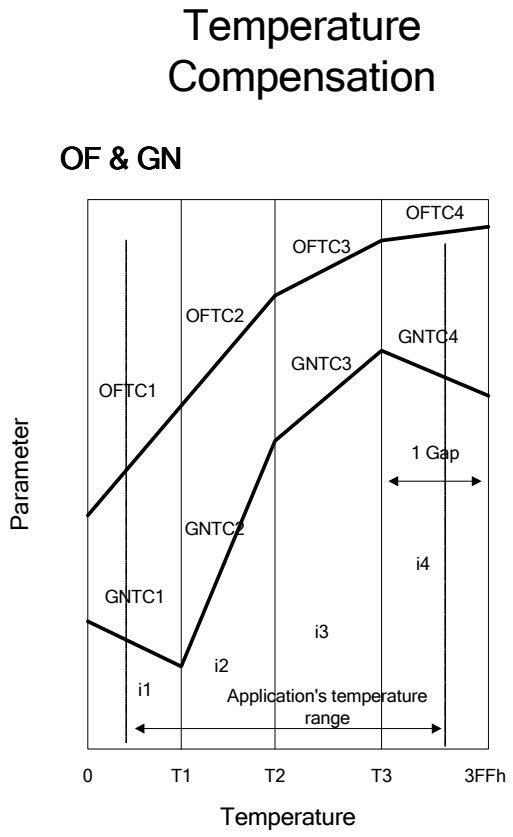


Figure 2. Temperature Compensation.

Temperature Gaps

There are four temperature gaps possible with the MLX90323. The gaps are defined with respect to the filtered digitized temperature value saved in RAM locations 58 and 59. The first temperature gap is always bound at the low end by a digitized temperature value of zero. The fourth temperature gap is bound at the high end by a digitized temperature value of 1023_{10} ($3FF_{hex}$).

Whenever fewer than four gaps are used, the last gap should have an upper bound of 1023_{10}. This is to ensure that if the temperature exceeds the last point it won't enter into an undefined temperature gap.

Temperature Points

The temperature points T1, T2 and T3 are defined by the user to differentiate between the four possible temperature compensation ranges. The low endpoint T0 is defined as the minimum digitized filtered temperature value, zero. This means that the coefficients for the first gap, OFTC1 and GNTC1, will apply to the signal until the digitized filtered temperature reaches zero. The high endpoint T4 is defined as the maximum digitized filtered temperature value, 1023_{10}. This means that the coefficients for the last gap, OFTC4 and GNTC4 will apply to the signal from the T3 point and up until the digitized filtered temperature reaches its maximum, 1023_{10}.

When defining these points, the number that is used is simply copied from the 'Temp Value' box (see *"MLX90323_software_descroption.pdf"*) at the desired temperature (contents of ram locations 58 and 59).

GNTC

The GNTC values are the gain temperature compensation values for each of the four temperature gaps, GNCT1, GNTC2, GNTC3, and GNTC4. These values are used to adjust the signal up or down based on the relative temperature within a particular gap. Mathematically this is represented by the following equation:

$$DAC\_GAIN = CSGN * \{GN[9:0] + [GNTCi * \Delta Ti]\}$$

Where:

ΔTi = (T1 – temp_f) for gap 1;
ΔTi = (temp_f – T_{i-1}) for gaps 2,3,and 4;
Temp_f = Filtered temperature;
DAC_GAIN = The digital value that adjusts the gain on the gain amplifier;
Ti = Temperature segment point i = 2, 3, or 4;
GNTCi = Gain TC for a given temperature segment I;
CSGN = Course Gain;
GN[9:0] = Fixed Gain (doesn't change with temperature).

The GNTC and OFTC values are 12 bit fixed point signed numbers (see table 4). That means that the most significant bit is a sign bit. The next bit is one or zero (whole number). The remaining 10 bits are to the right of the decimal point. This gives the variable the range of –1.9990234 to +1.9990234. The table below shows how the fixed point numbers are represented as the binary number progresses from 0 to 4095.

OFTC

The OFTC values are the offset temperature compensation values for each of the four temperature gaps, OFCT1, OFTC2, OFTC3, and OFTC4. These values are used to adjust the signal's offset up or down based on the relative temperature within a particular gap. The offset adjustment is additive from one gap to the next. That is the offset adjustment for the fourth gap is added to the total offset adjustment of the third gap which is also added to the total offset adjustment of the second gap. Mathematically this is represented by the following equation:

For the first temperature gap:

$$DAC\_OFFSET = OF[9:0] + OFTCi * (T1 - Temp\_f)$$

For the second temperature gap:

$$DAC\_OFFSET = OF[9:0] + OFTC2 * (Temp\_f - T2)$$

For the third temperature gap:

$$DAC\_OFFSET = OF[9:0] + [OFTC2 * (T2-T1)] + OFTC3 * (Temp\_f - T3)$$

For the fourth temperature gap:

$$DAC\_OFFSET = OF[9:0] + [OFTC2 * (T2-T1)] + [OFTC3 * (T3 - T2)] + OFTC4 * (Temp\_f - T4),$$

Where OF[9:0] = Fixed offset

9 Calibration

9.1 Baseline Calibration

The baseline calibration involves setting the operating modes and temperature gain along with the coarse and fixed gain and offset.

The operating modes are turbo mode, internal or external temperature sensor, and checksum test. The checksum test, if used, should be enabled after all other settings are complete.

The invert signal bit swaps the differential inputs to the signal path. This has the same effect as swapping the connections to the VBP and VBN pins of the chip.

Temperature amplifier gain, GNTP, should be set such that the analog converter doesn't under-run or over-run at the temperature extremes. When using the internal temperature sensor over the full temperature span of the device (-40C to +125°C) typically a GNTP setting of 2 will work. When using an external temperature sensor the voltage on the TMP pin must stay within the ranges as described in the datasheet. The more of the voltage range used the greater the temperature compensation adjustment range will be.

The coarse gain and fixed gain should be set before the coarse offset and fixed offset. Gain and offset are inter-related, the offset is multiplied by the gain. It is much easier to program the gain first then offset. It may be necessary to make some minor adjustment to the coarse offset settings before adjusting the gain. This is only needed if the output clips at either high end or low end. It is difficult to precisely calculate the offset and gain values. The amplifier circuitry within the chip uses resistors implemented in silicon. These resistors have around a 20% tolerance, thus the gain and offset will vary from chip to chip. Each chip is tested to provide a gain and offset adjustment capability within a specified range. For calculations a typical value can be taken.

9.2 Temperature calibration

The temperature compensation capability of the MLX90323 is piece-wise with first order compensation in each segment (gap). The compensation is based on the difference between the current digitized filtered temperature and the appropriate temperature point. The equations have been previously described. The first temperature gap is slightly different than the other three. The first gap uses the temperature difference between the current temperature and the T1 temperature point (the upper end of the temperature gap). The second temperature gap also uses the T1 point for determining the temperature differences (the low end of the second gap). The third and fourth gaps also use the temperature point at the low end of their gap. This means that programming the temperature compensation for the first gap is slightly different than the other gaps. The compensation coefficients for the first gap (OFTC1 and GNTC1) apply to digitized filtered temperature values from T1 down to zero. The fourth gap coefficients apply to digitized filtered temperature range from T3 to 1023 (decimal).

The temperature points T1 thru T3 should always be in increasing order from T1 to T2 to T3. If the temperature sensor has increasing signal with increasing temperature then the compensation procedure is intuitively easy. This is the case with the internal temperature sensor. If the temperature sensor has

decreasing signal with increasing temperature then the compensation will start at a hotter temperature and go towards cold. The procedure below is written with regard to the filtered digitized temperature not the real physical temperature.

9.3 Calibration procedure

1) Set the desired operating mode and number of gaps. It is also helpful to set T2 and T3 to 1023.

2) At the T1 temperature do a baseline calibration, the span then the offset by using CSGN[1:0] and GN[9:0] then CSOF[1:0] and OF[9:0]. The T1 temperature is somewhat arbitrary, typically its room temperature. If the temperature sensor goes down with increasing temperature then the T1 value will be towards the high end of the application's temperature range. Update the Temp value. Copy the digitized temperature reading to the T1 box. If one temperature gap is desired then T1 will be the highest digitized temperature value.

3) Lower the temperature to the lowest operating temperature and recalibrate the output using GNTC1 and OFTC1 only. If the temperature sensor goes down with increasing temperature then raise the temperature to its maximum value and re-calibrate the output using GNTC1 and OFTC1. Do not change the T1, OF, or GN values.

4) Raise the temperature until the second temperature point, T2. If the temperature sensor goes down with increasing temperature then lower the temperature to the T2 value. This point may be arbitrary and can be based on how far the output has deviated from it's desired value. Re-calibrate the sensor by adjusting GNTC2 and OFTC2 only.

5) Update the Temp value displayed on the screen. Copy the digitized temperature value to the T2 box. This must happen AFTER step 4.

6) Repeat steps 4 and 5 for T3 and setting GNTC3, OFTC3. T1, T2, and T3 must be in ascending order.

7) For the last temperature gap, raise the temperature to the highest operating temperature point and re-calibrate the output using GNTC4 and OFTC4. There is no T4, it is assumed to be 1023 (the maximum value of the digitized filtered temperature).

For less than four temperature gaps the last temperature point should be set to 1023. This means that the last gap extends out to the end of the temperature range.

10 EEPROM and RAM byte definitions

Table 5. EEPROM Byte Definitions

Byte	Designation	Note
0	Turbo mode, temp selection	Bit 0: must always be set to “1” Bit 1: (0 = internal temp, 1 = external temp) Bit 3: (0 = Turbo mode not active, 1 = active) Bit 2,4,5,6: must always be set to “0” Bit 7: (0 = EEPROM Checksum test inactive, 1 = active)
1	Cadj	Controls system clock during boot.
2	Coarse Control	Contents described in Table 6.
3	GN1L	The eight LSB's of the Fixed Gain, GN[7:0].
4	OF1L	The eight LSB's of Fixed Offset OF[7:0].
5	GNTC1L	The eight LSB's of the first gain TC GNTC1[7:0].
6	OFTC1L	The eight LSB's of the first offset TC OFTC1[7:0].
7	TR1L	The eight LSB's of the first temperature point, T1[7:0].
8	GNTC2L	The eight LSB's of the second gain TC GNTC2[7:0].
9	OFTC2L	The eight LSB's of the second offset TC OFTC2[7:0].
10	TR2L	The eight LSB's of the second temperature point T2[7:0].
11	GNTC3L	The eight LSB's of the third gain TC GNTC3[7:0].
12	OFTC3L	The eight LSB's of the third offset TC OFTC3[7:0]
13	TR3L	The eight LSB's of the third temperature point T3[7:0].
14	GNTC4L	The eight LSB's of the fourth gain TC GNTC4[7:0].
15	OFTC4L	The eight LSB's of the fourth offset TC OFTC4.
16	-	Reserved

Table 5. EEPROM Byte Definitions (continued)

Byte	Designation	Note	
		Upper four bits	**Lower four bits**
17	GN1[9:8] OF1[9:8]	Two MSB's of fixed gain GN[9:8].	Two MSB's of fixed offset OF[9:8]
18	GNTC1[11:8] OFTC1[11:8]	Four MSB's of first gain TC GNTC1[11:8].	Four MSB's of the first offset TC OFTC1[11:8].
19	TR1[9:8] GNTC2[11:8]	Two MSB's, first temperature point T1[9:8]	Four MSB's, second gain TC GNTC2[11:8]
20	OFTC2[11:8] TR2[9:8]	Four MSB's second offset TC OFTC2[11:8]	Two MSB's second temperature point T2[9:8]
21	GNTC3[11:8] OFTC3[11:8]	Four MSB's third gain TC GNTC3[11:8]	Four MSB's third offset TC OFTC3[11:8]
22	TR3[9:8] GNTC4[11:8]	Two MSB's third temperature point t3[9:8]	Four MSB's fourth gain TC GNTC4[11:8]
23	OFTC4[11:8] -	Four MSB's fourth offset TC	reserved
24	PNB_TNB	Number of temperature gaps, see Table 7	
25	n_factor	Temperature filter coefficient, four LSB's. Four MSB's must all be zero.	
26 - 31	reserved	reserved.	
32	ClkTC1	Value of Cadj at low temperature (Don’t change; factory set).	
33	ClkTC2	Value of Cadj at mid temperature (Don’t change; factory set).	
34	ClkTC3	Value of Cadj at high temperature Don’t change; factory set).	
35	Ctemp1	First Cadj temperature point, eight MSB’s of the 10 bit internal temperature value (set at factory; do not change).	
36	Ctemp2	Second Cadj temperature point, eight MSB’s of the 10 bit internal temperature value (set at factory; do not change).	
37-38	Not used	These bytes are not used and are available to the user.	
39	CLKgntp	Setting for temperature amplifier for clock temperature adjustment temperature reading (factory set, do not change).	

Table 5. EEPROM Byte Definitions (continued)

Byte	Designation	Note
40-41	Faultval	Value sent to output if checksum test fails is a 10 bit value.
42-46	Not Used	These bytes are not used and are available to the user.
47	Checksum	EEPROM checksum; value needed to make all bytes add to 0FFh. Must be set by user if checksum test is active.

Table 6. Bit Definitions, Coarse Control , Byte 2

Bit	Symbol	Function
7	IINV	Invert signal sign.
6	GNTP1	Gain & offset of temperature amplifier.
5	GNTP0	GNTP = 0 to 3.
4	CSOF 1	Coarse offset of signal amplifier.
3	CSOF 0	CSOF = 0 to 3.
2	-	Coarse gain of signal amplifier. CSGN = 0 to 3.
1	CSGN1	
0	CSGN0	

Table 7. PNB_TNB Bit Definition

Maximum number of temperature gaps	Maximum number of signal gaps
Fixed Gain and fixed Offset	5 Gaps
2 Gaps	3 Gaps
3 Gaps	2 Gaps
4 Gaps	Fixed signal

Table 8. RAM Byte Definitions

Byte	Functions	Remarks	
0	Mode byte		
1	GN1L	Fixed gain number (8LSB).	
2	OF1L	Fixed offset number (8LSB).	
3	GNTC1L	First gain TC (8LSB).	
4	OFTC1L	First offset TC (8LSB).	
5	TR1L	First temperature point.	
6	GNTC2L	Second gain TC.	
7	OFTC2L	Second offset TC.	
8	TR2L	Second temperature point.	
9	GNTC3L	Third gain TC.	
10	OFTC3L	Third offset TC.	
11	TR3L	Third temperature point.	
12	GNTC4L	Fourth gain TC.	
13	OFTC4L	Fourth offset TC.	
14	-	reserved	
		Upper four bits	**Lower four bits**
15	GN1[9:8] OF1[9:8]	Two MSB's of fixed gain GN[9:8].	Two MSB's of fixed offset OF[9:8].
16	GNTC1 [11:8] OFTC1[11:8]	Four MSB's of first gain TC GNTC1[11:8].	Four MSB's of the first offset TC OFTC1[11:8]
17	TR1[9:8] GNTC2[11:8]	Two MSB's, first temperature point T1[9:8]	Four MSB's, second gain TC GNTC2[11:8]
18	OFTC2[11:8] TR2[9:8]	Four MSB's, second offsetTC OFTC2[11:8]	Two MSB's, second temp. point T2[9:8]

Table 8. RAM Byte Definitions (continued)

Byte	Functions	Remarks
19	GNTC3[11:8] OFTC3[11:8]	Four MSB's, Third Gain TC GNTC3[11:8] Four MSB's Third Offset TC OFTC3[11:8]
20	TR3[9:8] GNTC4[11:8]	Two MSB's, third temperature point t3[9:8] Four MSB's, Fourth Gain TC GNTC4[11:8]
21	OFTC4[11:8] -	Four MSB's Fourth Offset TC OFTC4[11:8] reserved
22	PNB_TNB	Same as EEPROM.
23	n_factor	Temperature filter coefficient 4 LSB's, 4 MSB = 0
24	Not Used	
25-26	GN	Offset Ordinate of the current gap.
27-28	OF	Gain Ordinate of the current gap.
29	Taddress	4 bits for the max. temperature address of the current gap; 4 bits for the min. temperature address of the current gap.
35-36	A_16	16 bits A Register.
37-38	B_16	16 bits B Register.
39-42	RESULT_32	32 bits result (for 16 bit multiplication).
43-44	Tempo1	Measured temperature, internal or external, and temporary variable 1.
45	Tempo2	Temporary variable 2.
46-47	-	Reserved
48	Coms_backup	Address saved when command is send.
49	P3_copy	Port 3 setting copy.
50	Adsav1	Address saved at interrupt.
51-52	Aaccsav	A-Accumulators saved at interrupt.
53	Baccsav	B-Accumulators saved at interrupt.
54-55	DAC_gain	DAC gain (GN).
56-57	DAC_offset	DAC offset (OF).
58-59	Temp_f	Filtered temperature. This is a 10 bit number that is left justified in a 16 bit field.
60-61	-	Reserved
62-63	Adsav2	Address saved when call.

Note: Because of space considerations, the measured temperature can't be kept in the RAM at all times. If the measured temperature is to be available, the temperature filter variable, *n_factor*, must be set to 6.

11 Unique Features

Special Information

The output of the sensor bridge is amplified via offset and gain amplifiers and then converted to the correct output signal form in one of the output stages.
The sensitivity and offset of the analog signal chain are defined by numbers passed to the DAC interfaces from the microcontroller core (GN[9:0] and OF[9:0]). The wide range of bridge offset and gain is accommodated by means of a 2-bit coarse adjustment DAC in the offset adjustment (CSOF[1:0]), and a similar one in the gain adjustment (CSGN[1:0]). The signal path can be directed through the processor for digital processing.

Programming and Setup

The MLX90323 needs to have the compensation coefficients programmed for a particular bridge sensor to create the sensor system. Programming the EEPROM involves some minimal communications interface circuitry, Melexis setup software, and a PC. The communications interface circuitry is available in a development board. This circuitry communicates with the PC via a standard RS-232 serial communications port.

12 Application Information

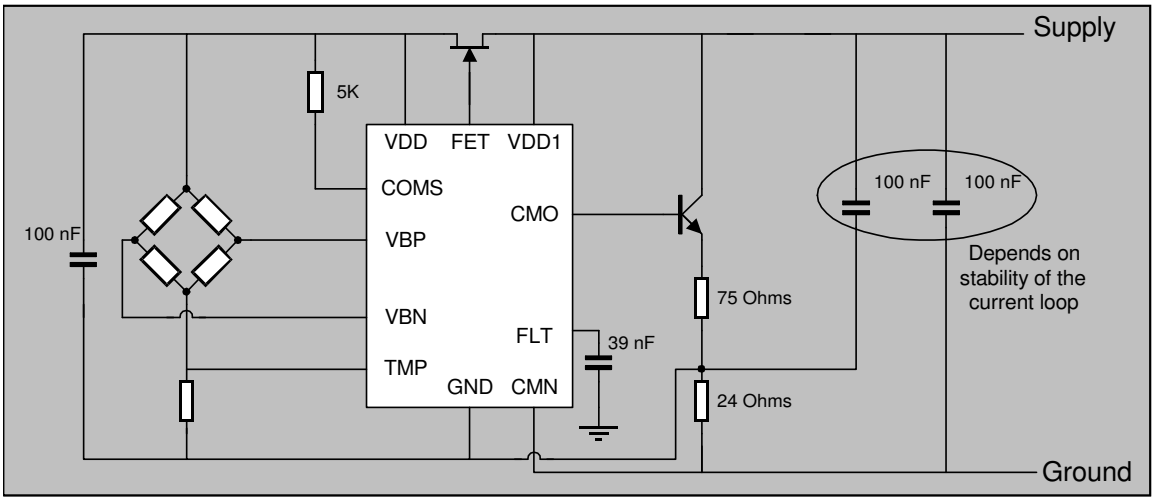


Figure 3. Typical application schematic

13 Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

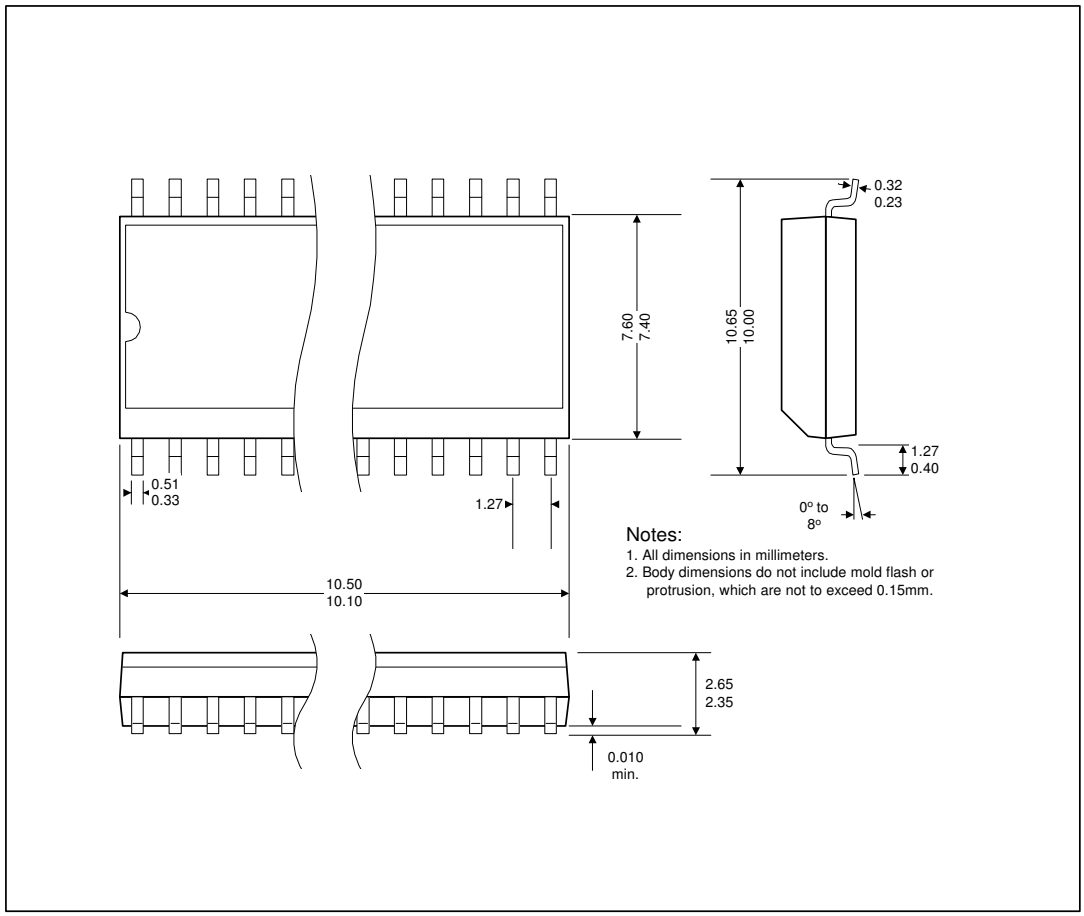
The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website:
http://www.melexis.com/quality.aspx

14 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

15 Package Information



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Or for additional information contact Melexis Direct:

Europe, Africa, Asia:
Phone: +32 1367 0495
E-mail: sales_europe@melexis.com

America:
Phone: +1 248 306 5400
E-mail: sales_usa@melexis.com

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