

# EEPROM PROGRAMMABLE CLOCK GENERATOR

# IDT5V49EE702

## Description

The IDT5V49EE702 is a programmable clock generator intended for high performance data-communications, telecommunications, consumer, and networking applications. There are four internal PLLs, each individually programmable, allowing for four unique non-integer-related frequencies. The frequencies are generated from a single reference clock. The reference clock can come from one of the two redundant clock inputs. A glitchless automatic or manual switchover function allows any one of the redundant clocks to be selected during normal operation.

The IDT5V49EE702 is in-system, programmable and can be programmed through the use of I<sup>2</sup>C interface. An internal EEPROM allows the user to save and restore the configuration of the device without having to reprogram it on power-up.

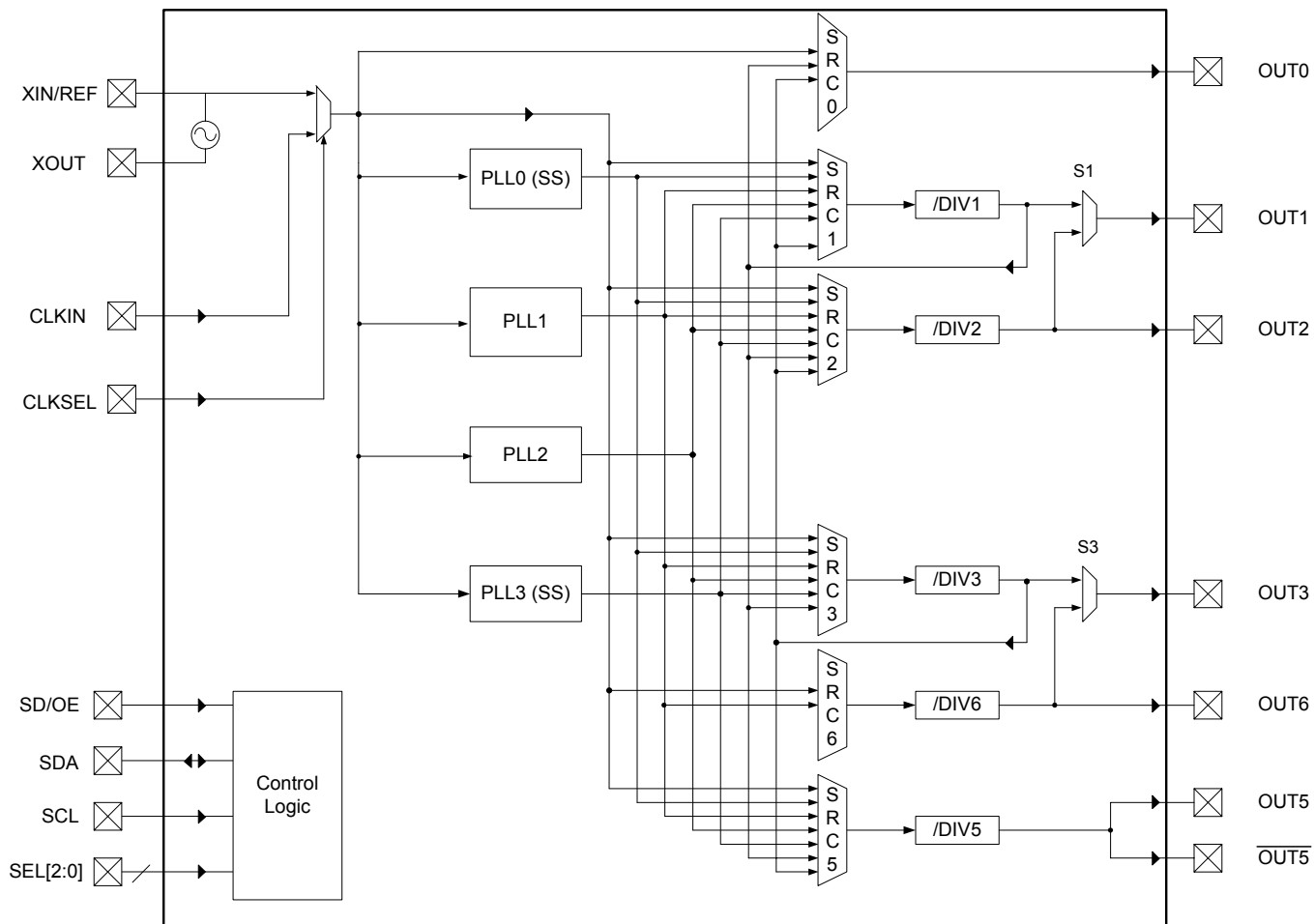
Each of the four PLLs has an 7-bit reference divider and a 12-bit feedback divider. This allows the user to generate four unique non-integer-related frequencies. The PLL loop bandwidth is programmable to allow the user to tailor the PLL response to the application. For instance, the user can tune the PLL parameters to minimize jitter generation or to maximize jitter attenuation. Spread spectrum generation and/or fractional divides are allowed on two of the PLLs.

There are a total of five 8-bit output dividers. Each output bank can be configured to support LVTTTL, LVPECL, LVDS or HCSL logic levels. Out0 (Output 0) supports LVTTTL standard only. The outputs are connected to the PLLs via a switch matrix. The switch matrix allows the user to route the PLL outputs to any output bank. This feature can be used to simplify and optimize the board layout. In addition, each output's slew rate and enable/disable function is programmable.

## Features:

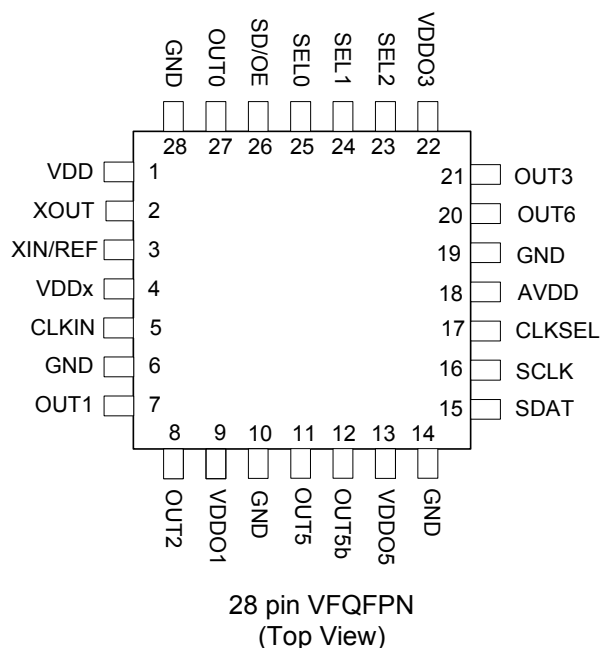
- Four internal PLLs
- Internal non-volatile EEPROM
- Fast (400kHz) mode I<sup>2</sup>C serial interface
- Input frequency range: 1 MHz to 200 MHz
- Output frequency range: 4.9 kHz to 500 MHz
- Reference crystal input with programmable linear load capacitance
  - Crystal frequency range: 8 MHz to 50 MHz
- Three independently controlled VDDO (1.8V - 3.3V)
- Each PLL has a 7-bit reference divider and a 12-bit feedback-divider
- 8-bit output-divider blocks
- Fractional division capability on one PLL
- Two of the PLLs support spread spectrum generation capability
- I/O Standards:
  - Outputs - 1.8 - 3.3 V LVTTTL/ LVCMOS
  - Outputs - LVPECL, LVDS and HCSL
  - Inputs - 3.3 V LVTTTL/ LVCMOS
- Programmable slew rate control
- Programmable loop bandwidth
- Programmable output inversion to reduce bimodal jitter
- Redundant clock inputs with glitchless auto and manual switchover options
- Individual output enable/disable
- Power-down mode
- 3.3V core V<sub>DD</sub>
- Available in VFQFPN package
- -40 to +85 C Industrial Temp operation

## Functional Block Diagram



1. OUT1 & OUT2, OUT3 & OUT6, and OUT5 &  $\overline{\text{OUT5}}$  pairs can be configured to be LVDS, LVPECL or HCSL, or two single-ended LVTTTL outputs.
2. CLKIN, CLKSEL, SD/OE and SEL[2:0] have pull down resistors.

## Pin Configuration



## Pin Descriptions

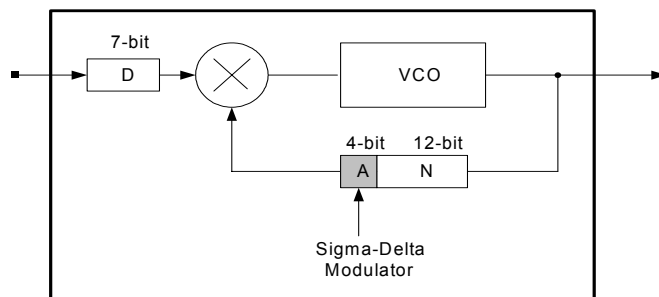
Pin#	Pin Name	I/O	Pin Type	Pin Description
1	VDD		Power	Device power supply. Connect to 3.3V.
2	XOUT	O	LVTTTL	CRYSTAL_OUT -- Reference crystal feedback.
3	XIN / REF	I	LVTTTL	CRYSTAL_IN -- Reference crystal input or external reference clock input.
4	VDDx		Power	Crystal oscillator power supply. Connect to 3.3V. Use filtered analog power supply if available.
5	CLKIN	I	LVTTTL	Input clock. Weak internal pull down resistor.
6	GND		Power	Connect to Ground.
7	OUT1	O	Adjustable <sup>1</sup>	Configurable clock output 1. Single-ended or differential when combined with OUT2.
8	OUT2	O	Adjustable <sup>1</sup>	Configurable clock output 2. Single-ended or differential when combined with OUT1.
9	VDDO1		Power	Device power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT1 and OUT2.
10	GND		Power	Connect to Ground.
11	OUT5	O	Adjustable <sup>1,2</sup>	Configurable clock output 5. Single-ended or differential when combined with OUT5b.
12	OUT5b	O	Adjustable <sup>1,2</sup>	Configurable clock output 5b. Single-ended or differential when combined with OUT5.

Pin#	Pin Name	I/O	Pin Type	Pin Description
13	VDDO5		Power	Device power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT5 and OUT5b.
14	GND		Power	Connect to Ground.
15	SDAT	I/O	LVTTTL	Bidirectional I <sup>2</sup> C data.
16	SCLK	I	LVTTTL	I <sup>2</sup> C clock.
17	CLKSEL	I	LVTTTL	Input clock selector. Weak internal pull down resistor.
18	AVDD		Power	Device analog power supply. Connect to 3.3V. Use filtered analog power supply if available.
19	GND		Power	Connect to Ground.
20	OUT6	O	Adjustable <sup>1</sup>	Configurable clock output 6. Single-ended or differential when combined with OUT3.
21	OUT3	O	Adjustable <sup>1</sup>	Configurable clock output 3. Single-ended or differential when combined with OUT6.
22	VDDO3		Power	Device power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT3 and OUT6.
23	SEL2	I	LVTTTL	Configuration select pin. Weak internal pull down resistor.
24	SEL1	I	LVTTTL	Configuration select pin. Weak internal pull down resistor.
25	SEL0	I	LVTTTL	Configuration select pin. Weak internal pull down resistor.
26	SD/OE	I	LVTTTL	Enables/disables the outputs or powers down the chip. The SP bit (0x02) controls the polarity of the signal to be either active HIGH or LOW. (Default is active HIGH.)
27	OUT0	O	LVTTTL	Configurable clock output 0.
28	GND		Power	Connect to Ground.

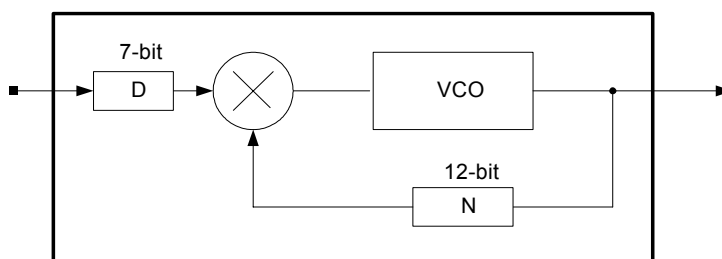
1. Outputs are user programmable to drive single-ended 3.3-V LVTTTL, or differential LVDS, LVPECL or HCSL interface levels

2. When only an individual single-ended clock output is required, tie OUT# and OUT#b together.

## PLL Features and Descriptions



**PLL0 Block Diagram**



**PLL1, PLL2 and PLL3 Block Diagram**

	Pre-Divider (D) <sup>1</sup> Values	Multiplier (M) <sup>2</sup> Values	Programmable Loop Bandwidth	Spread Spectrum Generation Capability
PLL0	1 - 127	10 - 8206	Yes	Yes
PLL1	1 - 127	1 - 4095	Yes	No
PLL2	1 - 127	1 - 4095	Yes	No
PLL3	3 - 127	12 - 4095	Yes	Yes

1. For PLL0, PLL1 and PLL2, D=0 means PLL power down. For PLL3, 0, 1, and 2 are DNU (do not use)

2. For PLL0,  $M = 2 \cdot N + A + 1$  (for  $A > 0$ );  $M = 2 \cdot N$  (for  $A = 0$ );  $A \leq N-1$ . For PLL1, PLL2 and PLL3,  $M=N$ .

## Reference Clock Input Pins and Selection

The IDT5V49EE702 supports up to two clock inputs. One of the clock inputs (XIN/ REF) can be driven by either an external crystal or a reference clock. The second clock input (CLKIN) can only be driven from an external reference clock. The CLKSEL pin selects the input clock from either XTAL/REF or CLKIN.

Either clock input can be set as the primary clock. The primary clock designation is to establish which is the main reference clock to the PLLs. The non-primary clock is designated as the secondary clock in case the primary clock goes absent and a backup is needed. The PRIMSRC bit (0xBE through 0xC3) determines which clock input will be selected as primary clock. When PRIMSRC bit is "0", XIN/REF is selected as the primary clock, and when "1", CLKIN as the primary clock.

The two external reference clocks can be manually selected using the CLKSEL pin. The SM bits (0xBE through 0xC3) must be set to "0x" for manual switchover which is detailed in SWITCHOVER MODES section.

### Crystal Input (XIN/REF)

The crystal used should be a fundamental mode quartz crystal; overtone crystals should not be used.

When the XIN/REF pin is driven by a crystal, it is important to set the internal inverter oscillator drive strength and tuning/load capacitor values correctly to achieve the best clock performance. These values are programmable through I<sup>2</sup>C interface to allow for maximum compatibility with crystals from various manufacturers, processes, performances, and qualities. The internal load capacitors are true parallel-plate capacitors for ultra-linear performance. Parallel-plate capacitors were chosen to reduce the frequency shift that occurs when non-linear load capacitance interacts with load, bias, supply, and temperature changes. External non-linear crystal load capacitors should not be used for applications that are sensitive to absolute frequency requirements. The value of the internal load capacitors are determined by XTAL[4:0] bits. The load capacitance can be set with a resolution of 0.125 pF for a total crystal load ranging from 3.5 pF to 7.5 pF. Check with the crystal vendor's load capacitance specification for the exact setting to tune the internal load capacitor. The following equation governs how the total

internal load capacitance is set.

$$\text{XTAL load cap} = 3.5 \text{ pF} + \text{XTAL}[4:0] * 0.125 \text{ pF (Eq. 1)}$$

Parameter	Bits	Step (pF)	Min (pF)	Max (pF)
XTAL	8	0.125	0	4

When using an external reference clock instead of a crystal on the XTAL/REF pin, the input load capacitors may be completely bypassed. This allows for the input frequency to be up to 200 MHz. When using an external reference clock, the XOUT pin must be left floating, XTAL must be programmed to the default value of "00h", and the crystal drive strength bit, XDRV (0x06), must be set to the default value of "11h".

## Switchover Modes

The IDT5V49EE702 features redundant clock inputs which supports both Automatic and Manual switchover mode. These two modes are determined by the configuration bits, SM (0xBE through 0xC3). The primary clock source can be programmed, via the PRIMSRC bit, to be either XIN/REF or CLKIN. The other clock input will be considered as the secondary source. Note that the switchover modes are asynchronous. If the reference clocks are directly routed to OUTx with no phase relationship, short pulses can be generated during switchover. The automatic switchover mode will work only when the primary clock source is XIN/REF. Switchover modes are not supported for crystal input configurations.

### Manual Switchover Mode

When SM[1:0] is "0x", the redundant inputs are in manual switchover mode. In this mode, CLKSEL pin is used to switch between the primary and secondary clock sources. As previously mentioned, the primary and secondary clock source setting is determined by the PRIMSRC bit. During the switchover, no glitches will occur at the output of the device, although there may be frequency and phase drift, depending on the exact phase and frequency relationship between the primary and secondary clocks.

### Automatic Switchover Mode

The redundant inputs are in automatic switchover mode. Automatic switchover mode has revertive functionality. The input clock selection will switch to the secondary clock source when there are no transitions on the primary clock source for two secondary clock cycles. If both reference

clocks are at different frequencies, the device will always remain on the primary clock unless it is absent for two secondary clock cycles. The secondary clock must always run at a frequency less than or equal to the primary clock frequency.

### Reference Divider, Feedback Divider, and Output Divider

Each PLL incorporates a 7-bit reference divider (D[6:0]) and a 12-bit feedback divider (N[11:0]) that allows the user to generate four unique non-integer-related frequencies. Each output divide supports 8-bit output-divider (PM and Q[7:0]). The following equation governs how the output frequency is calculated.

$$F_{OUT} = \frac{F_{IN} * \left(\frac{M}{D}\right)}{ODIV} \quad (\text{Eq. 1})$$

Where FIN is the reference frequency, M is the total feedback-divider value, D is the reference divider value, ODIV is the total output-divider value, and FOUT is the resulting output frequency.

For PLL0,

$$M = 2 * N + A + 1 \quad (\text{for } A > 0)$$

$$M = 2 * N \quad (\text{for } A = 0)$$

For PLL1, PLL2 and PLL3,

$$M = N$$

PM and Q[6:0] are the bits used to program the 8-bit output-dividers for outputs OUT1-6. OUT0 does not have any output divide along its path. The 8-bit output-dividers will bypass or divide down the output banks' frequency with even integer values ranging from 2 to 256.

There is the option to choose between disabling the output-divider, utilizing a div/1, a div/2, or the 7-bit Q-divider by using the PM bit. If the output is disabled, it will be driven High, Low or High Impedance, depending on OEM[1:0]. Each bank, except for OUT0, has a PM bit. When disabled, no clocks will appear at the output of the divider, but will remain powered on. The output divides selection table is shown below.

Q[6:0]	PM	Output Divider
111 1111	0	Disabled
	1	/1
<111 1111	0	/2
	1	/((Q[6:0] + 2) * 2)

Note that the actual 7-bit Q-divider value has a 2 added to the integer value Q and the outputs are routed through another div/2 block. The output divider should never be disabled unless the output bank will never be used during normal operation. The output frequency range for LVTTTL outputs are from 4.9KHz to 200MHz. The output frequency for LVPECL/LVDS/HCSL outputs range from 4.9KHz to 500MHz.

### Spread Spectrum Generation (PLL0)

PLL0 supports spread spectrum generation capability, which users have the option of turning on or off. Spread spectrum profile, frequency, and spread amplitude are fully programmable. The programmable spread spectrum generation parameters are TSSC[3:0], NSSC[2:0], SS\_OFFSET[5:0], SD[3:0], DITH, and X2 bits. These bits are in the memory address from 0xAC to 0xBD for PLL0. The spread spectrum generation on PLL0 can be enabled/disabled using the TSSC[3:0] bits. To enable spread spectrum, set TSSC > '0' and set NSSC[2:0], SS\_OFFSET[5:0], SD[3:0], and the A[3:0] (in the total M value) accordingly. To disable spread spectrum generation, set TSSC = '0'.

#### TSSC[3:0]

These bits are used to determine the number of phase/frequency detector cycles per spread spectrum cycle (ssc) steps. The modulation frequency can be calculated with the TSSC bits in conjunction with the NSSC bits. Valid TSSC integer values for the modulation frequency range from 5 to 14. Values of 0 - 4 and 15 should not be used.

#### NSSC[2:0]

These bits are used to determine the number of delta-encoded samples used for a single quadrant of the spread spectrum waveform. All four quadrants of the spread spectrum waveform are mirror images of each other. The modulation frequency is also calculated based on the NSSC bits in conjunction with the TSSC bits. Valid NSSC integer

values range from 1 to 6. Values of 0 and 7 should not be used.

### SS\_OFFSET[5:0]

These bits are used to program the fractional offset with respect to the nominal M integer value. For center spread, the SS\_OFFSET is set to '0' so that the spread spectrum waveform is centered about the nominal M (Mnom) value. For down spread, the SS\_OFFSET > '0' such the spread spectrum waveform is centered about the (Mideal -1 +SS\_Offset) value. The downspread percentage can be thought of in terms of center spread. For example, a downspread of -1% can also be considered as a center spread of ±0.5% but with Mnom shifted down by one and offset. The SS\_OFFSET has integer values ranging from 0 to 63.

### SD[3:0]

These bits are used to shape the profile of the spread spectrum waveform. These are delta-encoded samples of the waveform. There are twelve sets of SD samples. The NSSC bits determine how many of these samples are used for the waveform. The sum of these delta-encoded samples (sigma delta- encoded samples) determine the amount of spread and should not exceed (63 - SS\_OFFSET). The maximum spread is inversely proportional to the nominal M integer value.

### DITH

This bit is used for dithering the sigma-delta-encoded samples. This will randomize the least-significant bit of the input to the spread spectrum modulator. Set the bit to '1' to enable dithering.

### X2

This bit will double the total value of the sigma-delta-encoded-samples which will increase the amplitude of the spread spectrum waveform by a factor of two. When X2 is '0', the amplitude remains nominal but if set to '1', the amplitude is increased by x2. The following equations govern how the spread spectrum is set:

$$T_{SSC} = TSSC[3:0] + 2 \text{ (Eq. 2)}$$

$$N_{SSC} = NSSC[2:0] * 2 \text{ (Eq. 3)}$$

$$SD[3:0]_K = S_{J+1}(\text{unencoded}) - S_J(\text{unencoded}) \text{ (Eq. 4)}$$

where  $S_J$  is the unencoded sample out of a possible 12 and

$SD_K$  is the delta-encoded sample out of a possible 12.

$$\text{Amplitude} = ((2 * N[11:0] + A[3:0] + 1) * \text{Spread\%} / 100) / 2 \text{ (Eq. 5)}$$

if  $1 < \text{Amplitude} < 2$ , then set X2 bit to '1'.

### Modulation frequency:

$$F_{PPD} = F_{IN} / D \text{ (Eq. 6)}$$

$$F_{VCO} = F_{PPD} * M_{NOM} \text{ (Eq. 7)}$$

$$F_{SSC} = F_{PPD} / (4 * N_{SSC} * T_{SSC}) \text{ (Eq. 8)}$$

### Spread:

$$\Sigma \Delta = SD_0 + SD_1 + SD_2 + \dots + SD_{11}$$

the number of samples used depends on the Nssc value

$$\Sigma \Delta \leq 63 - SS\_OFFSET$$

$$\pm \text{Spread\%} = (\Sigma \Delta * 100) / (64 * (2 * N[11:0] + A[3:0] + 1)) \text{ (Eq. 9)}$$

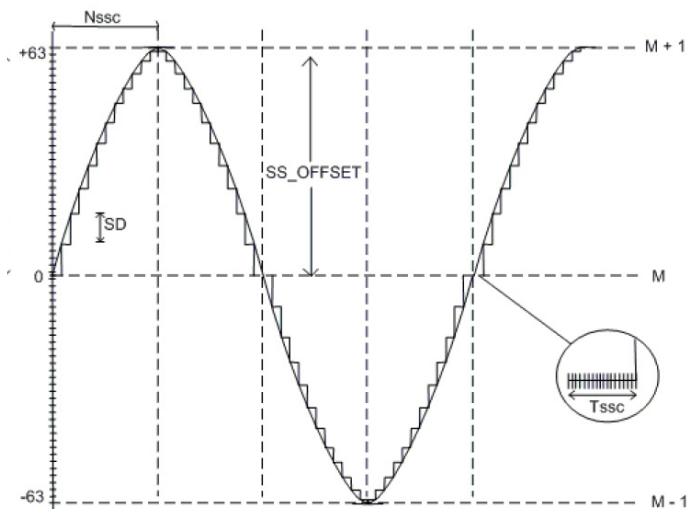
$$\pm \text{Max Spread\%} / 100 = 1 / M_{NOM} \text{ or } 2 / M_{NOM} (X2=1)$$



## Profile:

Waveform starts with SS\_OFFSET, SS\_OFFSET + SD<sub>J</sub>, SS\_OFFSET + SD<sub>J+1</sub>, etc.

### Spread Spectrum Using Sinusoidal Profile



## Example

$F_{IN} = 25\text{MHz}$ ,  $F_{OUT} = 100\text{MHz}$ ,  $F_{SSC} = 33\text{KHz}$  with center spread of  $\pm 2\%$ . Find the necessary spread spectrum register settings.

Since the spread is center, the SS\_OFFSET can be set to '0'. Solve for the nominal M value; keep in mind that the nominal M should be chosen to maximize

the VCO. Start with  $D = 1$ , using Eq.6 and Eq.7.

$$M_{NOM} = 1200\text{MHz} / 25\text{MHz} = 48$$

Using Eq.4, we arbitrarily choose  $N = 22$ ,  $A = 3$ . Now that we have the nominal M value, we can determine TSSC and NSSC by using Eq.8.

$$N_{SSC} * T_{SSC} = 25\text{MHz} / (33\text{KHz} * 4) = 190$$

However, using Eq. 2 and Eq.3, we find that the closest value is when  $T_{SSC} = 14$  and  $N_{SSC} = 6$ . Keep in mind to maximize the number of samples used

to enhance the profile of the spread spectrum waveform.

$$T_{SSC} = 14 + 2 = 16$$

$$N_{SSC} = 6 * 2 = 12$$

$$N_{SSC} * T_{SSC} = 192$$

Use Eq.10 to determine the value of the sigma-delta-encoded samples.

$$\pm 2\% = (\Sigma\Delta * 100) / (64 * 48)$$

$$\Sigma\Delta = 61.4$$

Either round up or down to the nearest integer value. Therefore, we end up with 61 or 62 for sigma-delta-encoded samples. Since the sigma-delta-encoded samples must not exceed 63 with SS\_OFFSET set to '0', 61 or 62 is well within the limits. It is the discretion of the user to define the shape of the profile that is better suited for the intended application.

Using Eq. 9 again, the actual spread for the sigma-delta-encoded samples of 56 and 57 are  $\pm 1.99\%$  and  $\pm 2.02\%$ , respectively.

Use Eq.10 to determine if the X2 bit needs to be set;

$$\text{Amplitude} = 48 * (1.99 \text{ or } 2.02) / 100/2 = 0.48 < 1$$

Therefore, the X2 = '0'. The dither bit is left to the discretion of the user.

The example above was of a center spread using spread spectrum. For down spread, the nominal M value can be set one integer value lower to 47.

Note that the IDT5V49EE702 should not be programmed with  $T_{SSC} > '0'$ ,  $SS\_OFFSET = '0'$ , and  $SD = '0'$  in order to prevent an unstable state in the modulator.

The PLL loop bandwidth must be at least 10x the modulation frequency along with higher damping (larger  $\omega_z$ ) to prevent the spread spectrum from being filtered and reduce extraneous noise. Refer to the LOOP FILTER section for more detail on  $\omega_z$ . The A[3:0] must be used for spread spectrum, even if the total multiplier value is an even integer.

## Spread Spectrum Generation (PLL3)

PLL3 support spread spectrum generation capability, which users have the option of turning on and off. Spread spectrum profile, frequency, and spread are fully programmable (within limits). The technique is different from that used in PLL0. The programmable spread spectrum generation parameters are SS\_D3[7:0], SSVCO[15:0], SSENb, IP3[4:0] and RZ3[3:0] bits. These bits are in the memory address range of 0x4C to 0x85 for PLL3. The spread spectrum generation on PLL3 can be enabled/disabled using the SSENb bit. To enable spread spectrum, set SSENb = '1'.

### For Spread Enabled:

Spread spectrum is configured using SS\_D3(spread spectrum reference divide)

$$SS\_D3 = \frac{F_{IN}}{4 * F_{MOD}} \quad (\text{Eq. 10})$$

and SSVCO (spread spectrum loop feedback counter).

$$SSVCO = [0.5 * \frac{F_{VCO}}{F_{MOD}} * (1 + SS/400) + 5] \quad (\text{Eq. 11})$$

SS is the total Spread Spectrum amount (I.e. center spread  $\pm 0.5\%$  has a total spread of 1.0% and down spread -0.5% has a total spread of 0.5%.)

### Loop Filter

The loop filter for each PLL can be programmed to optimize the jitter performance. The low-pass frequency response of the PLL is the mechanism that dictates the jitter transfer characteristics. The loop bandwidth can be extracted from the jitter transfer. A narrow loop bandwidth is good for jitter attenuation while a wide loop bandwidth is best for low-jitter frequency generation. The specific loop filter components that can be programmed are the resistor via the RZ[3:0] bits, zero capacitor via the CZ bit (for PLL0, PLL1 and PLL2), and the charge pump current via the IP[2:0] bits (for PLL0, PLL1 and PLL2) or IP[3:0] (for PLL3).

The following equations govern how the loop filter is set for PLL0 - PLL2:

$$\text{Resistor (Rz)} = (RZ[0] + 2 * RZ[1] + 4 * RZ[2] + 8 * RZ[3]) * 4.0 \text{ kOhm}$$

$$\text{Zero capacitor (Cz)} = 196 \text{ pF} + CZ * 217 \text{ pF}$$

$$\text{Pole capacitor (Cp)} = 15 \text{ pF}$$

$$\text{Charge pump (Ip)} = 6 * (IP[0] + 2 * IP[1] + 4 * IP[2]) \text{ uA}$$

$$\text{VCO gain (Kvco)} = 900 \text{ MHz/V} * 2\pi$$

The following equations govern how the loop filter is set for PLL3:

For Non-Spread Spectrum Operation:

$$\text{Resistor(Rz)} = \frac{(12.5 + 12.5 * (RZ[1] + 2 * RZ[2] + 4 * RZ[3]))}{* RZ[0] + 6 * (1 - RZ[0])} \text{ kOhms (Eq. 12)}$$

For Spread Spectrum Operation:

$$\text{Resistor(Rz)} = \frac{(62.5 + 12.5 * (RZ[1] + 2 * RZ[2] + 4 * RZ[3]))}{* RZ[0] + 6 * (1 - RZ[0])} \text{ kOhms (Eq. 13)}$$

$$\text{Zero capacitor (Cz)} = 250 \text{ pF}$$

$$\text{Pole capacitor (Cp)} = 15 \text{ pF}$$

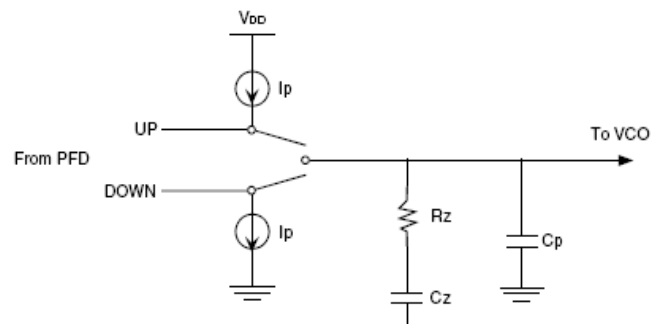
For Non-Spread Spectrum Operation:

$$\text{Charge pump (Ip)} = \frac{24 * (1 + (2 * IP[0]) + (4 * IP[1]) + (8 * IP[2]))}{3 + (5 * IP[3]) + (11 * IP[4])} \text{ A (Eq. 14)}$$

For Spread Spectrum Operation:

$$\text{Charge pump (Ip)} = \frac{12 * (1 + (2 * IP[0]) + (4 * IP[1]) + (8 * IP[2]))}{27 + (5 * IP[3]) + (11 * IP[4])} \text{ A (Eq. 14)}$$

$$\text{VCO gain (Kvco)} = 900 \text{ MHz/V} * 2\pi$$



**PLL Loop Bandwidth:**

Charge pump gain ( $K\phi$ ) =  $I_p / 2\pi$

VCO gain ( $K_{VCO}$ ) = 900 MHz/V \*  $2\pi$

M = Total multiplier value (See the Reference Divider, Feedback Divider and Output Divider section for more detail)

$$\omega_c = (R_z * K\phi * K_{VCO} * C_z) / (M * (C_z + C_p))$$

$$F_c = \omega_c / 2\pi$$

Note, the phase/frequency detector frequency ( $F_{PFD}$ ) is typically seven times the PLL closed-loop bandwidth ( $F_c$ ) but too high of a ratio will reduce the phase margin thus compromising loop stability.

To determine if the loop is stable, the phase margin ( $\phi_m$ ) needs to be calculated as follows.

**Phase Margin:**

$$\omega_z = 1 / (R_z * C_z)$$

$$\omega_p = (C_z + C_p) / (R_z * C_z * C_p)$$

$$\phi_m = (360 / 2\pi) * [\tan^{-1}(\omega_c / \omega_z) - \tan^{-1}(\omega_c / \omega_p)]$$

To ensure stability in the loop, the phase margin is recommended to be  $> 60^\circ$  but too high will result in the lock time being excessively long. Certain loop filter parameters would need to be compromised to not only meet a required loop bandwidth but to also maintain loop stability.

## SEL[2:0] Function

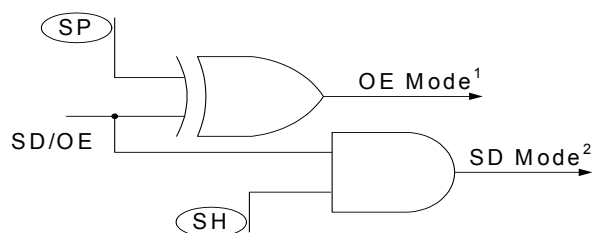
The IDT5V49EE702 can support up to six unique configurations. Users may pre-programmed all these configurations, and select the configurations using SEL[2:0]

pins. Alternatively, users may use I<sup>2</sup>C interface to configure these registers on-the-fly.

SEL2	SEL1	SEL0	Configuration Selections
0	0	0	Select CONFIG0
0	0	1	Select CONFIG1
0	1	0	Select CONFIG2
0	1	1	Select CONFIG3
1	0	0	Select CONFIG4
1	0	1	Select CONFIG5
1	1	0	Reserved (Do not use)
1	1	1	Reserved (Do not use)

## SD/OE Pin Function

The polarity of the SD/OE signal pin can be programmed to be either active HIGH or LOW with the SP bit (0x02). When SP is "0" (default), the pin becomes active HIGH and when SP is "1", the pin becomes active LOW. The SD/OE pin can be configured as either to shutdown the PLLs or to enable/disable the outputs.



- 1 Assert to disable the outputs whose OE bits are set  
2 Assert to shut down power, on the outputs and 3-level pins

## Configuration OUTx IO Standard

Users can configure the individual output IO standard from a specified 1.8V to 3.3V power supplies. Each output can support 1.8V to 3.3V LVTTTL. Each output pair can support LVDS, LVPECL or HCSL from the specified 3.3V power supply. OUT0 can only be 3.3V single-ended output.

## Programming the Device

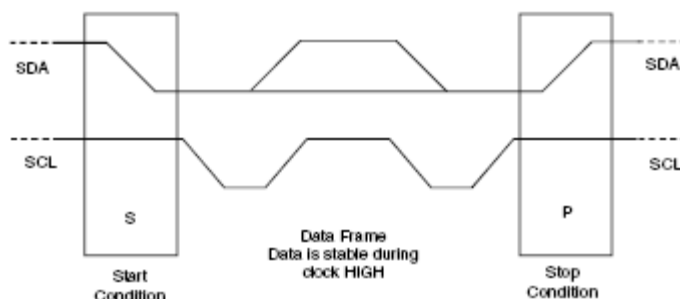
I<sup>2</sup>C may be used to program the IDT5V49EE702.

– Device (slave) address = 7'b1101010

## I<sup>2</sup>C Programming

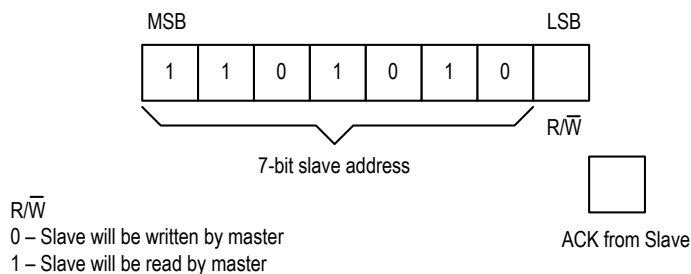
The IDT5V49EE702 is programmed through an I<sup>2</sup>C-Bus serial interface, and is an I<sup>2</sup>C slave device. The read and write transfer formats are supported. The first byte of data after a write frame to the correct slave address is interpreted as the register address; this address auto-increments after each byte written or read.

The frame formats are shown in the following illustration.



Framing

Each frame starts with a “Start Condition” and ends with an “End Condition”. These are both generated by the Master device.



The first byte transmitted by the Master is the Slave Address followed by the R/W bit. The Slave acknowledges by sending a “1” bit.

### First Byte Transmitted on I<sup>2</sup>C Bus

### External I<sup>2</sup>C Interface Condition

#### KEY:

- ☐ From Master to Slave
- ☐ From Master to Slave, but can be omitted if followed by the correct sequence  
Normally, data transfer is terminated by a STOP condition generated by the Master. However, if the Master still wishes to communicate on the bus, it can generate a separate START condition, and address another Slave address without first generating a STOP condition.
- ☐ From Slave to Master

#### SYMBOLS:

ACK - Acknowledge (SDAT LOW)  
NACK – Not Acknowledge (SDAT HIGH)  
SR – Repeated Start Condition  
S – START Condition  
P – STOP Condition

### Progrwrite

S	Address	R/W	ACK	Command Code	ACK	Register	ACK	Data	ACK	P
	7-bits	0	1-bit	8-bits: xxxx xx00	1-bit	8-bits	1-bit	8-bits	1-bit	

### Progrwrite Command Frame

Writes can continue as long as a Stop condition is not sent and each byte will increment the register address.

## Proread

Note: If the expected read command is not from the next higher register to the previous read or write command, then set a known “read” register address prior to a read operation by issuing the following command:

S	Address	R/ $\overline{W}$	ACK	Command Code	ACK	Register	ACK	P
	7-bits	0	1-bit	8-bits: xxxx xx00	1-bit	8-bits	1-bit	

Prior to Proread Command Set Register Address

The user can ignore the STOP condition above and use a repeated START condition instead, straight after the slave acknowledgement bit (i.e., followed by the Proread command):

S	Address	R/ $\overline{W}$	ACK	ID Byte	ACK	Data_1	ACK	Data_2	ACK	Data_last	NACK	P
	7-bits	1	1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit	

### Proread Command Frame

## Progsave

S	Address	R/ $\overline{W}$	ACK	Command Code	ACK	P
	7-bits	0	1-bit	8-bits: xxxx xx01	1-bit	

Note:

PROGWRITE is for writing to the IDT5V49EE702 registers.

PROGREAD is for reading the IDT5V49EE702 registers.

PROGSAVE is for saving all the contents of the IDT5V49EE702 registers to the EEPROM.

PROGRESTORE is for loading the entire EEPROM contents to the IDT5V49EE702 registers.

## Progestore

S	Address	R/ $\overline{W}$	ACK	Command Code	ACK	P
	7-bits	0	1-bit	8-bits: xxxx xx10	1-bit	

## EEPROM Interface

The IDT5V49EE702 can also store its configuration in an internal EEPROM. The contents of the device's internal programming registers can be saved to the EEPROM by issuing a save instruction (ProgSave) and can be loaded back to the internal programming registers by issuing a restore instruction (ProgRestore).

To initiate a save or restore using I<sup>2</sup>C, only two bytes are transferred. The Device Address is issued with the read/write bit set to “0”, followed by the appropriate command code. The save or restore instruction executes after the STOP condition is issued by the Master, during which time the IDT5V49EE702 will not generate Acknowledge bits. The IDT5V49EE702 will acknowledge the instructions after it has completed execution of them. During that time, the I<sup>2</sup>C bus should be interpreted as busy by all other users of the bus.

On power-up of the IDT5V49EE702, an automatic restore is performed to load the EEPROM contents into the internal programming registers. The IDT5V49EE702 will be ready to accept a programming instruction once it acknowledges its 7-bit I<sup>2</sup>C address.

## I<sup>2</sup>C Bus DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	Input HIGH Level		0.7xV <sub>DD</sub>			V
V <sub>IL</sub>	Input LOW Level				0.3xV <sub>DD</sub>	V
V <sub>HYS</sub>	Hysteresis of Inputs		0.05xV <sub>DD</sub>			V
I <sub>IN</sub>	Input Leakage Current				±1.0	μA
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 3 mA			0.4	V

## I<sup>2</sup>C Bus AC Characteristics for Standard Mode

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>SCLK</sub>	Serial Clock Frequency (SCL)	0		100	kHz
t <sub>BUF</sub>	Bus free time between STOP and START	4.7			μs
t <sub>SU:START</sub>	Setup Time, START	4.7			μs
t <sub>HD:START</sub>	Hold Time, START	4			μs
t <sub>SU:DATA</sub>	Setup Time, data input (SDA)	250			ns
t <sub>HD:DATA</sub>	Hold Time, data input (SDA) <sup>1</sup>	0			μs
t <sub>OVD</sub>	Output data valid from clock			3.45	μs
C <sub>B</sub>	Capacitive Load for Each Bus Line			400	pF
t <sub>R</sub>	Rise Time, data and clock (SDAT, SCLK)			1000	ns
t <sub>F</sub>	Fall Time, data and clock (SDAT, SCLK)			300	ns
t <sub>HIGH</sub>	HIGH Time, clock (SCLK)	4			μs
t <sub>LOW</sub>	LOW Time, clock (SCLK)	4.7			μs
t <sub>SU:STOP</sub>	Setup Time, STOP	4			μs

Note 1: A device must internally provide a hold time of at least 300 ns for the SDAT signal (referred to the V<sub>IH</sub>(MIN) of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.

## I<sup>2</sup>C Bus AC Characteristics for Fast Mode

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>SCLK</sub>	Serial Clock Frequency (SCL)	0		400	kHz
t <sub>BUF</sub>	Bus free time between STOP and START	1.3			μs
t <sub>SU:START</sub>	Setup Time, START	0.6			μs
t <sub>HD:START</sub>	Hold Time, START	0.6			μs
t <sub>SU:DATA</sub>	Setup Time, data input (SDA)	100			ns
t <sub>HD:DATA</sub>	Hold Time, data input (SDA) <sup>1</sup>	0			μs
t <sub>OVD</sub>	Output data valid from clock			0.9	μs
C <sub>B</sub>	Capacitive Load for Each Bus Line			400	pF
t <sub>R</sub>	Rise Time, data and clock (SDA, SCL)	20 + 0.1xC <sub>B</sub>		300	ns
t <sub>F</sub>	Fall Time, data and clock (SDA, SCL)	20 + 0.1xC <sub>B</sub>		300	ns
t <sub>HIGH</sub>	HIGH Time, clock (SCL)	0.6			μs
t <sub>LOW</sub>	LOW Time, clock (SCL)	1.3			μs
t <sub>SU:STOP</sub>	Setup Time, STOP	0.6			μs

Note 1: A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IH</sub>(MIN) of the SCL signal) to bridge the undefined region of the falling edge of SCL.



## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V49EE702. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Symbol	Description	Min	Max	Unit
$V_{DD}$	Internal Power Supply Voltage	-0.5	+4.6	V
$V_I$	Input Voltage <sup>1</sup>	-0.5	+4.6	V
$V_O$	Output Voltage (not to exceed 4.6 V) <sup>1</sup>	-0.5	$V_{DD}+0.5$	V
$T_J$	Junction Temperature		150	°C
$T_{STG}$	Storage Temperature	-65	150	°C

1. Input negative and output voltage ratings may be exceeded if the input and output current ratings are observed.

## Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
$V_{DD}$	Power supply voltage for $V_{DD}$ pins supporting core and outputs	3.135	3.3	3.465	V
$V_{DDX}$	Power supply voltage for crystal oscillator. Use filtered analog power supply if available.	3.135	3.3	3.465	V
$AV_{DD}$	Analog power supply voltage. Use filtered analog power supply if available.	3.135	3.3	3.465	V
$V_{DDOX}$	3.3V VDDO Range	3.0	3.3	3.6	V
	2.5V VDDO Range for 2.5V LVTTTL	2.25	2.5	2.75	V
	1.8V VDDO Range for 1.8V LVTTTL	1.7	1.8	1.9	V
	Power supply voltage for $V_{DD}$ pins supporting LVDS/LVPECL/HCSL outputs	3.135	3.3	3.465	V
$T_A$	Operating temperature, ambient	-40		+85	°C
$C_{LOAD\_OUT}$	Maximum load capacitance (3.3V LVTTTL only)			15	pF
	Maximum load capacitance (1.8V/2.5V LVTTTL only)			8	pF
$F_{IN}$	External reference crystal	8		50	MHz
	External reference clock CLKIN	1		200	
$t_{PU}$	Power up time for all $V_{DD}$ s to reach minimum specified voltage (power ramps must be monotonic)	0.05		5	ms

## Capacitance ( $T_A = +25\text{ }^{\circ}\text{C}$ )

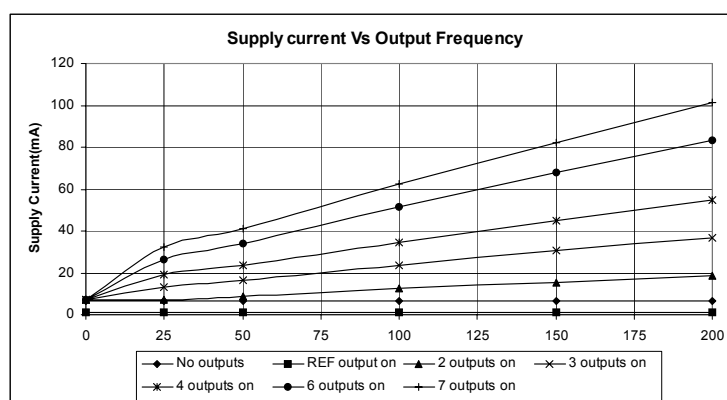
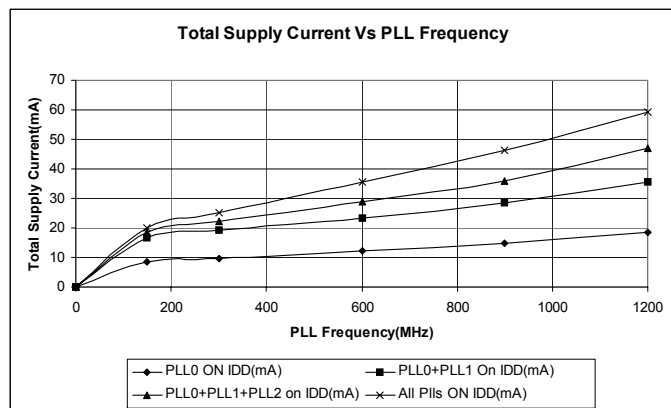
Symbol	Parameter	Min	Typ	Max	Unit
$C_{IN}$	Input Capacitance (CLKIN, CLKSEL, SD/OE, SDA, SCL, SEL[2:0])		3	7	pF
Pull-down Resistor	CLKIN, CLKSEL, SD/OE, SEL[2:0]		180		k $\Omega$
<b>Crystal Specifications</b>					
XTAL_FREQ	Crystal frequency	8		50	MHz
XTAL_MIN	Minimum crystal load capacitance	3.5			pF
XTAL_MAX	Maximum crystal load capacitance			35.5	pF
XTAL_V <sub>PP</sub>	Voltage swing (peak-to-peak, nominal)	1.5	2.3	3.2	V

## DC Electrical Characteristics for 3.3-V LVTTTL<sup>1</sup>

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage		2.4		$V_{DD}$	V
$V_{OL}$	Output LOW Voltage				0.4	V
$V_{IH}$	Input HIGH Voltage		2			V
$V_{IL}$	Input LOW Voltage				0.8	V
$I_{OZDD}$	Output Leakage Current	3-state outputs. $V_O = V_{DD}$ or GND, $V_{DD} = 3.6\text{V}$			10	$\mu\text{A}$

Note 1: See "Recommended Operating Conditions" table.

## Power Supply Characteristics for PLLs and LVTTTL Outputs



## DC Electrical Characteristics for LVDS

Symbol	Parameter	Min	Typ	Max	Unit
$V_{OT}(+)$	Differential Output Voltage for the TRUE binary state	247		454	mV
$V_{OT}(-)$	Differential Output Voltage for the FALSE binary state	-247		-454	mV
$\Delta V_{OT}$	Change in $V_{OT}$ between Complimentary Output States			50	mV
$V_{OS}$	Output Common Mode Voltage (Offset Voltage)	1.125	1.2	1.375	V
$\Delta V_{OS}$	Change in $V_{OS}$ between Complimentary Output States			50	mV
$I_{OS}$	Outputs Short Circuit Current, $V_{OUT+}$ or $V_{OUT-} = 0V$ or $V_{DD}$		9	24	mA
$I_{OSD}$	Differential Outputs Short Circuit Current, $V_{OUT+} = V_{OUT-}$		6	12	mA

## Power Supply Characteristics for LVDS Outputs <sup>1</sup>

Symbol	Parameter	Test Conditions <sup>2</sup>	Typ	Max	Unit
$I_{DDQ}$	Quiescent $V_{DD}$ Power Supply Current	REF = LOW Outputs enabled, all outputs unloaded	68	90	mA
$I_{DDD}$	Dynamic $V_{DD}$ Power Supply Current per Output	$V_{DD} = \text{Max.}$ , $C_L = 0\text{pF}$	30	45	$\mu\text{A}/\text{MHz}$
$I_{TOT}$	Total Power $V_{DD}$ Supply Current	$F_{\text{REFERENCE CLOCK}} = 100\text{ MHz}$ , $C_L = 5\text{ pF}$	86	130	mA
		$F_{\text{REFERENCE CLOCK}} = 200\text{ MHz}$ , $C_L = 5\text{ pF}$	100	150	
		$F_{\text{REFERENCE CLOCK}} = 400\text{ MHz}$ , $C_L = 5\text{ pF}$	122	190	

Note 1: Output bank 5 is toggling. Other output banks are powered down.

Note 2: The termination resistors are excluded from these measurements.

## DC Electrical Characteristics for LVPECL

Symbol	Parameter	Min	Typ	Max	Unit
$V_{OH}$	Output Voltage HIGH, terminated through $50\Omega$ tied to $V_{DD}-2\text{ V}$	$V_{DD}-1.2$		$V_{DD}-0.9$	V
$V_{OL}$	Output Voltage LOW, terminated through $50\Omega$ tied to $V_{DD}-2\text{ V}$	$V_{DD}-1.95$		$V_{DD}-1.61$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing	0.55		0.93	V

## Power Supply Characteristics for LVPECL Outputs <sup>1</sup>

Symbol	Parameter	Test Conditions <sup>2</sup>	Typ	Max	Unit
$I_{DDQ}$	Quiescent $V_{DD}$ Power Supply Current	REF = LOW Outputs enabled, all outputs unloaded	86	110	mA
$I_{DDD}$	Dynamic $V_{DD}$ Power Supply Current per Output	$V_{DD} = \text{Max.}$ , $C_L = 0\text{pF}$	35	50	$\mu\text{A}/\text{MHz}$

Symbol	Parameter	Test Conditions <sup>2</sup>	Typ	Max	Unit
$I_{TOT}$	Total Power $V_{DD}$ Supply Current	$F_{REFERENCE\ CLOCK} = 100\ MHz, C_L = 5\ pF$	120	180	mA
		$F_{REFERENCE\ CLOCK} = 200\ MHz, C_L = 5\ pF$	130	190	
		$F_{REFERENCE\ CLOCK} = 400\ MHz, C_L = 5\ pF$	140	210	

Note 1: Output bank 5 is toggling. Other output banks are powered down.

Note 2: The termination resistors are excluded from these measurements.

## DC Electrical Characteristics for HCSL

Symbol	Parameter	Min	Typ	Max	Unit
$V_{OH}$	Output Voltage HIGH	660	700	850	mV
$V_{OL}$	Output Voltage LOW	-150	0	27	mV
Crossing Point Voltage	Absolute	250	350	550	mV

## Power Supply Characteristics for HCSL Outputs <sup>1</sup>

Symbol	Parameter	Test Conditions <sup>2</sup>	Typ	Max	Unit
$I_{DDQ}$	Quiescent $V_{DD}$ Power Supply Current	REF = LOW Outputs enabled, all outputs unloaded	68	90	mA
$I_{DDD}$	Dynamic $V_{DD}$ Power Supply Current per Output	$V_{DD} = \text{Max.}, C_L = 0\ pF$	30	45	$\mu A/MHz$
$I_{TOT}$	Total Power $V_{DD}$ Supply Current	$F_{REFERENCE\ CLOCK} = 100\ MHz, C_L = 5\ pF$	86	130	mA
		$F_{REFERENCE\ CLOCK} = 200\ MHz, C_L = 5\ pF$	100	150	
		$F_{REFERENCE\ CLOCK} = 400\ MHz, C_L = 5\ pF$	122	190	

Note 1: Output bank 5 is toggling. Other output banks are powered down.

Note 2: The termination resistors are excluded from these measurements.

## AC Timing Electrical Characteristics

(Spread Spectrum Generation = OFF)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$f_{IN}^1$	Input Frequency	Input frequency limit (CLKIN)	1		200	MHz
		Input frequency limit (XIN/REF)	8		100	MHz
1 / t1	Output Frequency	Single ended clock output limit (LVTTTL)	0.001		200	MHz
		Differential clock output limit (LVPECL/ LVDS/HCSL)	0.001		500	
$f_{VCO}$	VCO Frequency	VCO operating frequency range	100		1200	MHz
$f_{PFD}$	PFD Frequency	PFD operating frequency range	0.5 <sup>1</sup>		100	MHz
$f_{BW}$	Loop Bandwidth	Based on loop filter resistor and capacitor values	0.01		10	MHz
t2	Input Duty Cycle	Duty Cycle for input	40		60	%
t3	Output Duty Cycle	Measured at $V_{DD}/2$ , all outputs except Reference output	45		55	%
		Measured at $V_{DD}/2$ , Reference output	40		60	%
t4 <sup>2</sup>	Slew Rate, SLEW[1:0] = 00	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of $V_{DD}$ (Output Load = 15 pF)		3.5		V/ns
	Slew Rate, SLEW[1:0] = 01	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of $V_{DD}$ (Output Load = 15 pF)		2.75		
	Slew Rate, SLEW[1:0] = 10	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of $V_{DD}$ (Output Load = 15 pF)		2		
	Slew Rate, SLEW[1:0] = 11	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of $V_{DD}$ (Output Load = 15 pF)		1.25		
t5	Rise Times	LVDS, 20% to 80%		600		ps
	Fall Times	LVDS, 80% to 20%		600		
	Rise Times	LVPECL, 20% to 80%		600		ps
	Fall Times	LVPECL, 80% to 20%		600		
	Rise Times	HCSL, From 0.175 V to 0.525 V	175	400	700	ps
	Fall Times	HCSL, From 0.525 V to 0.175 V	175	400	700	

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t <sub>7</sub>	Clock Jitter	Peak-to-peak period jitter, 1PLL, multiple output frequencies switching, LVTTTL outputs		80	100	ps
		Peak-to-peak period jitter, all 4 PLLs on, LVTTTL outputs <sup>3</sup>		200	270	ps
		Peak-to-peak period jitter, 1PLL, multiple output frequencies switching, LVPECL, LVDS or HCSL outputs		60	80	ps
		Peak-to-peak period jitter, all 4 PLLs on, LVPECL, LVDS or HCSL outputs		120	160	ps
t <sub>8</sub>	Output Skew	Skew between output to output on the same bank			75	ps
t <sub>9</sub> <sup>4</sup>	Lock Time	PLL lock time from power-up		10	20	ms
t <sub>10</sub> <sup>5</sup>	Lock Time	PLL lock time from shutdown mode			2	ms

1. Practical lower frequency is determined by loop filter settings.

2. A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.

3. Jitter measured with clock outputs of 27 MHz, 48 MHz, 24.576 MHz, 74.25 MHz and 25 MHz.

4. Includes loading the configuration bits from EEPROM to PLL registers. It does not include EEPROM programming/write time.

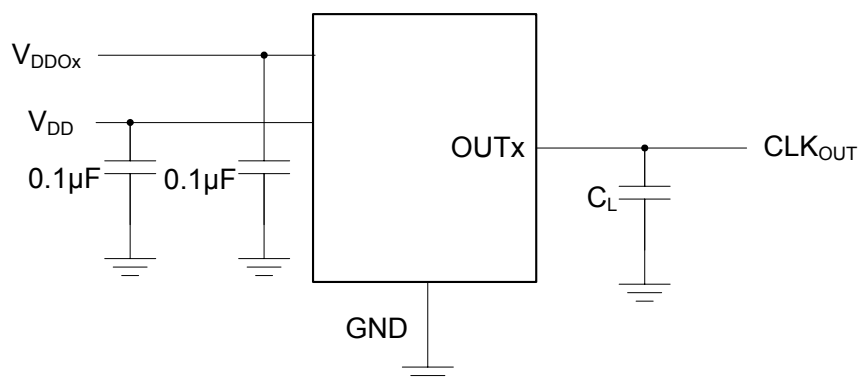
5. Actual PLL lock time depends on the loop configuration.

## Spread Spectrum Generation Specifications

Symbol	Parameter	Description	Min	Typ	Max	Unit
f <sub>IN</sub> <sup>1</sup>	Input Frequency	Input Frequency Limit	1		400	MHz
f <sub>MOD</sub>	Mod Frequency	Modulation Frequency		33		kHz
f <sub>SPREAD</sub>	Spread Value	Amount of Spread Value (programmable) - Down Spread	Programmable			%f <sub>OUT</sub>
		Amount of Spread Value (programmable) - Center Spread	Programmable			

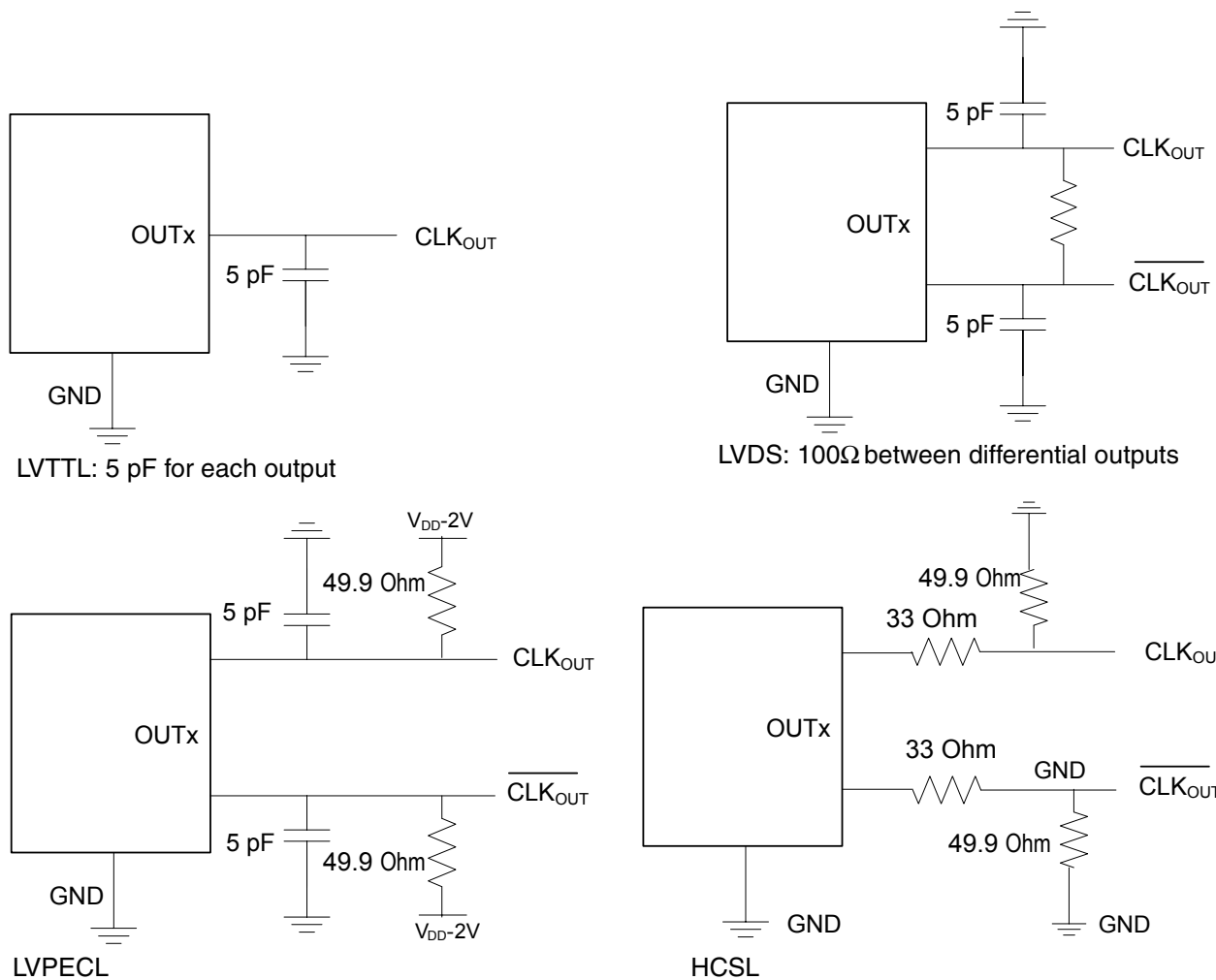
1. Practical lower frequency is determined by loop filter settings.

## Test Circuits and Conditions



Test Circuits for DC Outputs

## Other Termination Scheme (Block Diagram)





## Programming Registers Table

Addr	Default Register Hex Value	Bit #								Description
		7	6	5	4	3	2	1	0	
0x00	00	Reserved							HW/SW	Hardware/Software Mode control HW/SW - 0=HW, 1=SW
0x01	00	Reserved					SEL[2:0]			SEL[2:0] - selects configuration in SW mode
0x02	02	SP	OE6	OE5	OE4	OE3	OE2	OE1	OE0	OE=Output Power Suspend function for OUTx ('1'=OUTx will be suspended on SD/OE pin. Disable mode is defined by OEMx bits), '0'=outputs enabled and no association with OE pin (default).
0x03	02	Reserved	OS*[6:0]							OS*[6:0] - output suspend, active low. Overwrites OE setting.
0x04	0F	SH	Reserved			PLLS*[3:0]				PLLS*[3:0] - PLL Suspend, active low SH - shutdown/OE configuration
0x05	04	Reserved			XTCLKSEL		Reserved			XTCLKSEL - crystal/clock select. 0=Crytal, 1=ICLK
0x06	00	Reserved								
0x07	00	Reserved			XTAL[4:0]				XTAL[4:0] - crystal cap	
0x08	00	Reserved								
0x09	00	Reserved								
0x0A	10	CZ0_CFG4	IP0[2:0]_CFG4			RZ0[3:0]_CFG4				PLL0 loop parameter
0x0B	10	CZ0_CFG5	IP0[2:0]_CFG5			RZ0[3:0]_CFG5				
0x0C	10	CZ0_CFG0	IP0[2:0]_CFG0			RZ0[3:0]_CFG0				
0x0D	10	CZ0_CFG1	IP0[2:0]_CFG1			RZ0[3:0]_CFG1				
0x0E	10	CZ0_CFG2	IP0[2:0]_CFG2			RZ0[3:0]_CFG2				
0x0F	10	CZ0_CFG3	IP0[2:0]_CFG3			RZ0[3:0]_CFG3				
0x10	00	Reserved	D0[6:0]_CFG0							
0x11	00	Reserved	D0[6:0]_CFG1							
0x12	00	Reserved	D0[6:0]_CFG2							
0x13	00	Reserved	D0[6:0]_CFG3							
0x14	00	Reserved	D0[6:0]_CFG4							
0x15	00	Reserved	D0[6:0]_CFG5							
0x16	01	N0[7:0]_CFG4							N - Feedback Divider 2 - 4095 (values of "0" and "1" are not allowed) Total feedback with A, using provided calculation	
0x17	01	N0[7:0]_CFG5								
0x18	01	N0[7:0]_CFG0								
0x19	01	N0[7:0]_CFG1								
0x1A	01	N0[7:0]_CFG2								
0x1B	01	N0[7:0]_CFG3								
0x1C	00	A0[3:0]_CFG0				N0[11:8]_CFG0				
0x1D	00	A0[3:0]_CFG1				N0[11:8]_CFG1				
0x1E	00	A0[3:0]_CFG2				N0[11:8]_CFG2				
0x1F	00	A0[3:0]_CFG3				N0[11:8]_CFG3				
0x20	00	A0[3:0]_CFG4				N0[11:8]_CFG4				
0x21	00	A0[3:0]_CFG5				N0[11:8]_CFG5				
0x22	10	CZ1_CFG4	IP1[2:0]_CFG4			RZ1[3:0]_CFG4				PLL1 Loop Parameter
0x23	10	CZ1_CFG5	IP1[2:0]_CFG5			RZ1[3:0]_CFG5				
0x24	10	CZ1_CFG0	IP1[2:0]_CFG0			RZ1[3:0]_CFG0				
0x25	10	CZ1_CFG1	IP1[2:0]_CFG1			RZ1[3:0]_CFG1				
0x26	10	CZ1_CFG2	IP1[2:0]_CFG2			RZ1[3:0]_CFG2				
0x27	10	CZ1_CFG3	IP1[2:0]_CFG3			RZ1[3:0]_CFG3				

Addr	Default Register Hex Value	Bit #								Description
		7	6	5	4	3	2	1	0	
0x28	00	Reserved	D1[6:0]_CFG0							PLL1 input divider and input sel D1[6:0] - 127 step Ref Div D1 = 0 means power down.
0x29	00	Reserved	D1[6:0]_CFG1							
0x2A	00	Reserved	D1[6:0]_CFG2							
0x2B	00	Reserved	D1[6:0]_CFG3							
0x2C	00	Reserved	D1[6:0]_CFG4							
0x2D	00	Reserved	D1[6:0]_CFG5							
0x2E	01	N1[7:0]_CFG4							N - Feedback Divider 2 - 4095 (value of "0" is not allowed) Total feedback with A, using provided calculation	
0x2F	01	N1[7:0]_CFG5								
0x30	01	N1[7:0]_CFG0								
0x31	01	N1[7:0]_CFG1								
0x32	01	N1[7:0]_CFG2								
0x33	01	N1[7:0]_CFG3								
0x34	00	N3[11:8]_CFG0				N1[11:8]_CFG0				PLL3 Feedback Divider
0x35	00	N3[11:8]_CFG1				N1[11:8]_CFG1				
0x36	00	N3[11:8]_CFG2				N1[11:8]_CFG2				
0x37	00	N3[11:8]_CFG3				N1[11:8]_CFG3				
0x38	00	N3[11:8]_CFG4				N1[11:8]_CFG4				
0x39	00	N3[11:8]_CFG5				N1[11:8]_CFG5				
0x3A	00	CZ2_CFG4	IP2[2:0]_CFG4				RZ2[3:0]_CFG4			PLL2 Loop Parameter
0x3B	00	CZ2_CFG5	IP2[2:0]_CFG5				RZ2[3:0]_CFG5			
0x3C	00	CZ2_CFG0	IP2[2:0]_CFG0				RZ2[3:0]_CFG0			
0x3D	00	CZ2_CFG1	IP2[2:0]_CFG1				RZ2[3:0]_CFG1			
0x3E	00	CZ2_CFG2	IP2[2:0]_CFG2				RZ2[3:0]_CFG2			
0x3F	00	CZ2_CFG3	IP2[2:0]_CFG3				RZ2[3:0]_CFG3			
0x40	00	Reserved	D2[6:0]_CFG0							PLL2 Reference Divide and Input Select D2[6:0] - 127 step Ref Div D2 = 0 means power down.
0x41	00	Reserved	D2[6:0]_CFG1							
0x42	00	Reserved	D2[6:0]_CFG2							
0x43	00	Reserved	D2[6:0]_CFG3							
0x44	00	Reserved	D2[6:0]_CFG4							
0x45	00	Reserved	D2[6:0]_CFG5							
0x46	01	N2[7:0]_CFG4							N2[7:0] - PLL2 Feedback Divider 2 - 4095 (value of "0" is not allowed). (See Addr 0x4C:0x51 for N2[15:8])	
0x47	01	N2[7:0]_CFG5								
0x48	01	N2[7:0]_CFG0								
0x49	01	N2[7:0]_CFG1								
0x4A	01	N2[7:0]_CFG2								
0x4B	01	N2[7:0]_CFG3								
0x4C	80	SSENB_CFG0	0	0	IP3[4]_CFG0	N2[11:8]_CFG0				N2[11:8] - PLL2 Feedback Divide
0x4D	80	SSENB_CFG1	0	0	IP3[4]_CFG1	N2[11:8]_CFG1				PLL3 Spread Spectrum
0x4E	80	SSENB_CFG2	0	0	IP3[4]_CFG2	N2[11:8]_CFG2				SSENB - Spread Spectrum Enable
0x4F	80	SSENB_CFG3	0	0	IP3[4]_CFG3	N2[11:8]_CFG3				SSENB = 1 means ON
0x50	80	SSENB_CFG4	0	0	IP3[4]_CFG4	N2[11:8]_CFG4				IP3[4:0] - PLL3 Charge Pump Current.
0x51	80	SSENB_CFG5	0	0	IP3[4]_CFG5	N2[11:8]_CFG5				
0x52	00	Reserved								
0x53	00	Reserved								
0x54	00	Reserved								
0x55	00	Reserved								

Addr	Default Register Hex Value	Bit #								Description
		7	6	5	4	3	2	1	0	
0x56	00	IP3[3:0]_CFG4				RZ3[3:0]_CFG4				PLL3 Loop Parameter
0x57	00	IP3[3:0]_CFG5				RZ3[3:0]_CFG5				
0x58	00	IP3[3:0]_CFG0				RZ3[3:0]_CFG0				
0x59	00	IP3[3:0]_CFG1				RZ3[3:0]_CFG1				
0x5A	00	IP3[3:0]_CFG2				RZ3[3:0]_CFG2				
0x5B	00	IP3[3:0]_CFG3				RZ3[3:0]_CFG3				
0x5C	03	Reserved	D3[6:0]_CFG0							PLL3 Reference Divide and input sel D3[6:0] - 127 step Ref Div D3 = 0 means power down.
0x5D	03	Reserved	D3[6:0]_CFG1							
0x5E	03	Reserved	D3[6:0]_CFG2							
0x5F	03	Reserved	D3[6:0]_CFG3							
0x60	03	Reserved	D3[6:0]_CFG4							
0x61	03	Reserved	D3[6:0]_CFG5							
0x62	0C	N3[7:0]_CFG4							N - Feedback Divider 12 - 4095 (values of “0” through “11” are not allowed)	
0x63	0C	N3[7:0]_CFG5								
0x64	0C	N3[7:0]_CFG0								
0x65	0C	N3[7:0]_CFG1								
0x66	0C	N3[7:0]_CFG2								
0x67	0C	N3[7:0]_CFG3								
0x68	00	SSVCO[7:0]_CFG0							SSVCO[7:0] - PLL3 Spread Spectrum Loop Feedback Counter See Addr 0x80:0x85 for SSVCO[15:8]	
0x69	00	SSVCO[7:0]_CFG1								
0x6A	00	SSVCO[7:0]_CFG2								
0x6B	00	SSVCO[7:0]_CFG3								
0x6C	00	SSVCO[7:0]_CFG4								
0x6D	00	SSVCO[7:0]_CFG5								
0x6E	00	SS_D3[7:0]_CFG4							SS_D[7:0] - PLL3 Spread Spectrum Reference Divide	
0x6F	00	SS_D3[7:0]_CFG5								
0x70	00	SS_D3[7:0]_CFG0								
0x71	00	SS_D3[7:0]_CFG1								
0x72	00	SS_D3[7:0]_CFG2								
0x73	00	SS_D3[7:0]_CFG3								
0x74	01	Reserved								Reserved
0x75	03	OEM0[1:0]	SLEW0[1:0]		INV0	Reserved	S1	S3	Output Controls S1=1 - OUT1/OUT2 are from DIV1/DIV2 respectively S1=0 - Both from DIV2 S3=1 - OUT3/OUT6 are from DIV3/DIV6 S3=0 - Both from DIV6 SLEW# - LVTTTL only OEM#–output enable mode x0 - tristated 01 - park low 11 - park high OEM0 controls OUT0 only	
0x76	00	OEM1[1:0]	SLEW1[1:0]		INV1[1:0]		LVL1[1:0]		Output Controls LVL1[1:0] - output pair OUT1/OUT2 [00] - LVTTTL [01] - LVDS [10] - LVPECL [11] - HCSL INV1 [CLK1, CLK2] [0] - normal [1] - invert clock OEM1 controls OUT1/OUT2	

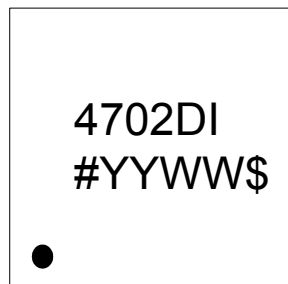
Addr	Default Register Hex Value	Bit #								Description		
		7	6	5	4	3	2	1	0			
0x77	00			SLEW2[1:0]				CMEN3	CMEN1	CMEN# - common mode enable Set to 1 for LVDS Set to 0 for LVTTTL, LVPECL, HCSL		
0x78	00	OEM3[1:0]		SLEW3[1:0]		INV3[1:0]		LVL3[1:0]		OEM3 controls OUT3 and OUT6		
0x79	00	Reserved										
0x7A	00	OEM5[1:0]		SLEW5[1:0]		INV5[1:0]		LVL5[1:0]		OEM5 controls OUT5 and OUT5b		
0x7B	00			SLEW6[1:0]				CMEN5	CMEN4			
0x7C	00	Reserved										
0x7D	00	Reserved										
0x7E	00	Reserved										
0x7F	00	Reserved										
0x80	00	SSVCO[15:8]_CFG0									PLL3 Spread Spectrum Feedback Counter	
0x81	00	SSVCO[15:8]_CFG1										
0x82	00	SSVCO[15:8]_CFG2										
0x83	00	SSVCO[15:8]_CFG3										
0x84	00	SSVCO[15:8]_CFG4										
0x85	00	SSVCO[15:8]_CFG5										
0x86	00	Reserved									Reserved	
0x87	00	Reserved									Reserved	
0x88	FF	PM1_CFG0	Q1[6:0]_CFG0									Output Divides for Q<>111111, PM=0 - Divide by 2 PM=1, (Q+2)*2 for Q=1111111 PM=0, disable the output divider PM=1, bypass the output divide, (divide by 1)
0x89	FF	PM1_CFG1	Q1[6:0]_CFG1									
0x8A	FF	PM1_CFG2	Q1[6:0]_CFG2									
0x8B	FF	PM1_CFG3	Q1[6:0]_CFG3									
0x8C	FF	PM1_CFG4	Q1[6:0]_CFG4									
0x8D	FF	PM1_CFG5	Q1[6:0]_CFG5									
0x8E	7F	PM2_CFG4	Q2[6:0]_CFG4									
0x8F	7F	PM2_CFG5	Q2[6:0]_CFG5									
0x90	7F	PM2_CFG0	Q2[6:0]_CFG0									
0x91	7F	PM2_CFG1	Q2[6:0]_CFG1									
0x92	7F	PM2_CFG2	Q2[6:0]_CFG2									
0x93	7F	PM2_CFG3	Q2[6:0]_CFG3									
0x94	7F	PM3_CFG0	Q3[6:0]_CFG0									
0x95	7F	PM3_CFG1	Q3[6:0]_CFG1									
0x96	7F	PM3_CFG2	Q3[6:0]_CFG2									
0x97	7F	PM3_CFG3	Q3[6:0]_CFG3									
0x98	7F	PM3_CFG4	Q3[6:0]_CFG4									
0x99	7F	PM3_CFG5	Q3[6:0]_CFG5									
0x9A	7F	PM4_CFG4	Q4[6:0]_CFG4									
0x9B	7F	PM4_CFG5	Q4[6:0]_CFG5									
0x9C	7F	PM4_CFG0	Q4[6:0]_CFG0									
0x9D	7F	PM4_CFG1	Q4[6:0]_CFG1									
0x9E	7F	PM4_CFG2	Q4[6:0]_CFG2									
0x9F	7F	PM4_CFG3	Q4[6:0]_CFG3									
0xA0	7F	PM5_CFG0	Q5[6:0]_CFG0									
0xA1	7F	PM5_CFG1	Q5[6:0]_CFG1									
0xA2	7F	PM5_CFG2	Q5[6:0]_CFG2									
0xA3	7F	PM5_CFG3	Q5[6:0]_CFG3									
0xA4	7F	PM5_CFG4	Q5[6:0]_CFG4									
0xA5	7F	PM5_CFG5	Q5[6:0]_CFG5									
0xA6	7F	PM6_CFG4	Q6[6:0]_CFG4									

Addr	Default Register Hex Value	Bit #								Description	
		7	6	5	4	3	2	1	0		
0xA7	7F	PM6_CFG5	Q6[6:0]_CFG5								
0xA8	7F	PM6_CFG0	Q6[6:0]_CFG0								
0xA9	7F	PM6_CFG1	Q6[6:0]_CFG1								
0xAA	7F	PM6_CFG2	Q6[6:0]_CFG2								
0xAB	7F	PM6_CFG3	Q6[6:0]_CFG3								
0xAC	00	TSSC[3:0]_CFG0				NSSC[3:0]_CFG0				PLL0 Spread Spectrum Control	
0xAD	00	TSSC[3:0]_CFG1				NSSC[3:0]_CFG1					
0xAE	00	TSSC[3:0]_CFG2				NSSC[3:0]_CFG2					
0xAF	00	TSSC[3:0]_CFG3				NSSC[3:0]_CFG3					
0xB0	00	TSSC[3:0]_CFG4				NSSC[3:0]_CFG4					
0xB1	00	TSSC[3:0]_CFG5				NSSC[3:0]_CFG5					
0xB2	00	DITH_CFG4	X2_CFG4	SSOFFSET[5:0]_CFG4							
0xB3	00	DITH_CFG5	X2_CFG5	SSOFFSET[5:0]_CFG5							
0xB4	00	DITH_CFG0	X2_CFG0	SSOFFSET[5:0]_CFG0							
0xB5	00	DITH_CFG1	X2_CFG1	SSOFFSET[5:0]_CFG1							
0xB6	00	DITH_CFG2	X2_CFG2	SSOFFSET[5:0]_CFG2							
0xB7	00	DITH_CFG3	X2_CFG3	SSOFFSET[5:0]_CFG3							
0xB8	11	SD1[3:0]_CFG0				SD0[3:0]_CFG0					
0xB9	11	SD1[3:0]_CFG1				SD0[3:0]_CFG1					
0xBA	11	SD1[3:0]_CFG2				SD0[3:0]_CFG2					
0xBB	11	SD1[3:0]_CFG3				SD0[3:0]_CFG3					
0xBC	11	SD1[3:0]_CFG4				SD0[3:0]_CFG4					
0xBD	11	SD1[3:0]_CFG5				SD0[3:0]_CFG5					
0xBE	AE	SRC1[1:0]_CFG4		SRC0[1:0]_CFG4		PDPL3_CFG4	SM[1:0]_CFG4		PRIMSRC_CFG4	Output Divide Source Selection	
0xBF	AE	SRC1[1:0]_CFG5		SRC0[1:0]_CFG5		PDPL3_CFG5	SM[1:0]_CFG5		PRIMSRC_CFG5	PRIMSRC - primary source - crystal or ICLOCK 0 = crystal/REFIN 1 = CLKIN	
0xC0	AE	SRC1[1:0]_CFG0		SRC0[1:0]_CFG0		PDPL3_CFG0	SM[1:0]_CFG0		PRIMSRC_CFG0	SM = switch mode 0x = manual 10 = reserved 11 = auto-revertive	
0xC1	AE	SRC1[1:0]_CFG1		SRC0[1:0]_CFG1		PDPL3_CFG1	SM[1:0]_CFG1		PRIMSRC_CFG1	PDPL3 - PLL3 shutdown 0 = normal 1 = shut down	
0xC2	AE	SRC1[1:0]_CFG2		SRC0[1:0]_CFG2		PDPL3_CFG2	SM[1:0]_CFG2		PRIMSRC_CFG2	SRC = MUX control bit prior to DIV# SRC0[1:0] 00 - DIV1 01 - DIV3 10 - Reference input	
0xC3	AE	SRC1[1:0]_CFG3		SRC0[1:0]_CFG3		PDPL3_CFG3	SM[1:0]_CFG3		PRIMSRC_CFG3		
0xC4	24	Reserved	SRC3[2:0]_CFG0			SRC2[2:0]_CFG0			SRC1[2]_CFG0	SRC1/SRC2/SRC3..SRC5 000 - DIV1 001 - DIV3 010 - Reference input 011 - Reserved 100 - PLL0 101 - PLL1 110 - PLL2 111 - PLL3	
0xC5	24		SRC3[2:0]_CFG1			SRC2[2:0]_CFG1			SRC1[2]_CFG1		
0xC6	24		SRC3[2:0]_CFG2			SRC2[2:0]_CFG2			SRC1[2]_CFG2		
0xC7	24		SRC3[2:0]_CFG3			SRC2[2:0]_CFG3			SRC1[2]_CFG3		
0xC8	24		SRC3[2:0]_CFG4			SRC2[2:0]_CFG4			SRC1[2]_CFG4		
0xC9	24		SRC3[2:0]_CFG5			SRC2[2:0]_CFG5			SRC1[2]_CFG5		

Addr	Default Register Hex Value	Bit #								Description
		7	6	5	4	3	2	1	0	
0xCA	49	SRC6[2:0]_CFG4			SRC5[2:0]_CFG4			Reserved		SRC6 000 - Reserved 001 - Reserved 010 - Reference input 011 - Reserved 100 - Reserved 101 - PLL1 110 - Reserved 111 - Reserved Quiet MUX
0xCB	49	SRC6[2:0]_CFG5			SRC5[2:0]_CFG5					
0xCC	49	SRC6[2:0]_CFG0			SRC5[2:0]_CFG0					
0xCD	49	SRC6[2:0]_CFG1			SRC5[2:0]_CFG1					
0xCE	49	SRC6[2:0]_CFG2			SRC5[2:0]_CFG2					
0xCF	49	SRC6[2:0]_CFG3			SRC5[2:0]_CFG3					

Default Configuration: OUT1 = Reference Clock output, all other outputs turned off.

## Marking Diagram



### Notes:

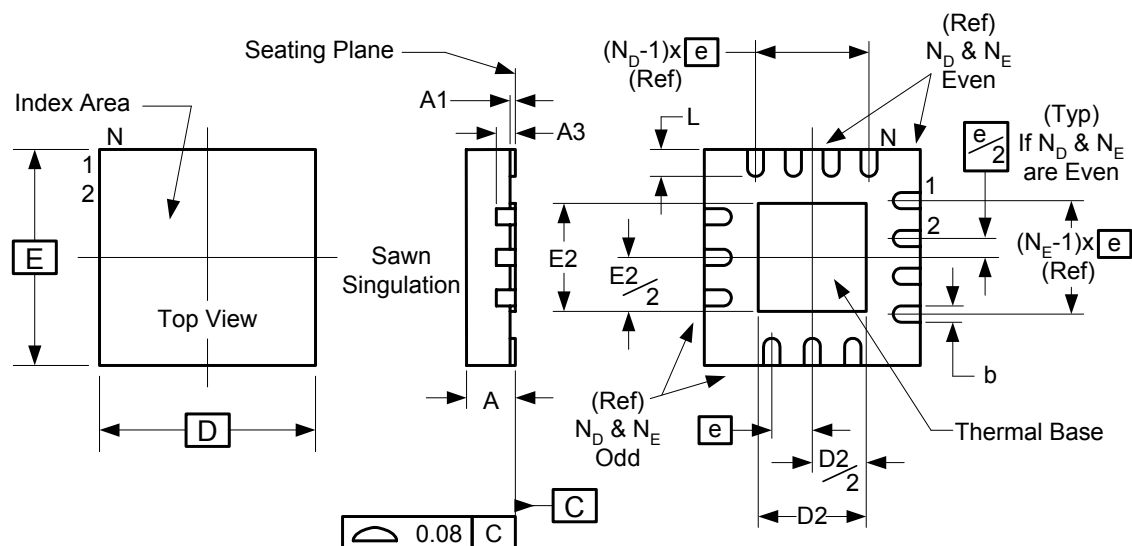
1. “#” is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “\$” is the assembly mark code.
4. “I” at the end of part number indicates industrial temperature range.
5. Bottom marking: country of origin if not USA.

## Thermal Characteristics 28-pin QFN

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	$\theta_{JA}$	Still air		47.0		°C/W
	$\theta_{JA}$	1 m/s air flow		41.8		°C/W
	$\theta_{JA}$	2.5 m/s air flow		39.2		°C/W
Thermal Resistance Junction to Case	$\theta_{JC}$			52.9		°C/W

## Package Outline and Package Dimensions (28-pin 4mm x 4mm QFN)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters	
	Min	Max
A	0.80	1.00
A1	0	0.05
A3	0.20 Reference	
b	0.15	0.25
e	0.40 BASIC	
N	28	
$N_D$	7	
$N_E$	7	
D x E BASIC	4.00 x 4.00	
D2	2.50	2.70
E2	2.50	2.70
L	0.30	0.50

## Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5V49EE702NDGI	See Page 30	Tubes	28-pin QFN	-40 to +85° C
5V49EE702NDGI8	See Page 30	Tape and Reel	28-pin QFN	-40 to +85° C

“G” after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

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## Revision History

Rev.	Originator	Date	Description of Change
A	R.Willner	4/27/09	Advance Information.
B	R.Willner	5/04/09	Identified VDDX (crystal oscillator power) and AVDD (analog power) on device.
C	R.Willner	6/04/09	Add default configurations, pull-down resistor values on input pins. Released Datasheet from Advanced Information.
D	R.Willner	06/10/09	Updates: crystal load specs; "Output Duty Cycle" specs; addresses 0x07, 0x02 and 0xBF in "Programming Registers" table.
E	R.Willner	10/06/09	Changed IP3[3:0] to IP3[4:0] ; updated "Programming Registers Table".
F	R.Willner	02/23/10	Updated Recommended Operation Conditions to include Vddx and AVdd parameters.

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