SN74AUP1G74 Low-Power Single Positive-Edge-Triggered D-Type Flip-Flop With Clear and Preset

1 Features

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption: I_{CC} = 0.9 µA Maximum
- Low Dynamic-Power Consumption: C_{pd} = 5.5 pF Typical at 3.3 V
- Low Input Capacitance: C_i = 1.5 pF Typical
- Low Noise – Overshoot and Undershoot < 10% of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the Input (V_{hys} = 250 mV Typical at 3.3 V)
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- t_{pd} = 5 ns Maximum at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

3 Description

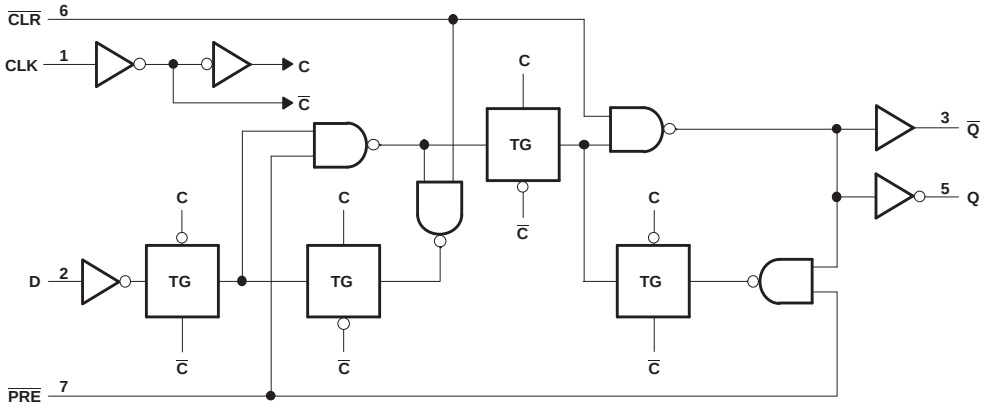
The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life. This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in Figure 6).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1G74YFP	DSBGA (8)	1.56 mm × 0.76 mm
SN74AUP1G74YZP	DSBGA (8)	1.86 mm × 0.89 mm
SN74AUP1G74DCU	VSSOP (8)	2.30 mm × 2.00 mm
SN74AUP1G74DQE	X2SON (8)	1.40 mm × 1.00 mm
SN74AUP1G74RSE	UQFN (8)	1.50 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

AUP – The Lowest-Power Family



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2010) to Revision D **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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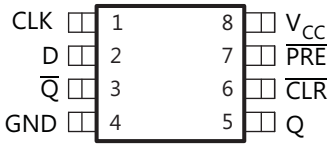
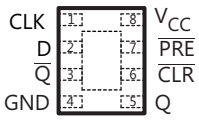
5 Pin Configuration and Functions

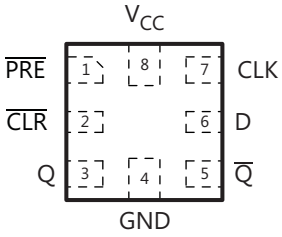
DCU Package
8-Pin VSSOP
Top View



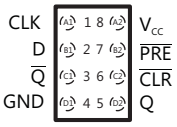
DQE Package
8-Pin X2SON
Top View



RSE Package
8-Pin UQFN
Top View



YFP or YZP Package
8-Pin DSBGA
Top View



Pin Functions[1]

PIN				I/O	DESCRIPTION
NAME	VSSOP, X2SON	UQFN	DSBGA		
CLK	1	7	A1	I	Rising edge triggered clock signal input
$\overline{CLR}$	6	2	C2	I	Clear, Active low
D	2	6	B1	I	Data input
GND	4	4	D1	—	Ground
$\overline{PRE}$	7	1	B2	I	Preset, Active low
Q	5	3	D2	O	Output
$\overline{Q}$	3	5	C1	O	Inverted output
V_{CC}	8	8	A2	—	Power supply

(1) See *Mechanical, Packaging, and Orderable Information* for dimensions.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)		–0.5	4.6	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
V_O	Output voltage in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.7 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.6		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.3 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.9	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 0.8 V		–20	μA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		–4	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

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Recommended Operating Conditions[1] (continued)

			MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	μA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		SN74AUP1G74				UNIT
		DCU (VSSOP)	DQE (X2SON)	RSE (UQFN)	YFP/YZP (DSBGA)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	227	261	253	102	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics, T_A = 25°C

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –20 μA	0.8 V to 3.6 V	V_{CC} – 0.1			V
		I_{OH} = –1.1 mA	1.1 V	0.7 × V_{CC}			
		I_{OH} = –1.7 mA	1.4 V	1.11			
		I_{OH} = –1.9 mA	1.65 V	1.32			
		I_{OH} = –2.3 mA	2.3 V	2.05			
		I_{OH} = –3.1 mA		1.9			
		I_{OH} = –2.7 mA	3 V	2.72			
		I_{OH} = –4 mA		2.6			
V_{OL}		I_{OL} = 20 μA	0.8 V to 3.6 V			0.1	V
		I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}	
		I_{OL} = 1.7 mA	1.4 V			0.31	
		I_{OL} = 1.9 mA	1.65 V			0.31	
		I_{OL} = 2.3 mA	2.3 V			0.31	
		I_{OL} = 3.1 mA				0.44	
		I_{OL} = 2.7 mA	3 V			0.31	
		I_{OL} = 4 mA				0.44	
I_I	A or B input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1	μA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.2	μA
$ΔI_{off}$		V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2	μA
I_{CC}		V_I = GND or (V_{CC} to 3.6 V), I_O = 0	0.8 V to 3.6 V			0.5	μA
$ΔI_{CC}$		V_I = V_{CC} – 0.6 V[1], I_O = 0	3.3 V			40	μA
C_i		V_I = V_{CC} or GND	0 V		1.5		pF
			3.6 V		1.5		
C_o		V_O = GND	0 V		3		pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND

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6.6 Electrical Characteristics, T_A = –40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –20 µA	0.8 V to 3.6 V	V_{CC} – 0.1			V
		I_{OH} = –1.1 mA	1.1 V	0.7 × V_{CC}			
		I_{OH} = –1.7 mA	1.4 V	1.03			
		I_{OH} = –1.9 mA	1.65 V	1.3			
		I_{OH} = –2.3 mA	2.3 V	1.97			
		I_{OH} = –3.1 mA		1.85			
		I_{OH} = –2.7 mA	3 V	2.67			
		I_{OH} = –4 mA		2.55			
V_{OL}		I_{OL} = 20 µA	0.8 V to 3.6 V			0.1	V
		I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}	
		I_{OL} = 1.7 mA	1.4 V			0.37	
		I_{OL} = 1.9 mA	1.65 V			0.35	
		I_{OL} = 2.3 mA	2.3 V			0.33	
		I_{OL} = 3.1 mA				0.45	
		I_{OL} = 2.7 mA	3 V			0.33	
		I_{OL} = 4 mA				0.45	
I_I	A or B input	V_I = GND to 3.6 V	0 V to 3.6 V			0.5	µA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.6	µA
ΔI_{off}		V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.6	µA
I_{CC}		V_I = GND or (V_{CC} to 3.6 V), I_O = 0	0.8 V to 3.6 V			0.9	µA
ΔI_{CC}		V_I = V_{CC} – 0.6 V(1), I_O = 0	3.3 V			50	µA
C_i		V_I = V_{CC} or GND	0 V				pF
			3.6 V				
C_o		V_O = GND	0 V				pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND

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6.7 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

			V_{CC}	MIN(1)	TYP(2)	MAX(1)	UNIT
f_{clock}	Clock frequency		0.8 V		21		MHz
			1.2 V ± 0.1 V			40	
			1.5 V ± 0.1 V			50	
			1.8 V ± 0.15 V			60	
			2.5 V ± 0.2 V			90	
			3.3 V ± 0.3 V			90	
t_w	Pulse duration	CLK high or low	0.8 V		3.5		ns
			1.2 V ± 0.1 V	2			
			1.5 V ± 0.1 V	2			
			1.8 V ± 0.15 V	2			
			2.5 V ± 0.2 V	2			
			3.3 V ± 0.3 V	2			
		$\overline{PRE}$ or $\overline{CLR}$ low	0.8 V		4.5		
			1.2 V ± 0.1 V	2			
			1.5 V ± 0.1 V	2			
			1.8 V ± 0.15 V	2			
			2.5 V ± 0.2 V	2			
			3.3 V ± 0.3 V	2			
t_{su}	Setup time before CLK↑	Data high	0.8 V		3		ns
			1.2 V ± 0.1 V	1.3			
			1.5 V ± 0.1 V	1			
			1.8 V ± 0.15 V	1			
			2.5 V ± 0.2 V	0.5			
			3.3 V ± 0.3 V	0.5			
		Data low	0.8 V		1		
			1.2 V ± 0.1 V	1.2			
			1.5 V ± 0.1 V	1			
			1.8 V ± 0.15 V	1			
			2.5 V ± 0.2 V	1			
			3.3 V ± 0.3 V	1			
		$\overline{PRE}$ or $\overline{CLR}$ inactive	0.8 V		1		
			1.2 V ± 0.1 V	0.5			
			1.5 V ± 0.1 V	0.5			
			1.8 V ± 0.15 V	0.5			
			2.5 V ± 0.2 V	0.5			
			3.3 V ± 0.3 V	0.5			
t_h	Hold time, data after CLK↑		0.8 V		0		ns
			1.2 V ± 0.1 V	0			
			1.5 V ± 0.1 V	0			
			1.8 V ± 0.15 V	0			
			2.5 V ± 0.2 V	0			
			3.3 V ± 0.3 V	0			

(1) Minimum and maximum values are for T_A = –40°C to +85°C
(2) Typicals are for T_A = 25°C

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6.8 Switching Characteristics, C_L = 5 pF

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A	MIN	TYP	MAX	UNIT
f_{max}			0.8 V	T_A = 25°C		60		MHz
			1.2 V ± 0.1 V	T_A = 25°C		80		
				T_A = –40°C to 85°C	60			
			1.5 V ± 0.1 V	T_A = 25°C		125		
				T_A = –40°C to 85°C	90			
			1.8 V ± 0.15 V	T_A = 25°C		150		
				T_A = –40°C to 85°C	120			
			2.5 V ± 0.2 V	T_A = 25°C		180		
				T_A = –40°C to 85°C	160			
			3.3 V ± 0.3 V	T_A = 25°C		190		
				T_A = –40°C to 85°C	180			
t_{pd}	CLK	Q	0.8 V	T_A = 25°C		31		ns
			1.2 V ± 0.1 V	T_A = 25°C	2	10	20	
				T_A = –40°C to 85°C	2.7		20.4	
			1.5 V ± 0.1 V	T_A = 25°C	2	6	12	
				T_A = –40°C to 85°C	1.9		12.4	
			1.8 V ± 0.15 V	T_A = 25°C	2	5	9	
				T_A = –40°C to 85°C	1.4		9.5	
			2.5 V ± 0.2 V	T_A = 25°C	2	3	6	
				T_A = –40°C to 85°C	1.1		6.2	
			3.3 V ± 0.3 V	T_A = 25°C	2	3	4	
				T_A = –40°C to 85°C	1		4.7	
		$\overline{Q}$	0.8 V	T_A = 25°C		28		
			1.2 V ± 0.1 V	T_A = 25°C	2	9	19	
				T_A = –40°C to 85°C	2.4		19	
			1.5 V ± 0.1 V	T_A = 25°C	2	6	11	
				T_A = –40°C to 85°C	1.6		11.8	
			1.8 V ± 0.15 V	T_A = 25°C	2	5	9	
				T_A = –40°C to 85°C	1.3		9	
			2.5 V ± 0.2 V	T_A = 25°C	2	3	6	
				T_A = –40°C to 85°C	1.1		6	
			3.3 V ± 0.3 V	T_A = 25°C	2	3	4	
				T_A = –40°C to 85°C	1		4.6	
	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	0.8 V	T_A = 25°C		26		
			1.2 V ± 0.1 V	T_A = 25°C	2	9	20	
				T_A = –40°C to 85°C	2		20	
			1.5 V ± 0.1 V	T_A = 25°C	2	6	12	
				T_A = –40°C to 85°C	1.5		13	
			1.8 V ± 0.15 V	T_A = 25°C	2	5	9	
				T_A = –40°C to 85°C	1.3		10	
			2.5 V ± 0.2 V	T_A = 25°C	2	3	6	
				T_A = –40°C to 85°C	1		7	
			3.3 V ± 0.3 V	T_A = 25°C	2	3	5	
				T_A = –40°C to 85°C	1		5	

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6.9 Switching Characteristics, C_L = 10 pF

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A	MIN	TYP	MAX	UNIT
f_{max}			0.8 V	T_A = 25°C		46		MHz
			1.2 V ± 0.1 V	T_A = 25°C		65		
				T_A = –40°C to 85°C	50			
			1.5 V ± 0.1 V	T_A = 25°C		95		
				T_A = –40°C to 85°C	55			
			1.8 V ± 0.15 V	T_A = 25°C		110		
				T_A = –40°C to 85°C	60			
			2.5 V ± 0.2 V	T_A = 25°C		170		
				T_A = –40°C to 85°C	130			
			3.3 V ± 0.3 V	T_A = 25°C		180		
				T_A = –40°C to 85°C	160			
t_{pd}	CLK	Q	0.8 V	T_A = 25°C		33		ns
			1.2 V ± 0.1 V	T_A = 25°C	2	10	22	
				T_A = –40°C to 85°C	3.4		21.8	
			1.5 V ± 0.1 V	T_A = 25°C	2	7	13	
				T_A = –40°C to 85°C	2.4		13.5	
			1.8 V ± 0.15 V	T_A = 25°C	2	6	10	
				T_A = –40°C to 85°C	1.9		10.4	
			2.5 V ± 0.2 V	T_A = 25°C	2	4	6	
				T_A = –40°C to 85°C	1.5		7	
			3.3 V ± 0.3 V	T_A = 25°C	2	3	5	
				T_A = –40°C to 85°C	1.2		5.3	
		$\overline{Q}$	0.8 V	T_A = 25°C		30		
			1.2 V ± 0.1 V	T_A = 25°C	2	10	20	
				T_A = –40°C to 85°C	3		20.3	
			1.5 V ± 0.1 V	T_A = 25°C	2	7	12	
				T_A = –40°C to 85°C	2.2		12.8	
			1.8 V ± 0.15 V	T_A = 25°C	2	5	9	
				T_A = –40°C to 85°C	1.8		9.9	
			2.5 V ± 0.2 V	T_A = 25°C	2	4	6	
				T_A = –40°C to 85°C	1.3		6.7	
			3.3 V ± 0.3 V	T_A = 25°C	2	3	5	
				T_A = –40°C to 85°C	1.1		5.2	
	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	0.8 V	T_A = 25°C		29		
			1.2 V ± 0.1 V	T_A = 25°C	2	10	21	
				T_A = –40°C to 85°C	2		21.4	
			1.5 V ± 0.1 V	T_A = 25°C	2	7	13	
				T_A = –40°C to 85°C	2		13.8	
			1.8 V ± 0.15 V	T_A = 25°C	2	5	10	
				T_A = –40°C to 85°C	2		10.8	
			2.5 V ± 0.2 V	T_A = 25°C	2	4	7	
				T_A = –40°C to 85°C	1.5		7.4	
			3.3 V ± 0.3 V	T_A = 25°C	2	3	5	
				T_A = –40°C to 85°C	1.5		5.8	

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6.10 Switching Characteristics, C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A	MIN	TYP	MAX	UNIT
f_{max}			0.8 V	T_A = 25°C		41		MHz
			1.2 V ± 0.1 V	T_A = 25°C		75		
				T_A = –40°C to 85°C	50			
			1.5 V ± 0.1 V	T_A = 25°C		95		
				T_A = –40°C to 85°C	55			
			1.8 V ± 0.15 V	T_A = 25°C		100		
				T_A = –40°C to 85°C	60			
			2.5 V ± 0.2 V	T_A = 25°C		150		
				T_A = –40°C to 85°C	130			
			3.3 V ± 0.3 V	T_A = 25°C		200		
				T_A = –40°C to 85°C	160			
t_{pd}	CLK	Q	0.8 V	T_A = 25°C		35		ns
			1.2 V ± 0.1 V	T_A = 25°C	2	12	23.1	
				T_A = –40°C to 85°C	4.1		23.2	
			1.5 V ± 0.1 V	T_A = 25°C	2	8	14.1	
				T_A = –40°C to 85°C	2.9		14.6	
			1.8 V ± 0.15 V	T_A = 25°C	2	6	10.7	
				T_A = –40°C to 85°C	2.4		11.3	
			2.5 V ± 0.2 V	T_A = 25°C	2	4	7	
				T_A = –40°C to 85°C	1.9		7.6	
			3.3 V ± 0.3 V	T_A = 25°C	2	4	5.4	
				T_A = –40°C to 85°C	1.6		5.9	
		$\overline{Q}$	0.8 V	T_A = 25°C		32		
			1.2 V ± 0.1 V	T_A = 25°C	2	11	21.8	
				T_A = –40°C to 85°C	3.7		21.8	
			1.5 V ± 0.1 V	T_A = 25°C	2	7	13.5	
				T_A = –40°C to 85°C	2.6		14	
			1.8 V ± 0.15 V	T_A = 25°C	2	6	10.4	
				T_A = –40°C to 85°C	2.2		10.9	
			2.5 V ± 0.2 V	T_A = 25°C	2	4	7.1	
				T_A = –40°C to 85°C	1.7		7.5	
			3.3 V ± 0.3 V	T_A = 25°C	2	3	5.4	
				T_A = –40°C to 85°C	1.4		5.8	
	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	0.8 V	T_A = 25°C		31		
			1.2 V ± 0.1 V	T_A = 25°C	2	11	23	
				T_A = –40°C to 85°C	2		22.9	
			1.5 V ± 0.1 V	T_A = 25°C	2	7	14	
				T_A = –40°C to 85°C	2		14.9	
			1.8 V ± 0.15 V	T_A = 25°C	2	6	11	
				T_A = –40°C to 85°C	2		11.7	
			2.5 V ± 0.2 V	T_A = 25°C	2	4	7	
				T_A = –40°C to 85°C	2		8.1	
			3.3 V ± 0.3 V	T_A = 25°C	2	4	6	
				T_A = –40°C to 85°C	1.5		6.4	

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6.11 Switching Characteristics, C_L = 30 pF

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A	MIN	TYP	MAX	UNIT
f_{max}			0.8 V	T_A = 25°C		21		MHz
			1.2 V ± 0.1 V	T_A = 25°C		50		
				T_A = –40°C to 85°C	40			
			1.5 V ± 0.1 V	T_A = 25°C		60		
				T_A = –40°C to 85°C	50			
			1.8 V ± 0.15 V	T_A = 25°C		75		
				T_A = –40°C to 85°C	70			
			2.5 V ± 0.2 V	T_A = 25°C		100		
				T_A = –40°C to 85°C	90			
			3.3 V ± 0.3 V	T_A = 25°C		100		
				T_A = –40°C to 85°C	90			
t_{pd}	CLK	Q	0.8 V	T_A = 25°C		32		ns
			1.2 V ± 0.1 V	T_A = 25°C	3	14	27	
				T_A = –40°C to 85°C	5.9		27	
			1.5 V ± 0.1 V	T_A = 25°C	3	10	17	
				T_A = –40°C to 85°C	4.4		17.2	
			1.8 V ± 0.15 V	T_A = 25°C	3	8	13	
				T_A = –40°C to 85°C	3.6		13.4	
			2.5 V ± 0.2 V	T_A = 25°C	3	6	9	
				T_A = –40°C to 85°C	3		9.2	
			3.3 V ± 0.3 V	T_A = 25°C	3	5	7	
				T_A = –40°C to 85°C	2.6		7.2	
		$\overline{Q}$	0.8 V	T_A = 25°C		40		
			1.2 V ± 0.1 V	T_A = 25°C	3	13	26	
				T_A = –40°C to 85°C	5.5		25.9	
			1.5 V ± 0.1 V	T_A = 25°C	3	9	16	
				T_A = –40°C to 85°C	4.1		16.8	
			1.8 V ± 0.15 V	T_A = 25°C	3	7	13	
				T_A = –40°C to 85°C	3.5		13.2	
			2.5 V ± 0.2 V	T_A = 25°C	3	5	9	
				T_A = –40°C to 85°C	2.7		9.2	
			3.3 V ± 0.3 V	T_A = 25°C	3	5	7	
				T_A = –40°C to 85°C	2.4		7.2	
	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	0.8 V	T_A = 25°C		38		
			1.2 V ± 0.1 V	T_A = 25°C	3	13	26	
				T_A = –40°C to 85°C	3		27	
			1.5 V ± 0.1 V	T_A = 25°C	3	9	17	
				T_A = –40°C to 85°C	3		17.4	
			1.8 V ± 0.15 V	T_A = 25°C	3	8	13	
				T_A = –40°C to 85°C	3		14	
			2.5 V ± 0.2 V	T_A = 25°C	3	6	9	
				T_A = –40°C to 85°C	3		10	
			3.3 V ± 0.3 V	T_A = 25°C	3	5	7	
				T_A = –40°C to 85°C	2.5		8	

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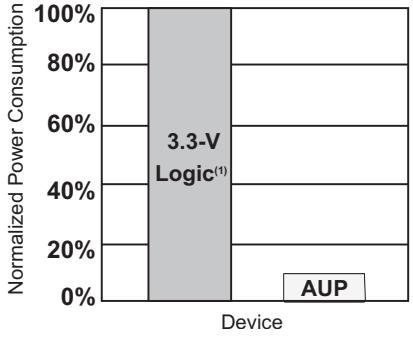
6.12 Operating Characteristics

T_A = 25°C

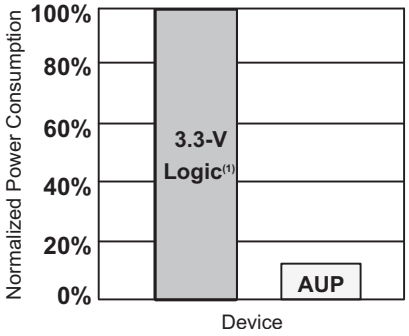
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	5.5	pF
			1.2 V ± 0.1 V	5.5	
			1.5 V ± 0.1 V	5.5	
			1.8 V ± 0.15 V	5.5	
			2.5 V ± 0.2 V	5.5	
			3.3 V ± 0.3 V	5.5	

6.13 Typical Characteristics



(1) Single, dual and triple gates

Figure 1. Static Power Consumption for AUP Devices (µA)



(1) Single, dual and triple gates

Figure 2. Dynamic Power Consumption for AUP Devices (pF)

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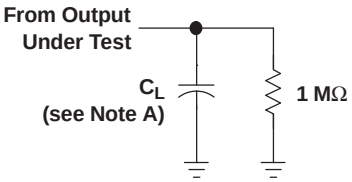
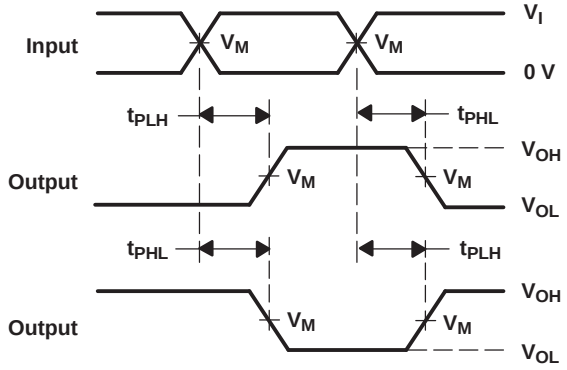
7 Parameter Measurement Information

7.1 Propagation Delays, Setup and Hold Times, and Pulse Width)

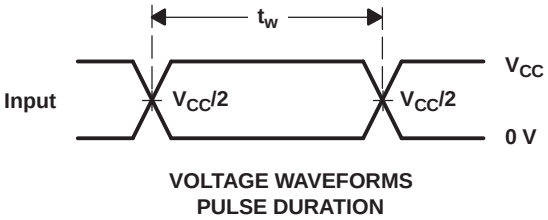


LOAD CIRCUIT

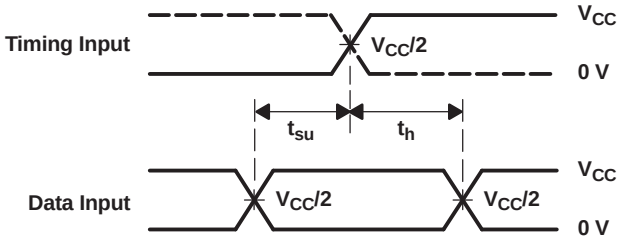
	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION

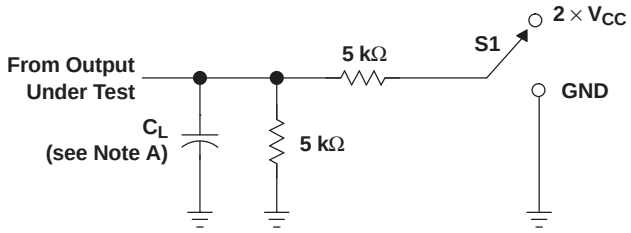


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

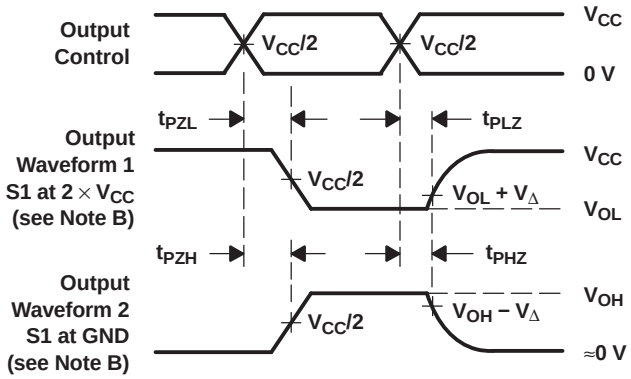
7.2 Enable and Disable Times



TEST	S1
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	$2 \times V_{CC}$ GND

LOAD CIRCUIT

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

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8 Detailed Description

8.1 Overview

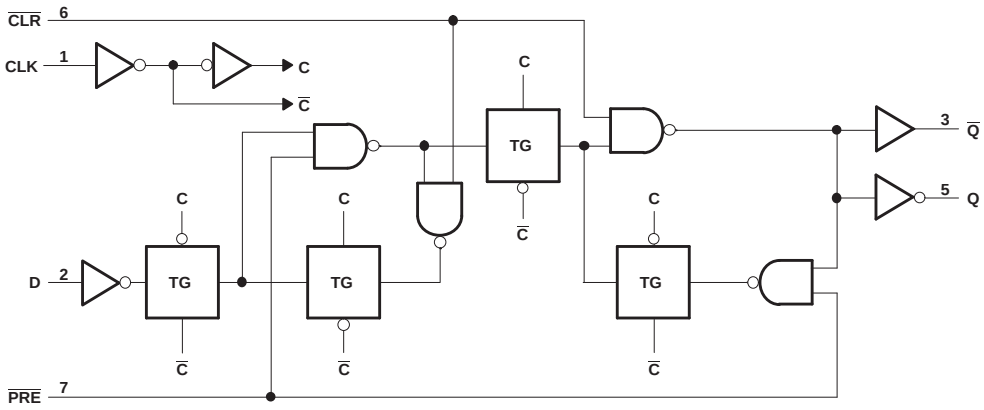
This single positive-edge-triggered D-type flip-flop is designed for 0.8-V to 3.6-V V_{CC} operation.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs. When both the $\overline{CLR}$ and $\overline{PRE}$ inputs are set low, the $\overline{CLR}$ input will override the $\overline{PRE}$ input.

NanoStar package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram



Pin numbers shown are for the DCU and DQE packages

8.3 Feature Description

This device is available in the Texas Instrument's NanoStar package. It has low static-power consumption of 0.9 uA maximum. It has low noise with overshoot and undershoot at less than ten percent of V_{CC}. It supports partial-power-down mode operation, which is specified by I_{off}. The Schmitt-trigger inputs allow for slow or noisy input signals. The device has a wide operating voltage range of 0.8 V to 3.6 V, and is optimized for 3.3 V. It has low propagation delay of 5 ns maximum at 3.3 V.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74AUP1G74.

Table 1. Function Table

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
X	L	X	X	L	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AUP1G74 can be used to control a power button input. Tying $\overline{Q}$ to D will switch the output between high and low each time that a high signal is sent to CLK from the push button.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The resistor and capacitor at the $\overline{CLR}$ pin are optional. If they are not used, the $\overline{CLR}$ pin must be connected directly to V_{CC} to be inactive.

9.2 Typical Power Button Circuit

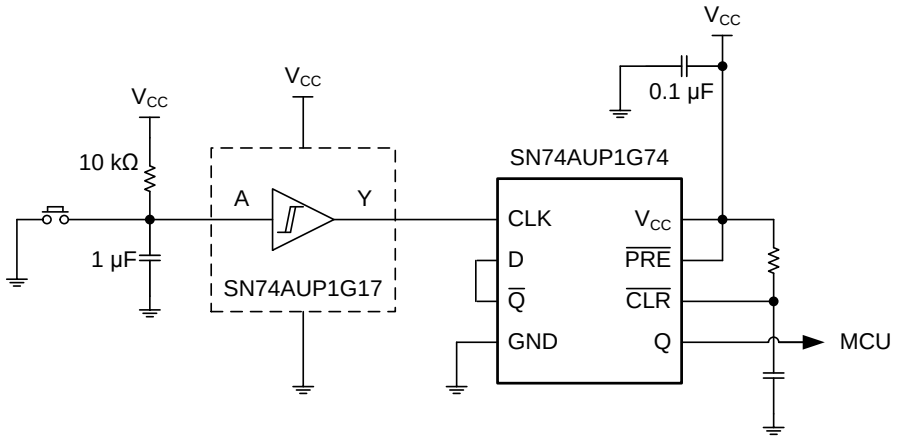

Figure 5. Device Power Button Circuit

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see (Δt/ΔV) in *Recommended Operating Conditions*.
   - For specified high and low levels, see (V_{IH} and V_{IL}) in Recommended Operating Conditions.
   - Inputs are overvoltage tolerant allowing them to go as high as 4.6 V at any valid V_{CC}.
2. Recommend Output Conditions:
   - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

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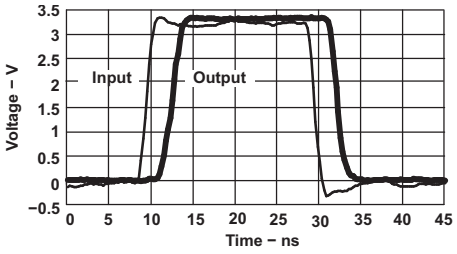
Typical Power Button Circuit (continued)

9.2.3 Application Curve



AUP1G08 data at C_L = 15 pF

Figure 6. Switching Characteristics at 25 MHz

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-μF capacitor, and if there are multiple V_{CC} pins, then TI recommends a 0.01-μF or 0.022-μF capacitor for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

11.2 Layout Example

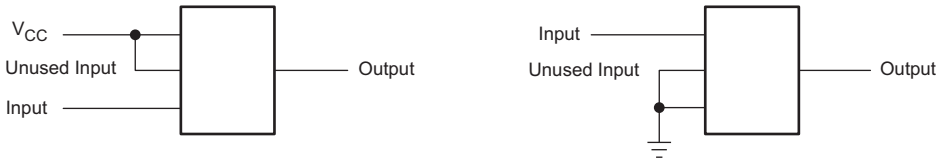


Figure 7. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

NanoStar, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G74DCUR	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H74R	Samples
SN74AUP1G74DCURG4	ACTIVE	VSSOP	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H74R	Samples
SN74AUP1G74DQER	ACTIVE	X2SON	DQE	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HS	Samples
SN74AUP1G74RSER	ACTIVE	UQFN	RSE	8	5000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HS	Samples
SN74AUP1G74YFPR	ACTIVE	DSBGA	YFP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HSN	Samples
SN74AUP1G74YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(HS7 ~ HSN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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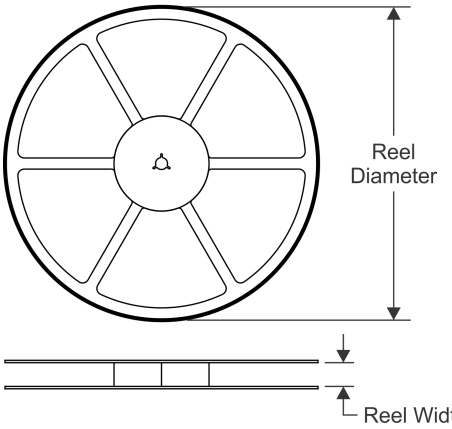
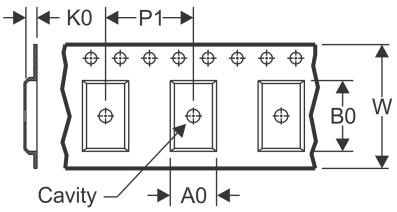
TAPE AND REEL INFORMATION

REEL DIMENSIONS

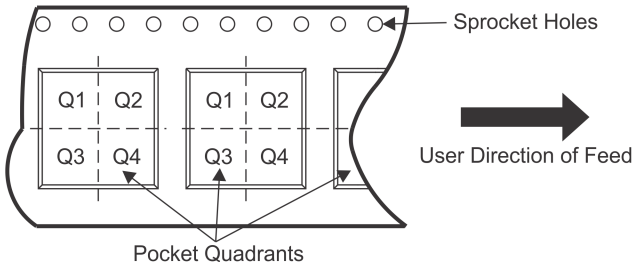


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

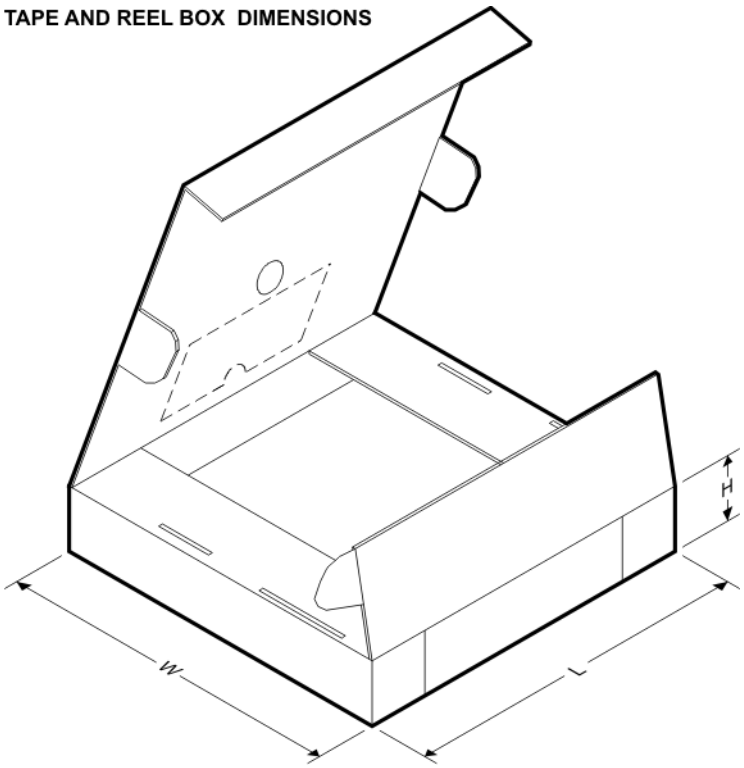
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G74DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP1G74DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
SN74AUP1G74RSER	UQFN	RSE	8	5000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
SN74AUP1G74YFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1
SN74AUP1G74YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

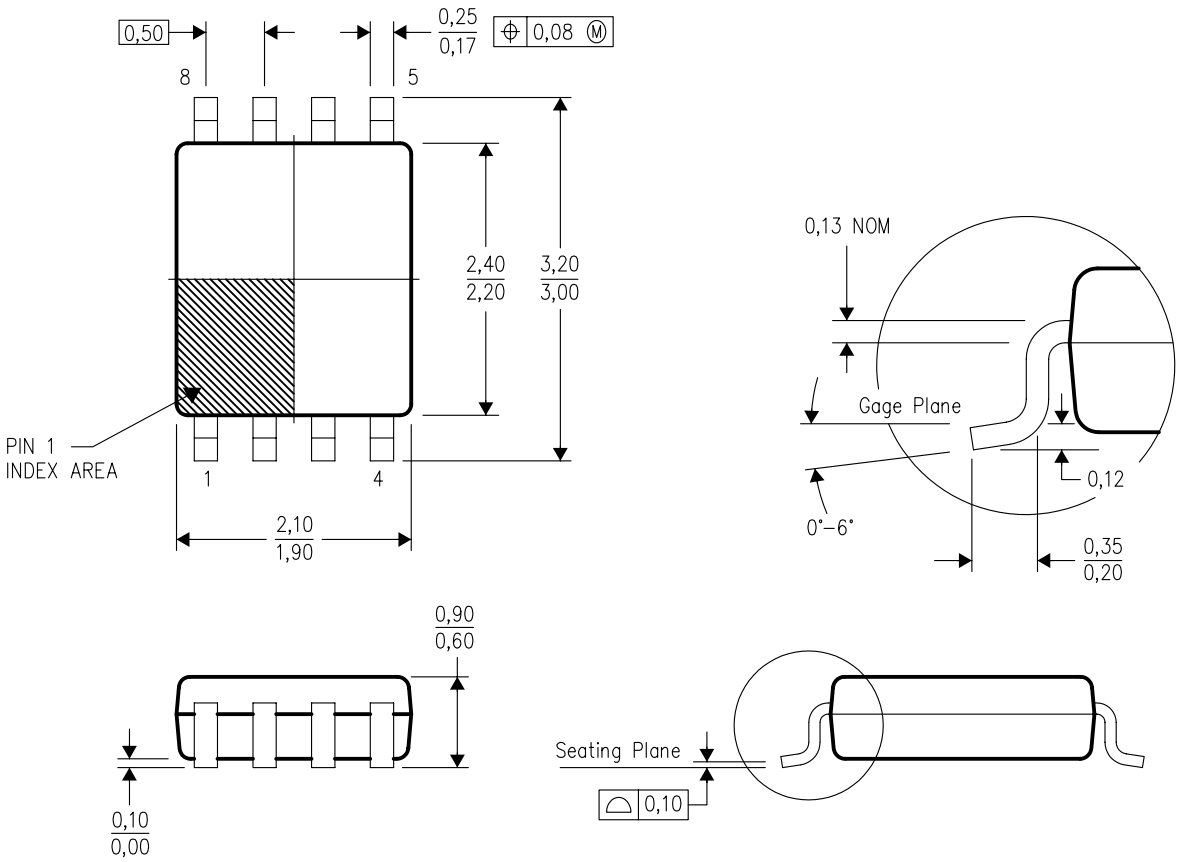
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G74DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP1G74DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AUP1G74RSER	UQFN	RSE	8	5000	202.0	201.0	28.0
SN74AUP1G74YFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0
SN74AUP1G74YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

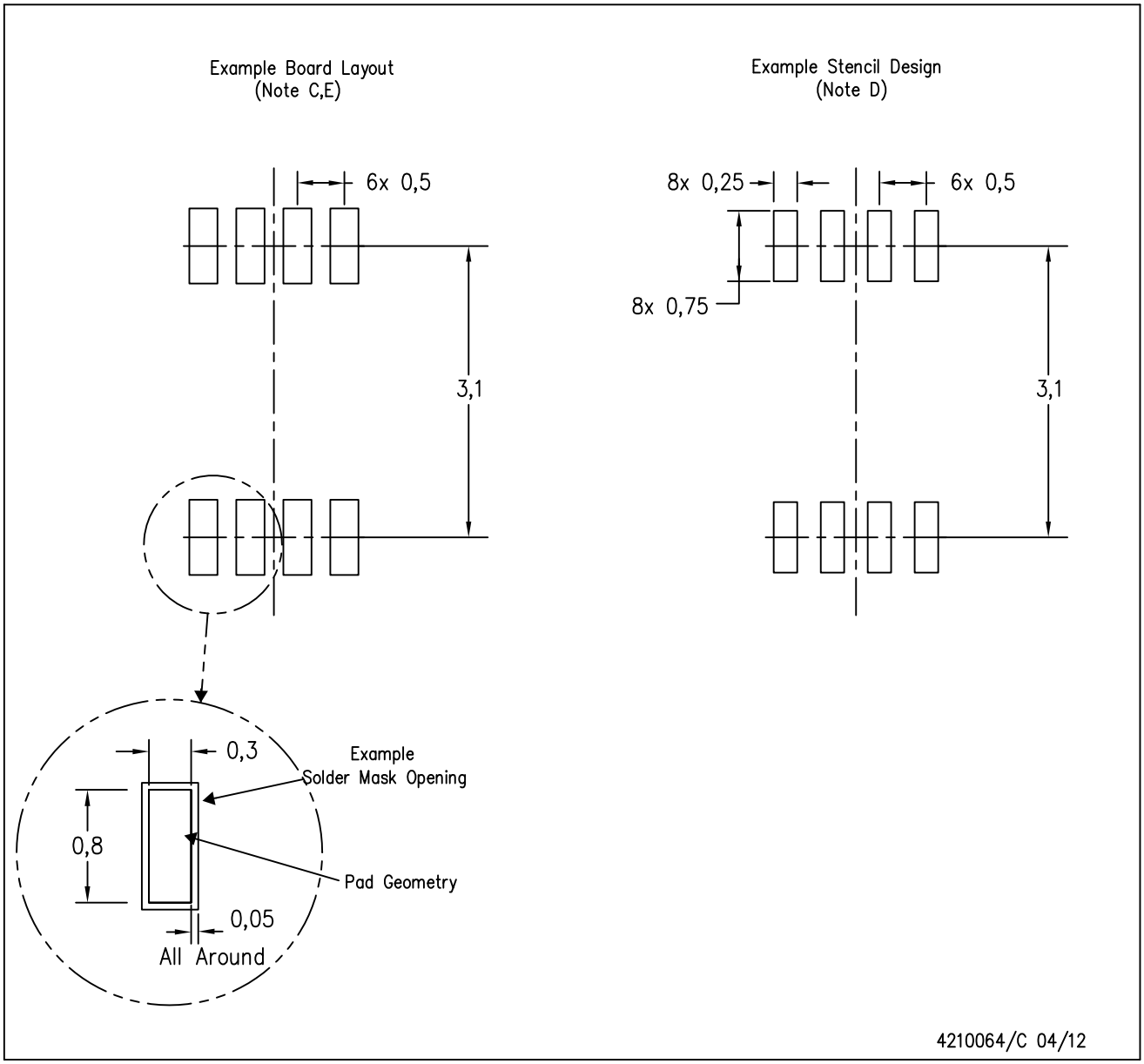
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4200503/F 07/05

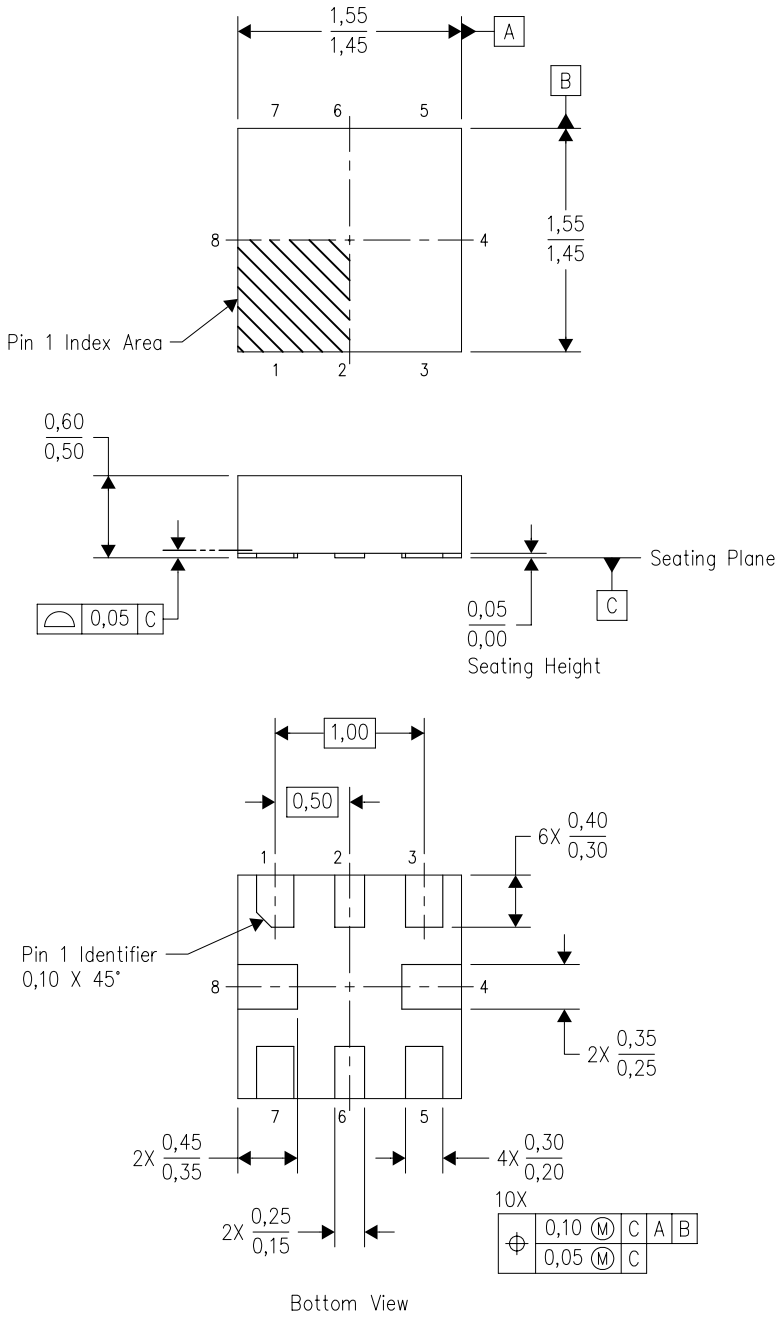
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSE (S–PUQFN–N8) PLASTIC QUAD FLATPACK NO–LEAD

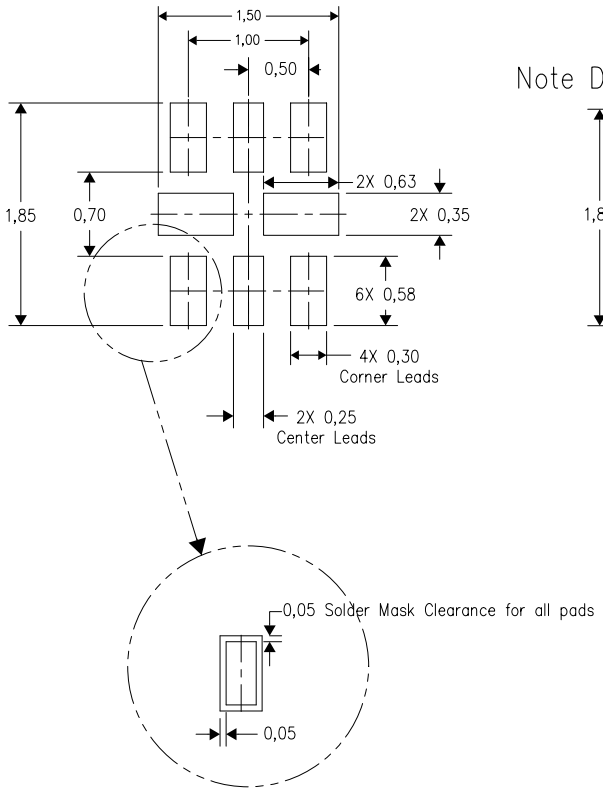


4207268–2/D 01/11

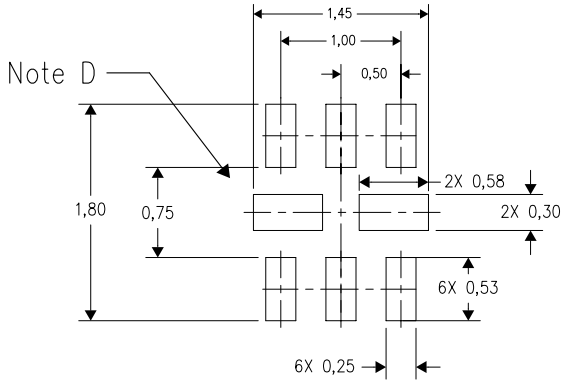
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UECD.

RSE (S–PUQFN–N8) PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout



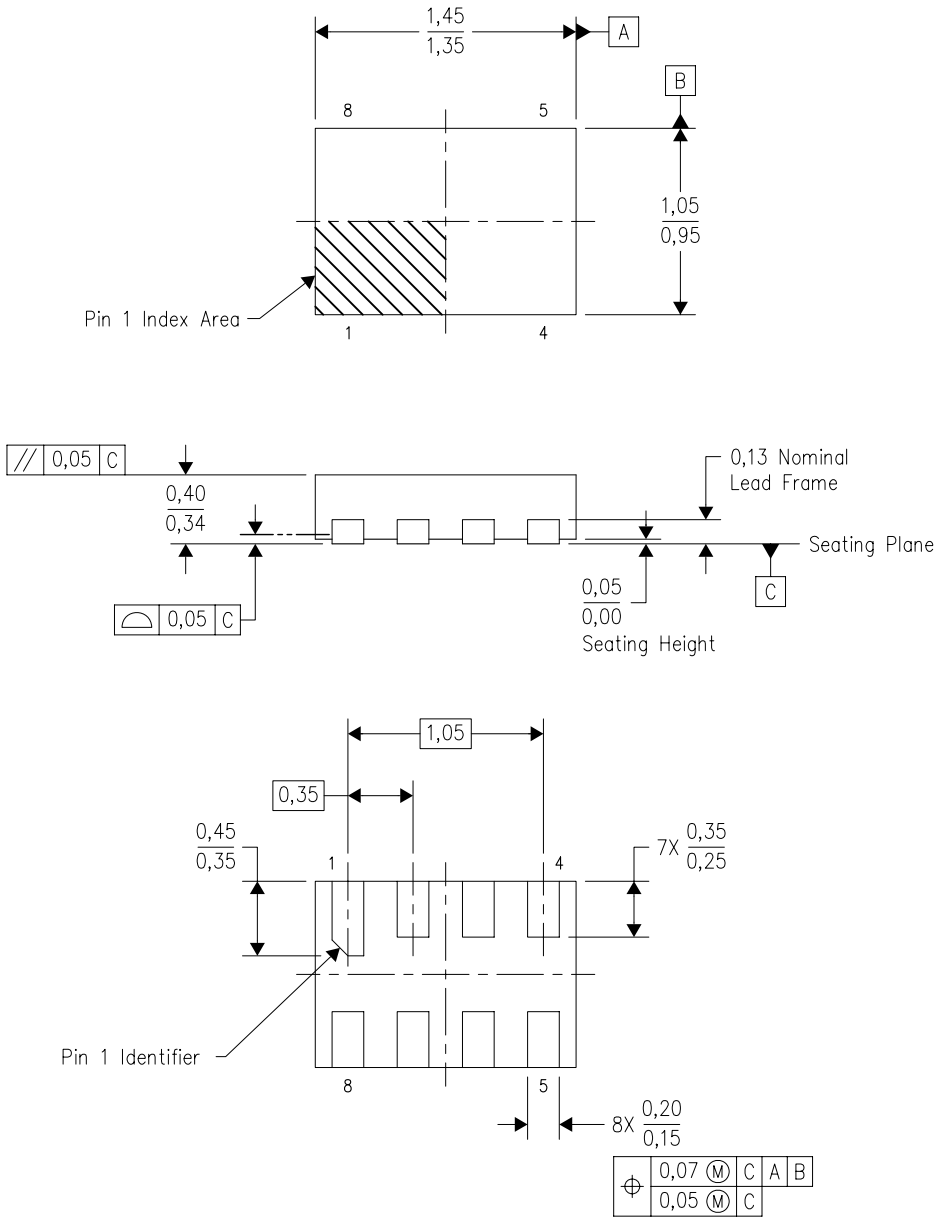
Example Stencil Design
(Note E)



4208106–2/E 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

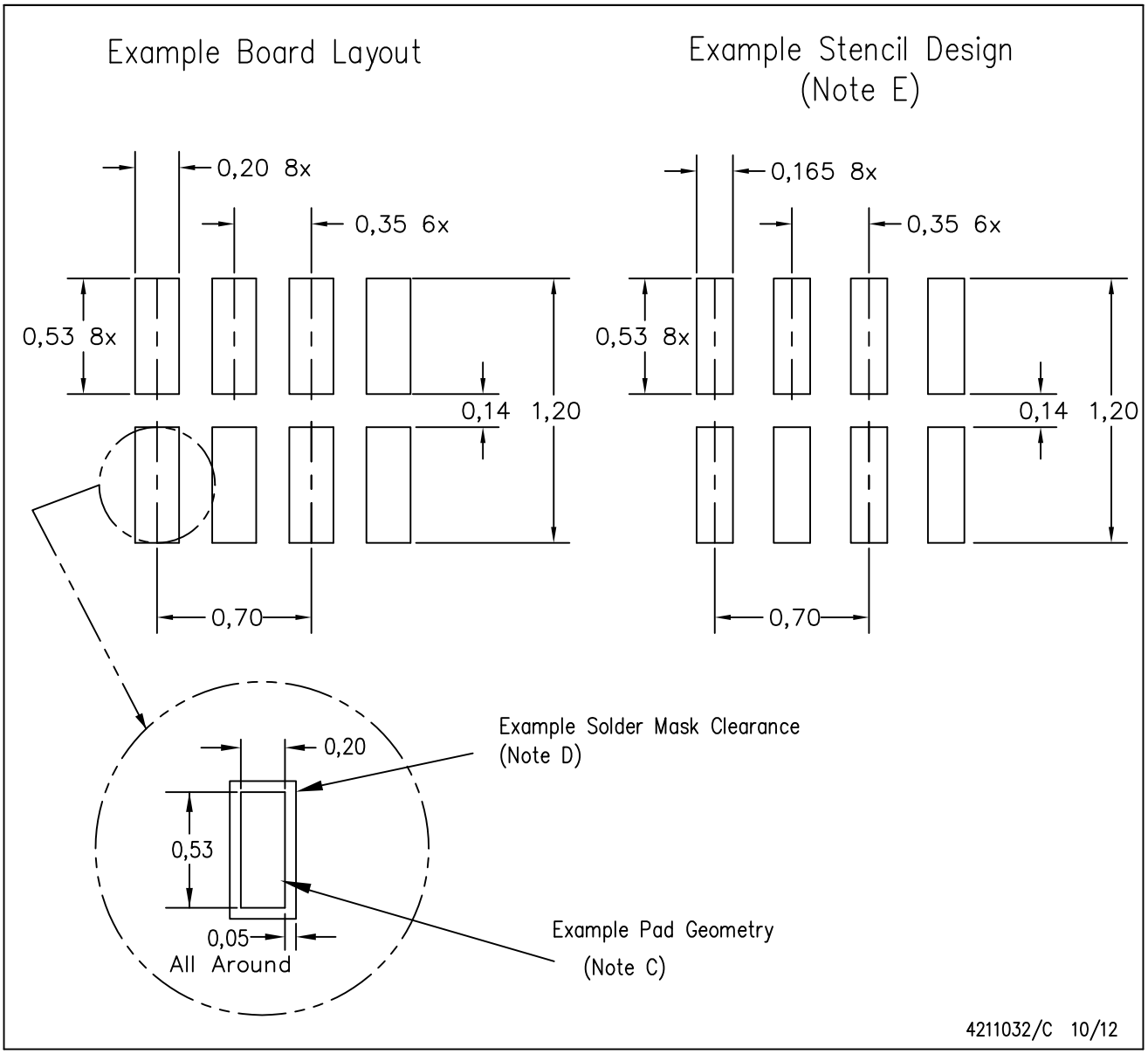
DQE (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4209779/B 10/2008

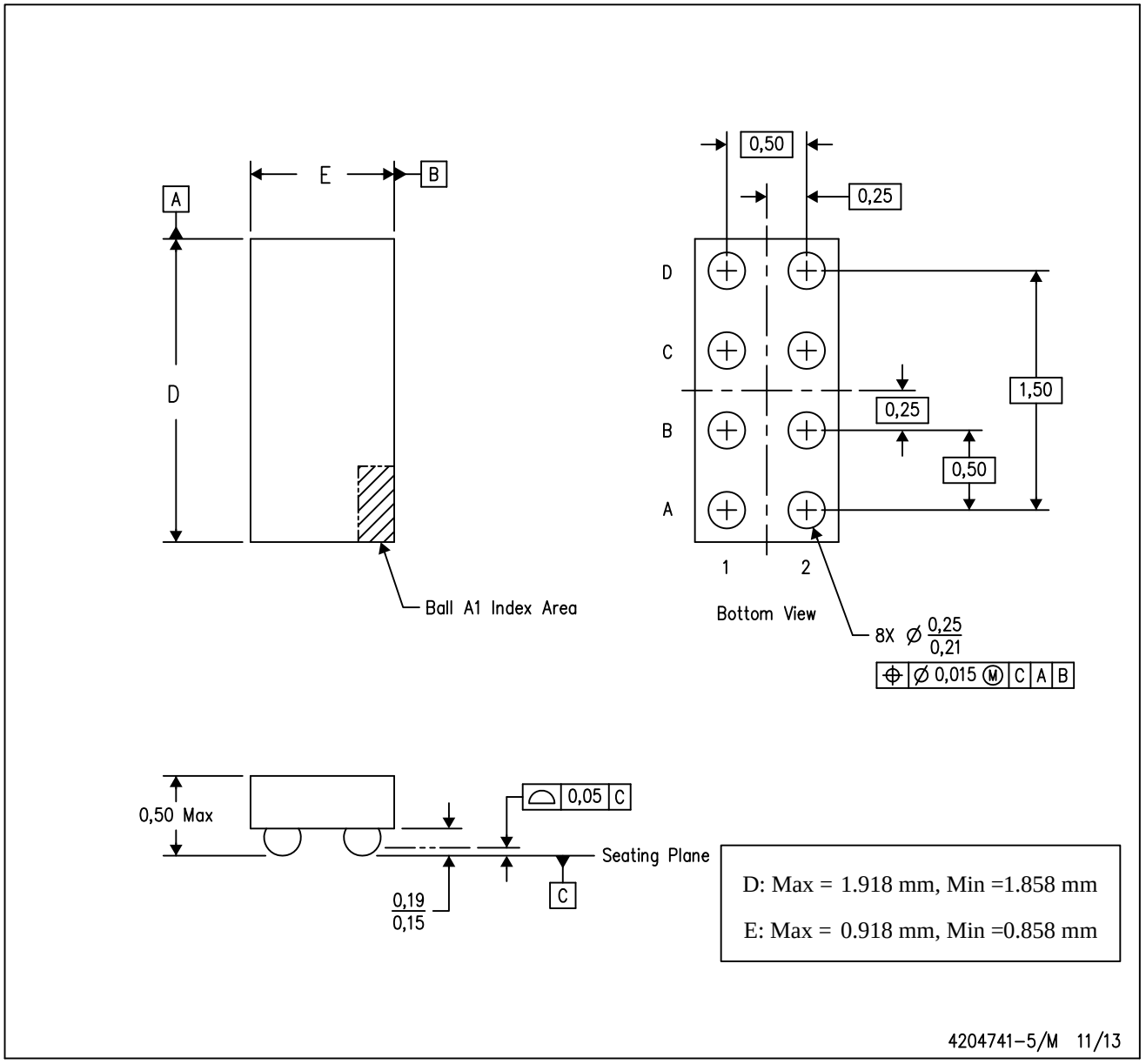
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. This package complies to JEDEC MO–287 variation X2EAF.

DQE (R–PX2SON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Over–printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
I. Component placement force should be minimized to prevent excessive paste block deformation.

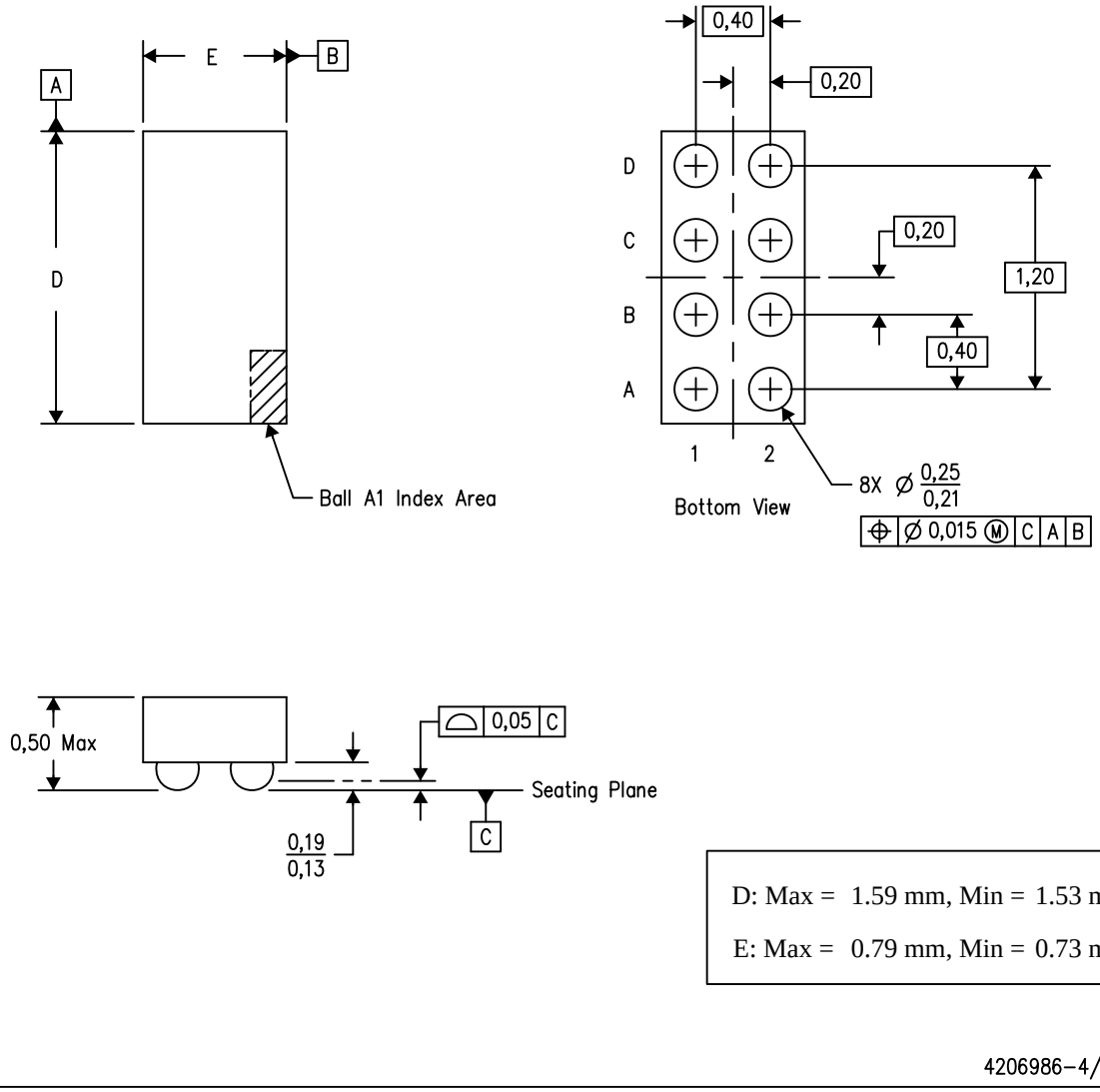
YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

YFP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

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