

# Hot Swappable 2-Wire Bus Buffer with Low Voltage Level Translation

## FEATURES

- Level Translates 1V Signals to Standard 3.3V and 5V Logic Rails
- Allows Bus Pull-Up Voltages as Low as 1V on SDAIN and SCLIN
- Bidirectional Buffer\* for SDA and SCL Lines Increases Fanout
- Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Backplane
- Isolates Input SDA and SCL Line from Output
- 10kV Human Body Model ESD Protection
- Supports Clock Stretching, Arbitration and Synchronization
- High Impedance SDA, SCL Pins for  $V_{CC} = 0V$
- $\overline{CS}$  Gates Connection from Input to Output
- Compatible with I<sup>2</sup>C™, I<sup>2</sup>C Fast Mode and SMBus Standards (Up to 400kHz Operation)
- Small 8-Pin MSOP and DFN (3mm × 3mm) Packages

## APPLICATIONS


- Hot Board Insertion
- Servers
- Capacitance Buffer/Bus Extender
- Desktop Computers

## DESCRIPTION

The LTC<sup>®</sup>4301L hot swappable, 2-wire bus buffer allows I/O card insertion into a live backplane without corruption of the data and clock busses. In addition, the LTC4301L SDAIN and SCLIN pins are compatible with systems with pull-up voltages as low as 1V. Control circuitry prevents the backplane from being connected to the card until a stop bit or a bus idle is present. When the connection is made, the LTC4301L provides bidirectional buffering, keeping the backplane and card capacitances isolated.

When driven low, the  $\overline{CS}$  input pin allows the part to connect after a stop bit or bus idle occurs. Driving  $\overline{CS}$  high breaks the connection between SCLIN and SCLOUT and between SDAIN and SDAOUT. A logic high on READY indicates that the backplane and card sides are connected together.

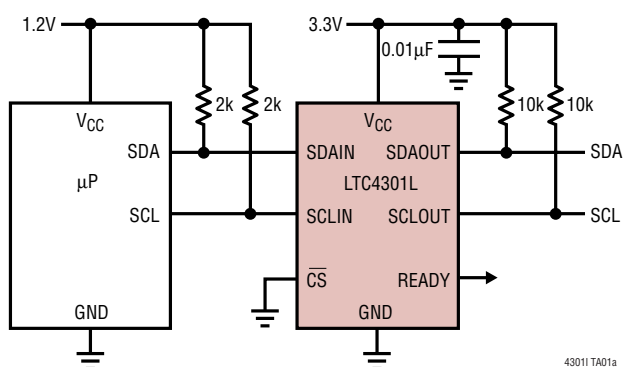
The LTC4301L is offered in 8-pin DFN (3mm × 3mm) and MSOP packages.

 LTC and LT are registered trademarks of Linear Technology Corporation.

I<sup>2</sup>C is a trademark of Philips Electronics N.V.

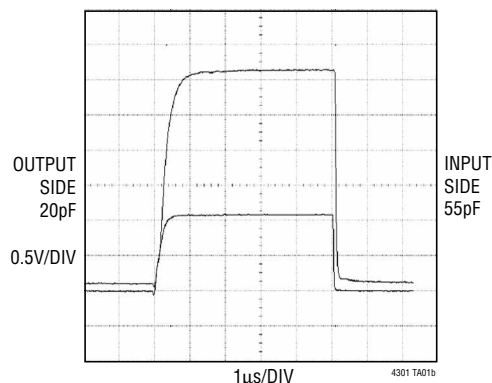
\*Patent Pending

## TYPICAL APPLICATION



43011 TA01a

Input-Output Connection



# LTC4301L

## ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{CC}$ to GND .....	-0.3V to 7V	Storage Temperature Range	
SDAIN, SCLIN, SDAOUT, SCLOUT, CS .....	-0.3V to 7V	MSOP .....	-65°C to 150°C
READY .....	-0.3V to 6V	DFN .....	-65°C to 125°C
Operating Temperature Range		Lead Temperature (Soldering, 10 sec) .....	300°C
LTC4301LC .....	0°C to 70°C		
LTC4301LI .....	-40°C to 85°C		

## PACKAGE/ORDER INFORMATION

<p>DD8 PACKAGE 8-LEAD (3mm x 3mm) PLASTIC DFN <math>T_{JMAX} = 125^{\circ}\text{C}</math>, <math>\theta_{JA} = 43^{\circ}\text{C/W}</math> EXPOSED PAD (PIN 9) IS GND PCB CONNECTION OPTIONAL</p>	ORDER PART NUMBER	<p>MS8 PACKAGE 8-LEAD PLASTIC MSOP <math>T_{JMAX} = 125^{\circ}\text{C}</math>, <math>\theta_{JA} = 200^{\circ}\text{C/W}</math></p>	ORDER PART NUMBER
	LTC4301LCDD8 LTC4301LIDD8		LTC4301LCMS8 LTC4301LIMS8
	DD8 PART MARKING		MS8 PART MARKING
	LBHS		LTBHQ

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ .  $V_{CC} = 2.7\text{V}$  to  $5.5\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Power Supply</b>						
$V_{CC}$	Positive Supply Voltage		● 2.7		5.5	V
$I_{CC}$	Supply Current	$V_{CC} = 5.5\text{V}$ , $V_{SDAIN} = V_{SCLIN} = 0\text{V}$ $V_{CC} = 5.5\text{V}$ , $\overline{CS} = 5.5\text{V}$	●	4.5 300	6.2	mA μA
<b>Start-Up Circuitry</b>						
$V_{PRE}$	Precharge Voltage	SDAOUT, SCLOUT Floating	● 0.85	1.05	1.25	V
$t_{IDLE}$	Bus Idle Time		● 60	95	175	μs
$RDY_{VOL}$	READY Output Low Voltage	$I_{PULLUP} = 3\text{mA}$	●		0.4	V
$V_{THR\overline{CS}}$	Connection Sense Threshold		0.8	1.4	2	V
$I_{\overline{CS}}$	$\overline{CS}$ Input Current	$\overline{CS}$ from 0V to $V_{CC}$		±0.1	±1	μA
$V_{THR}$	SDAIN, SCLIN Logic Input Threshold Voltage	Rising Edge	0.45	0.6	0.75	V
	SDAOUT, SCLOUT Logic Input Threshold Voltage	Rising Edge	1.55	1.8	2.0	V
$V_{HYS}$	SDAIN, SCLIN Logic Input Threshold Hysteresis	(Note 3)		85		mV
	SDAOUT, SCLOUT Logic Input Threshold Hysteresis	(Note 3)		50		mV
$t_{PLH}$	$\overline{CS}$ Delay On-Off			10		ns
	READY Delay Off-On			10		ns
$t_{PHL}$	$\overline{CS}$ Delay Off-On			95		μs
	READY Delay On-Off			10		ns
$I_{OFF}$	Ready Off Leakage Current			±0.1		μA

43011f

## ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 2.7\text{V}$  to  $5.5\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Input-Output Connection</b>							
$V_{OS}$	Input-Output Offset Voltage	10k to $V_{CC}$ on SDA, SCL, $V_{CC} = 3.3\text{V}$ , SDA or SCL = $0.2\text{V}$ (Note 2)	●	0	100	175	mV
$C_{IN}$	Digital Input Capacitance SDA <sub>IN</sub> , SDA <sub>OUT</sub> , SCL <sub>IN</sub> , SCL <sub>OUT</sub>	(Note 3)			10		pF
$I_{LEAK}$	Input Leakage Current	SDA, SCL Pins			±5		μA
$V_{OL}$	Output Low Voltage, Input = 0V	SDA, SCL Pins, $I_{SINK} = 3\text{mA}$ , $V_{CC} = 2.7\text{V}$ SDA, SCL Pins, $I_{SINK} = 1\text{mA}$ , $V_{CC} = 2.7\text{V}$	●	0		0.4	V
				0		0.2	V
<b>Timing Characteristics</b>							
$f_{I2C,MAX}$	I <sup>2</sup> C Maximum Operating Frequency	(Note 3)		400	600		kHz
$t_{BUF}$	Bus Free Time Between Stop and Start Condition	(Note 3)				1.3	μs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition	(Note 3)				100	ns
$t_{SU,STA}$	Repeated Start Condition Set-Up Time	(Note 3)				0	ns
$t_{SU,STO}$	Stop Condition Set-Up Time	(Note 3)				0	ns
$t_{HD,DAT}$	Data Hold Time Input	(Note 3)				0	ns
$t_{SU,DAT}$	Data Set-Up Time	(Note 3)				100	ns

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

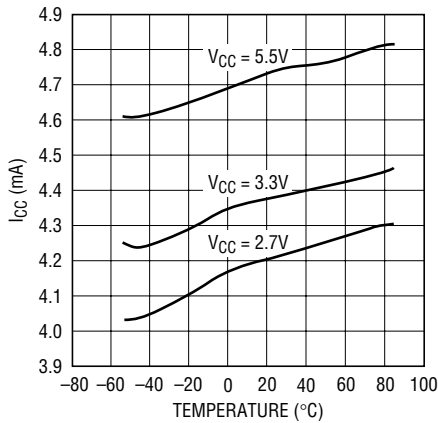
**Note 2:** The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of

the pull-up resistor and  $V_{CC}$  voltage is shown in the Typical Performance Characteristics section.

**Note 3:** Determined by design, not tested in production.

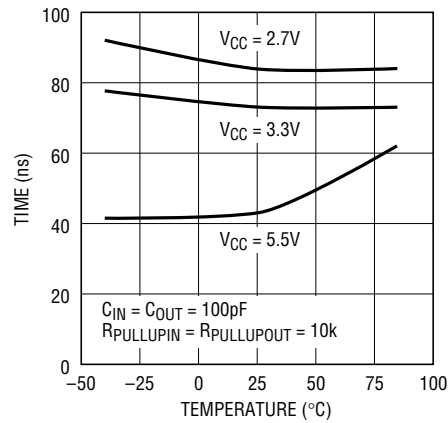
## TYPICAL PERFORMANCE CHARACTERISTICS

$I_{CC}$  vs Temperature



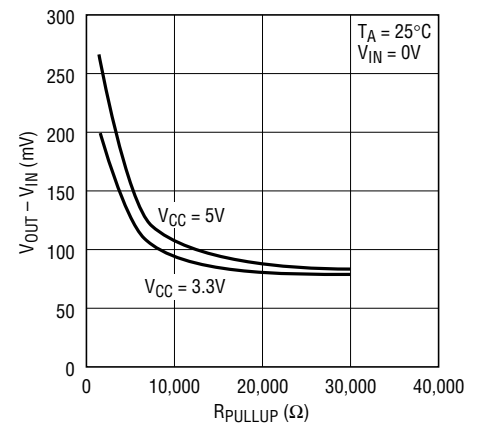
4301 G01

Input – Output High to Low Propagation Delay vs Temperature



4301 G02

Connection Circuitry  $V_{OUT} - V_{IN}$



4301 G03

## PIN FUNCTIONS

**$\overline{CS}$  (Pin 1):** The connection sense pin is a 1.4V threshold digital input pin. For normal operation  $\overline{CS}$  is grounded. Driving  $\overline{CS}$  above the 1.4V threshold isolates SDA<sub>IN</sub> from SDA<sub>OUT</sub> and SCL<sub>IN</sub> from SCL<sub>OUT</sub> and asserts READY low.

**SCL<sub>OUT</sub> (Pin 2):** Serial Clock Output. Connect this pin to the SCL bus on the card.

**SCL<sub>IN</sub> (Pin 3):** Serial Clock Input. Connect this pin to SCL on the bus backplane.

**GND (Pin 4, 9):** Ground. Connect this pin to a ground plane for best results. Exposed pad (DFN package) is ground.

**READY (Pin 5):** The READY pin is an open drain N-channel MOSFET output which pulls down when  $\overline{CS}$  is high or when the start-up sequence described in the Operation section has not been completed. READY goes high when  $\overline{CS}$  is low and a start-up is complete.

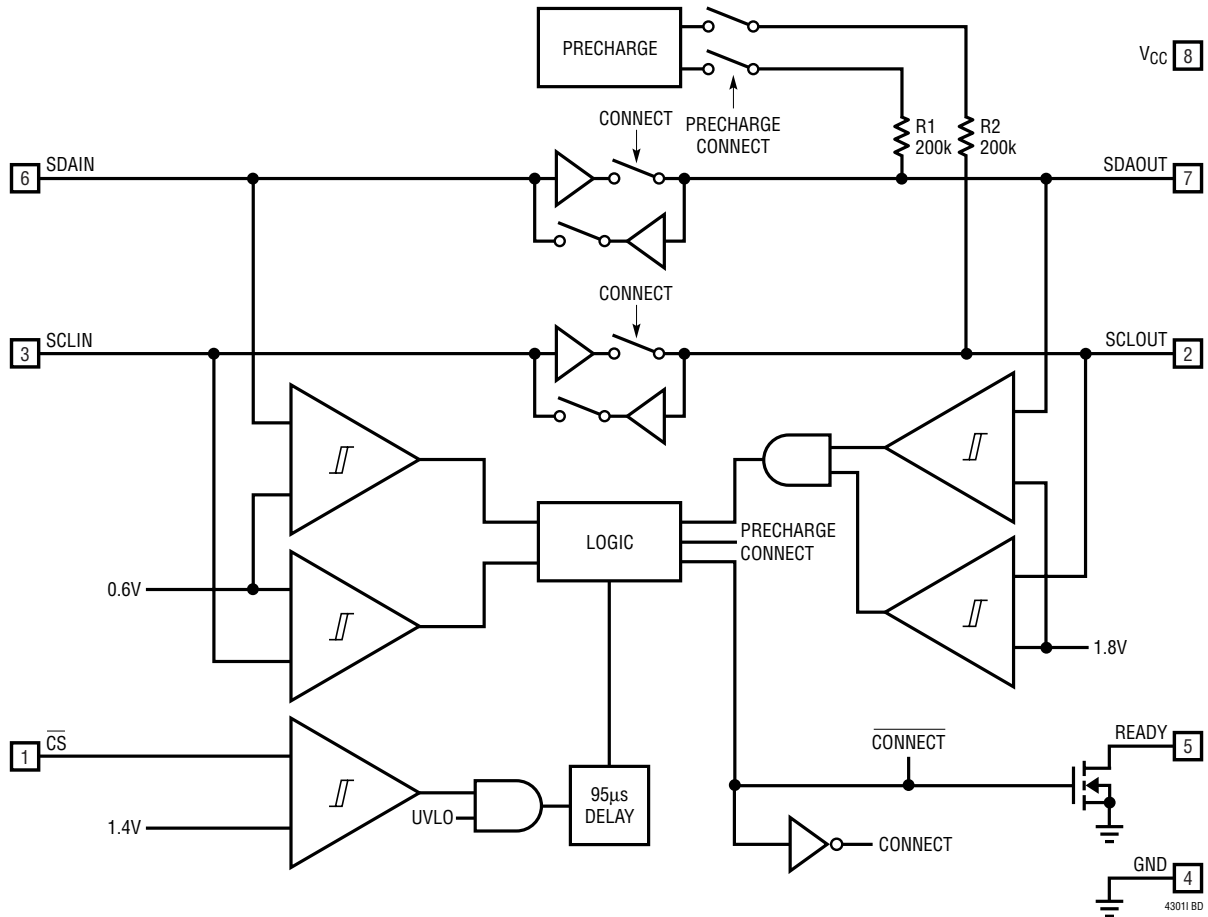
**SDA<sub>IN</sub> (Pin 6):** Serial Data Input. Connect this pin to the SDA bus on the backplane.

**SDA<sub>OUT</sub> (Pin 7):** Serial Data Output. Connect this pin to the SDA bus on the card.

**$V_{CC}$  (Pin 8):** Main Input Supply. Place a bypass capacitor of at least 0.01 $\mu$ F close to  $V_{CC}$  for best results.

# BLOCK DIAGRAM

LTC4301L Supply Independent 2-Wire Bus Buffer



## OPERATION

### Start-Up

When the LTC4301L first receives power on its  $V_{CC}$  pin, either during power-up or live insertion, it starts in an undervoltage lockout (UVLO) state, ignoring any activity on the SDA or SCL pins until  $V_{CC}$  rises above 2.5V. This is to ensure that the part does not try to function until it has enough voltage to do so.

During this time, the 1V precharge circuitry is active and forces 1V through 200k nominal resistors to the SDAOUT and SCLOUT pins. Precharging the SCLOUT and SDAOUT pins to 1V minimizes the worst-case voltage differential these pins will see at the moment of connection, therefore minimizing bus disturbances.

Once the LTC4301L comes out of UVLO, it assumes that SDAIN and SCLIN have been inserted into a live system and that SDAOUT and SCLOUT are being powered up at the same time as itself. Therefore, it looks for either a stop bit or bus idle condition on the backplane side to indicate the completion of a data transaction. When either one occurs, the part also verifies that both the SDAOUT and SCLOUT voltages are high. When all of these conditions are met, the input-to-output connection circuitry is activated, joining the SDA and SCL busses on the I/O card with those on the backplane.

### Connection Circuitry

Once the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A low forced on either pin at any time results in both pin voltages being low. For proper operation, logic low input voltages should be no higher than 0.4V with respect to the ground pin voltage of the LTC4301L. SDAIN and SDAOUT enter a logic high state only when all devices on both SDAIN and SDAOUT release high. The same is true for SCLIN and SCLOUT. This important feature ensures that clock stretching, clock synchronization, arbitration and the acknowledge protocol always work, regardless of how the devices in the system are tied to the LTC4301L.

Another key feature of the connection circuitry is that it provides bidirectional buffering, keeping the backplane and card capacitances isolated. Because of this isolation, the waveforms on the backplane busses look slightly different than the corresponding card bus waveforms as described here.

### Input-to-Output Offset Voltage

When a logic low voltage,  $V_{LOW1}$ , is driven on any of the LTC4301L's data or clock pins, the LTC4301L regulates the voltage on the other side of the device (call it  $V_{LOW2}$ ) at a slightly higher voltage, as directed by the following equation:

$$V_{LOW2} = V_{LOW1} + 75\text{mV} + (V_{CC}/R) \cdot 70\Omega \text{ (typical)}$$

where R is the bus pull-up resistance in ohms. For example, if a device is forcing SDAOUT to 10mV where  $V_{CC} = 3.3\text{V}$  and the pull-up resistor R on SDAIN is 10k, then the voltage on SDAIN =  $10\text{mV} + 75\text{mV} + (3.3/10000) \cdot 70 = 108\text{mV}$  (typical). See the Typical Performance Characteristics section for curves showing the offset voltage as a function of  $V_{CC}$  and R.

### Propagation Delays

During a rising edge, the rise time on each side is determined by the bus pull-up resistor and the equivalent capacitance on the line. In Figure 1,  $V_{CC} = 3.3\text{V}$ , SDAOUT and SCLOUT are pulled-up to 3.3V with 10k resistor (20pF on this side) and SDAIN and SCLIN are pulled-up to 1.2V with a 2k resistor (55pF on this side). Lower pull-up resistor values are used on the input side to allow the output side to be released sooner.

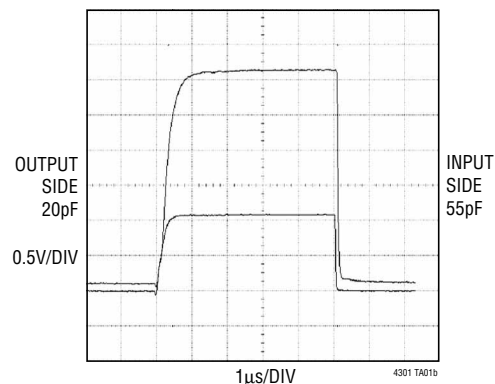


Figure 1. Input-Output Connection

There is a finite high to low propagation delay through the connection circuitry for falling waveforms. Figure 2 shows the falling edge waveforms for the same pull-up resistors and equivalent capacitance conditions as used in Figure 1. An external N-channel MOSFET device pulls down the voltage on the side with 55pF capacitance; LTC4301L pulls down the voltage on the opposite side with a delay of 60ns.

## OPERATION

This delay is always positive and is a function of supply voltage, temperature and the pull-up resistors and equivalent bus capacitances on both sides of the bus. The Typical Performance Characteristics section shows the high to low propagation delay as a function of temperature and voltage for 10k pull-up resistors pulled-up to  $V_{CC}$  and 100pF equivalent capacitance on both sides of the part. Larger output capacitances translate to longer delays (up to 150ns). Users must quantify the difference in propaga-

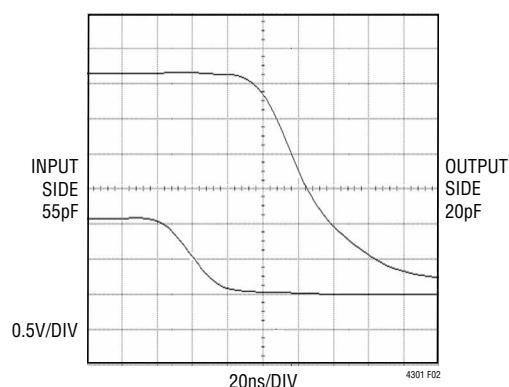


Figure 2. Input-Output Connection High to Low Propagation Delay

tion times for a rising edge versus a falling edge in their systems and adjust setup and hold times accordingly.

### Ready Digital Output

This pin provides a digital flag which is low when either  $\overline{CS}$  is high or the start-up sequence described earlier in this section has not been completed. READY goes high when  $\overline{CS}$  is low and start-up is complete. The pin is driven by an open-drain pull-down capable of sinking 3mA while holding 0.4V on the pin. Connect a resistor of 10k to  $V_{CC}$  to provide the pull-up.

### Connection Sense

When the  $\overline{CS}$  pin is driven above 1.4V with respect to the LTC4301L's ground, the backplane side is disconnected from the card side and the READY pin is internally pulled low. When the pin voltage is low, the part waits for data transactions on both the backplane and card sides to be complete (as described in the Start-Up section) before reconnecting the two sides. At this time the internal pulldown on READY releases.

## APPLICATIONS INFORMATION

### Live Insertion and Capacitance Buffering Application

Figure 3 illustrates applications of the LTC4301L with different bus pull-up and  $V_{CC}$  voltages, demonstrating its ability to recognize and buffer bus data levels that are above or below its  $V_{CC}$  supply. All of these applications take advantage of the LTC4301L's Hot Swap™ controlling, capacitance buffering and precharge features. If the I/O cards were plugged directly into the backplane without the LTC4301L buffer, all of the backplane and card capacitances would add directly together, making rise- and fall-time requirements difficult to meet. Placing an LTC4301L on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the LTC4301L drives the capacitance of everything on the card and the backplane must drive only the capacitance of the LTC4301L, which is less than 10pF.

In most applications the LTC4301L will be used with a staggered connector where  $V_{CC}$  and GND will be long pins. SDA and SCL are medium length pins to ensure that the  $V_{CC}$  and GND pins make contact first. This will allow the precharge circuitry to be activated on SDA and SCL before they make contact.  $\overline{CS}$  is a short pin that is pulled up when not connected. This is to ensure that the connection between the backplane and the cards data and clock busses is not enabled until the transients associated with live insertion have settled.

Figure 4 shows the LTC4301L in an application where all of the pins have the same length. In this case, an RC filter circuit on the I/O card with a product of 10ms provides a filter to prevent the LTC4301L from becoming activated until the transients associated with live insertion have settled. Connect the capacitor between  $V_{CC}$  and  $\overline{CS}$ , and the resistor from  $\overline{CS}$  to GND.

Hot Swap is a trademark of Linear Technology Corporation.

APPLICATIONS INFORMATION

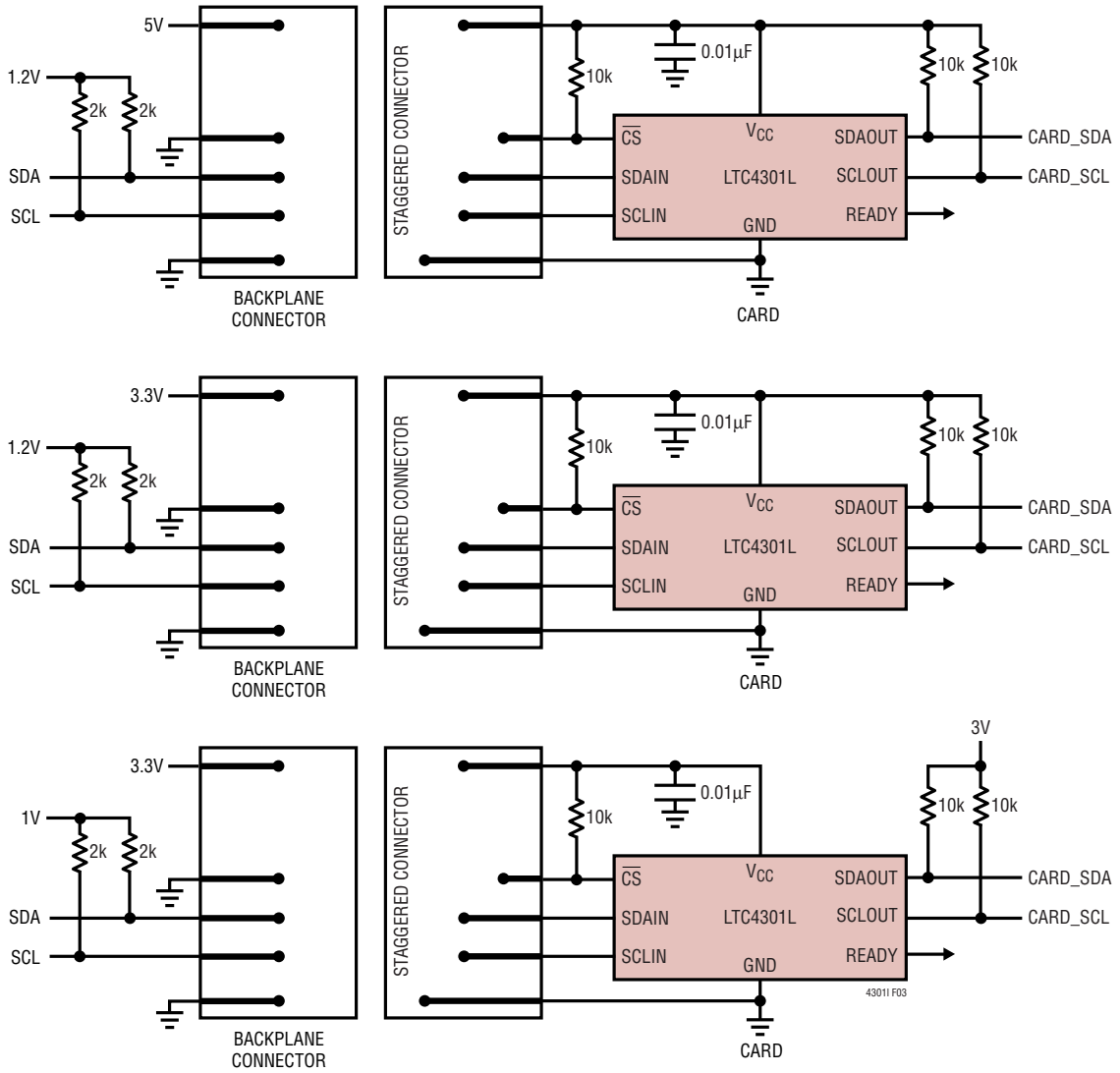


Figure 3. Typical Supply Independent Applications



APPLICATIONS INFORMATION

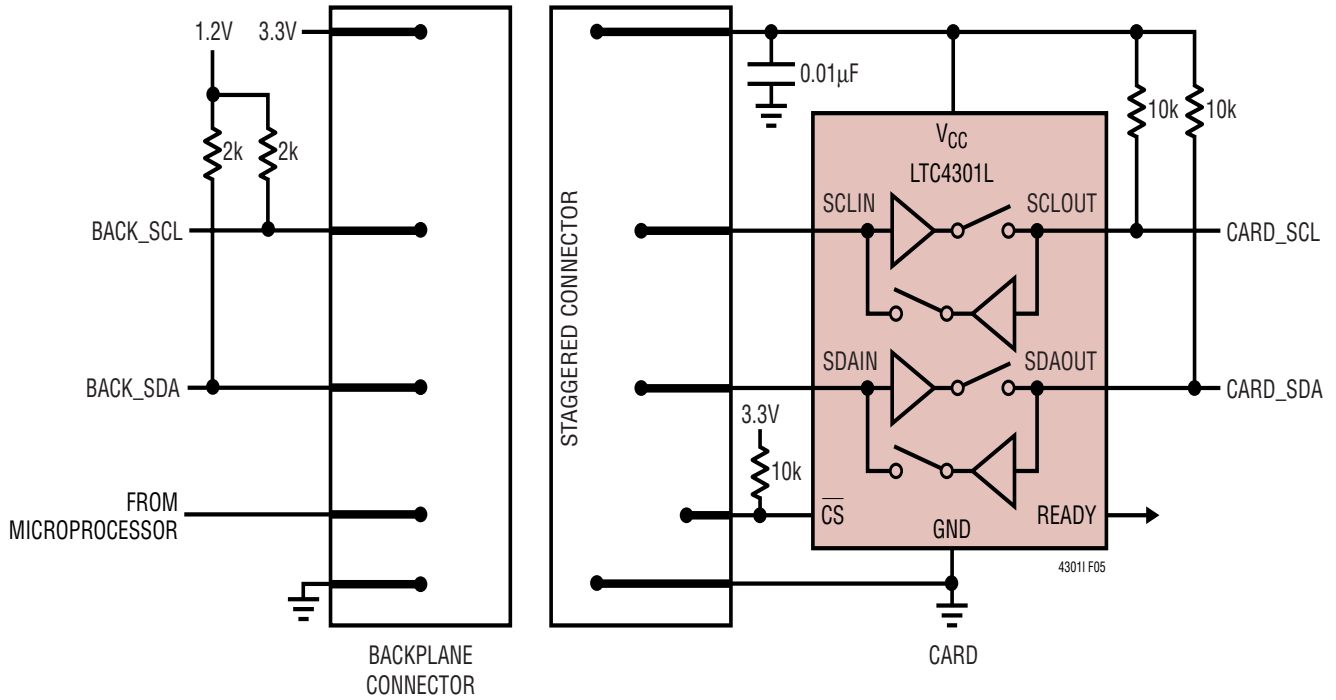
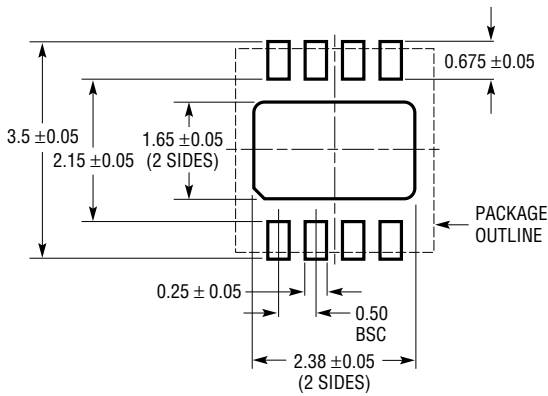


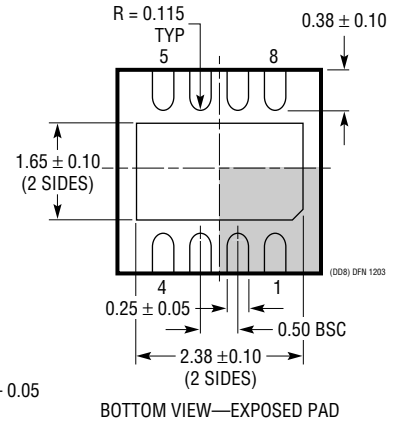
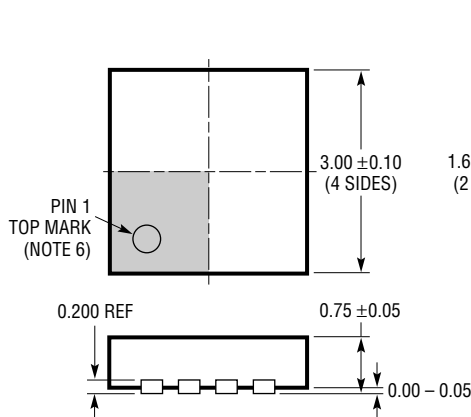
Figure 4. Inserting Multiple I/O Cards into a Live Backplane Using a Connector with All the Pins the Same Length

**PACKAGE DESCRIPTION**

**DD Package**  
**8-Lead Plastic DFN (3mm × 3mm)**  
 (Reference LTC DWG # 05-08-1698)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

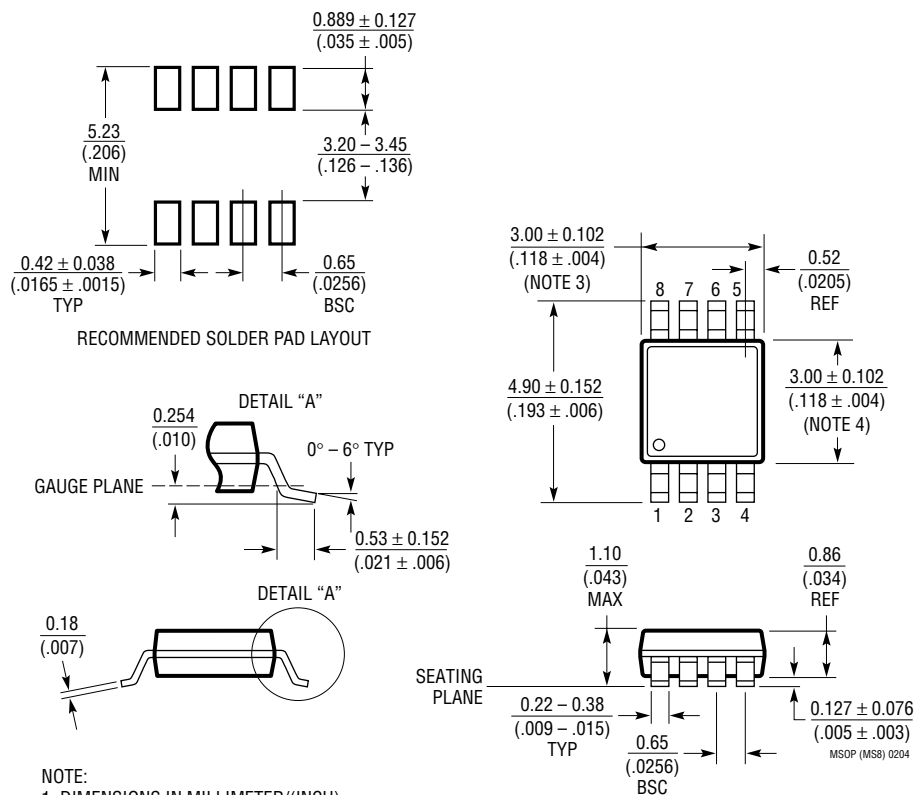


NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

## MS8 Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1660)



## NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)

2. DRAWING NOT TO SCALE

3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE

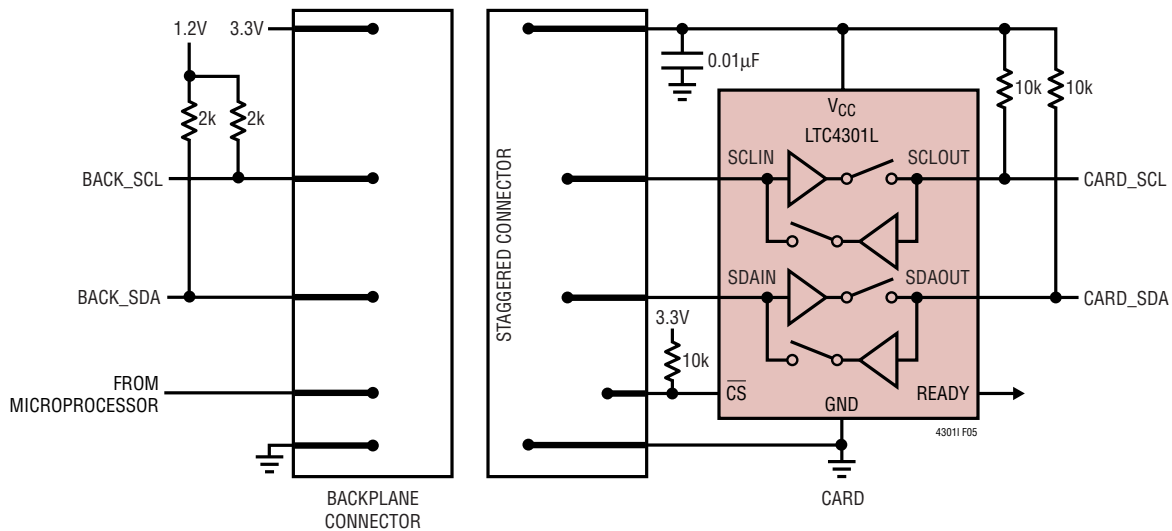
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.

INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE

5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

## TYPICAL APPLICATION

System with Active Connection Control



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1380/LTC1393	Single-Ended 8-Channel/Differential 4-Channel Analog Mux with SMBus Interface	Low $R_{ON}$ : 35 $\Omega$ Single-Ended/70 $\Omega$ Differential, Expandable to 32 Single or 16 Differential Channels
LTC1427-50	Micropower, 10-Bit Current Output DAC with SMBus Interface	Precision 50 $\mu$ A $\pm$ 2.5% Tolerance Over Temperature, 4 Selectable SMBus Addresses, DAC Powers up at Zero or Midscale
LTC1623	Dual High Side Switch Controller with SMBus Interface	8 Selectable Addresses/16-Channel Capability
LTC1663	SMBus Interface 10-Bit Rail-to-Rail Micropower DAC	DNL < 0.75LSB Max, 5-Lead SOT-23 Package
LTC1694/LTC1694-1	SMBus Accelerator	Improved SMBus/I <sup>2</sup> C Rise-Time, Ensures Data Integrity with Multiple SMBus/I <sup>2</sup> C Devices
LT1786F	SMBus Controlled CCFL Switching Regulator	1.25A, 200kHz, Floating or Grounded Lamp Configurations
LTC1695	SMBus/I <sup>2</sup> C Fan Speed Controller in ThinSOT™	0.75 $\Omega$ PMOS 180mA Regulator, 6-Bit DAC
LTC1840	Dual I <sup>2</sup> C Fan Speed Controller	Two 100 $\mu$ A 8-Bit DACs, Two Tach Inputs, Four GPIO
LTC4300A-1/LTC4300A-2	Hot Swappable 2-Wire Bus Buffer	Isolates Backplane and Card Capacitances
LTC4301	Supply Independent Hot Swappable 2-Wire Bus Buffer	Supply Independent
LTC4302-1/LTC4302-2	Addressable 2-Wire Bus Buffer	Address Expansion, GPIO, Software Controlled

ThinSOT is a trademark of Linear Technology Corporation.