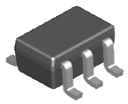
TSZ121

High accuracy (20 µV) zero drift micropower 5 V op amp

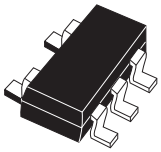
Datasheet — production data

Features

- Very low offset voltage: 20 µV max.
- Ultra low offset voltage drift: 60 nV/°C max.
- Rail-to-rail input and output
- Low supply voltage: 1.8 - 5.5 V
- Low power consumption: 42 µA max. at 5 V
- Gain bandwidth product: 400 kHz
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 to +125 °C
- Micro-packages: SC70-5 and SOT23-5



SC70-5



SOT23-5

Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Medical instrumentation

Description

The TSZ121 device is the first member of the TSZ12x series of high precision operational amplifiers featuring very low offset voltage with virtually zero drift.

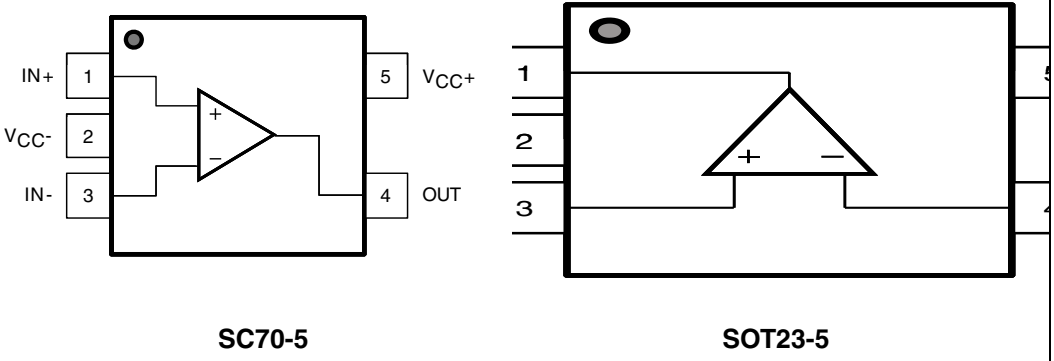
The TSZ12x series offers rail-to-rail input and output, excellent speed/power consumption ratio, and 400 kHz gain bandwidth product, while consuming less than 42 µA at 5 V. The devices also feature an ultra-low input bias current.

These features make the TSZ12x family ideal for sensor interfaces, battery-powered applications and portable applications.

Contents

1 Package pin connections

Figure 1. Pin connections for each package (top view)



SC70-5 SOT23-5

2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage(1)	6	V
V_{id}	Differential input voltage(2)	$\pm V_{cc}$	V
V_{in}	Input voltage(3)	V_{cc-} - 0.2 to V_{cc+}+ 0.2	V
I_{in}	Input current(4)	10	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction-to-ambient(5), (6)		°C/W
	SC70-5	205	
	SOT23-5	250	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model(7)	4	kV
	MM: machine model(8)	300	V
	CDM: charged device model(9)	1.5	kV
	Latch-up immunity	200	mA

1. All voltage values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. V_{cc} - V_{in} must not exceed 6 V, V_{in} must not exceed 6 V.
4. Input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. R_{th} are typical values.
7. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage	1.8 to 5.5	V
V_{icm}	Common mode input voltage range	V_{cc-} - 0.1 to V_{cc+} + 0.1	V
T_{oper}	Operating free air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 3. Electrical characteristics at V_{CC+} = 1.8 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T = 25 °C, and R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		1	20	µV
		-40 °C < T< 125 °C			28	
$\Delta V_{io}/\Delta T$	Input offset voltage drift(1)	-40 °C < T< 125 °C		0.01	0.08	µV/°C
I_{io}	Input offset current (V_{out} = V_{CC}/2)	T = 25 °C		100	400(2)	pA
		-40 °C < T< 125 °C			600(2)	
I_{ib}	Input bias current (V_{out} = V_{CC}/2)	T = 25 °C		50	200(2)	pA
		-40 °C < T< 125 °C			300(2)	
CMR	Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$) V_{ic} = 0 V to V_{CC}, V_{out} = V_{CC}/2, R_L > 1 MΩ	T = 25 °C	100	112		dB
		-40 °C < T< 125 °C	100			
A_{vd}	Large signal voltage gain V_{out} = 0.5 V to (V_{cc} - 0.5 V)	T = 25 °C		135		dB
		-40 °C < T< 125 °C	110			
V_{OH}	High level output voltage	T = 25 °C			30	mV
		-40 °C < T< 125 °C			70	
V_{OL}	Low level output voltage	T = 25 °C			30	mV
		-40 °C < T< 125 °C			70	
I_{out}	I_{sink} (V_{out} = V_{CC})	T = 25 °C	7	8		mA
		-40 °C < T< 125 °C	6			
	I_{source} (V_{out} = 0 V)	T = 25 °C	5	7		mA
		-40 °C < T< 125 °C	4			
I_{CC}	Supply current (per operator, V_{out} = V_{CC}/2, R_L > 1 MΩ)	T = 25 °C		28	42	µA
		-40 °C < T< 125 °C			45	

Table 3. Electrical characteristics at V_{CC+} = 1.8 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T = 25 °C, and R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		400		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		300		kHz
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		55		degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		17		dB
t_s	Settling time	To 0.1%, V_{in} = 1 Vp-p, R_L = 10 kΩ, C_L = 100 pF		50		µs
SR	Slew rate(3)	R_L = 10 kΩ, C_L = 100 pF		0.17		V/µs
e_n	Equivalent input noise voltage	f = 1 kHz f = 10 kHz		50 50		$\frac{nV}{\sqrt{Hz}}$
t_{init}	Initialization time	T = 25 °C		50		µs
		-40 °C < T< 125 °C		100		

1. See *Section 4.5: Input offset voltage drift over temperature on page 20*. Input offset voltage performance is enhanced by appropriate supply voltage decoupling, see *Section 4.7: PCB layout recommendations on page 20*.
2. Guaranteed by design.
3. Slew rate value is calculated as the average between positive and negative slew rates.

Table 4. Electrical characteristics at V_{CC+} = 3.3 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T = 25 °C, and R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		1	20	µV
		-40 °C < T< 125 °C			26	
$\Delta V_{io}/\Delta T$	Input offset voltage drift(1)	-40 °C < T< 125 °C		0.01	0.06	µV/°C
I_{io}	Input offset current (V_{out} = V_{CC}/2)	T = 25 °C		120	400(2)	pA
		-40 °C < T< 125 °C			600(2)	
I_{ib}	Input bias current (V_{out} = V_{CC}/2)	T = 25 °C		60	200(2)	pA
		-40 °C < T< 125 °C			300(2)	
CMR	Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$) V_{ic} = 0 V to V_{CC}, V_{out} = V_{CC}/2 R_L > 1 MΩ	T = 25 °C	106	118		dB
		-40 °C < T< 125 °C	106			
A_{vd}	Large signal voltage gain V_{out} = 0.5 V to (V_{cc} - 0.5 V)	T = 25 °C	118	135		dB
		-40 °C < T< 125 °C	110			
V_{OH}	High level output voltage	T = 25 °C			30	mV
		-40 °C < T< 125 °C			70	
V_{OL}	Low level output voltage	T = 25 °C			30	mV
		-40 °C < T< 125 °C			70	
I_{out}	I_{sink} (V_{out} = V_{CC})	T = 25 °C	15	18		mA
		-40 °C < T< 125 °C	12			
	I_{source} (V_{out} = 0 V)	T = 25 °C	14	16		mA
		-40 °C < T< 125 °C	10			
I_{CC}	Supply current (per operator, V_{out} = V_{CC}/2, R_L > 1 MΩ)	T = 25 °C		29	42	µA
		-40 °C < T< 125 °C			45	

Table 4. Electrical characteristics at V_{CC+} = 3.3 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T = 25 °C, and R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		400		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		300		kHz
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		56		degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		19		dB
t_s	Settling time	To 0.1%, V_{in} = 1 Vp-p, R_L = 10 kΩ, C_L = 100 pF		50		µs
SR	Slew rate(3)	R_L = 10 kΩ, C_L = 100 pF		0.19		V/µs
e_n	Equivalent input noise voltage	f = 1 kHz f = 10 kHz		50 50		$\frac{nV}{\sqrt{Hz}}$
t_{init}	Initialization time	T = 25 °C		50		µs
		-40 °C < T< 125 °C		100		

1. See *Section 4.5: Input offset voltage drift over temperature on page 20*. Input offset voltage performance is enhanced by appropriate supply voltage decoupling, see *Section 4.7: PCB layout recommendations on page 20*.
2. Guaranteed by design.
3. Slew rate value is calculated as the average between positive and negative slew rates.

Table 5. Electrical characteristics at V_{CC+} = 5 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T = 25 °C, and R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		1	20	µV
		-40 °C < T< 125 °C			26	
$\Delta V_{io}/\Delta T$	Input offset voltage drift(1)	-40 °C < T< 125 °C		0.01	0.06	µV/°C
I_{io}	Input offset current (V_{out} = V_{CC}/2)	T = 25 °C		140	400(2)	pA
		-40 °C < T< 125 °C			600(2)	
I_{ib}	Input bias current (V_{out} = V_{CC}/2)	T = 25 °C		70	200(2)	pA
		-40 °C < T< 125 °C			300(2)	
CMR	Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$) V_{ic} = 0 V to $V_{CC/}$, V_{out} = $V_{CC/}$/2 R_L > 1 MΩ	T = 25 °C	110	126		dB
		-40 °C < T< 125 °C	110			
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC/}/\Delta V_{io}$) $V_{CC/}$ = 1.8 to 5.5 V, V_{out} = $V_{CC/}$/2, R_L > 1 MΩ	T = 25 °C	106	115		dB
		-40 °C < T< 125 °C	106			
A_{vd}	Large signal voltage gain V_{out} = 0.5 V to (V_{cc} - 0.5 V)	T = 25 °C	120	135		dB
		-40 °C < T< 125 °C	110			
V_{OH}	High level output voltage	T = 25 °C			30	mV
		-40 °C < T< 125 °C			70	
V_{OL}	Low level output voltage	T = 25 °C			30	mV
		-40 °C < T< 125 °C			70	
I_{out}	I_{sink} (V_{out} = $V_{CC/}$)	T = 25 °C	15	18		mA
		-40 °C < T< 125 °C	14			
	I_{source} (V_{out} = 0 V)	T = 25 °C	14	17		mA
		-40 °C < T< 125 °C	12			
I_{CC}	Supply current (per operator, V_{out} = $V_{CC/}$/2, R_L > 1 MΩ)	T = 25 °C		31	42	µA
		-40 °C < T< 125 °C			45	

Table 5. Electrical characteristics at V_{CC+} = 5 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T = 25 °C, and R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		400		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		300		kHz
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		53		degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		19		dB
t_s	Settling time	To 0.1%, V_{in} = 1 Vp-p, R_L = 10 kΩ, C_L = 100 pF		50		µs
SR	Slew rate(3)	R_L = 10 kΩ, C_L = 100 pF		0.19		V/µs
e_n	Equivalent input noise voltage	f = 1 kHz f = 10 kHz		50 50		$\frac{nV}{\sqrt{Hz}}$
t_{init}	Initialization time	T = 25 °C		50		µs
		-40 °C < T< 125 °C		100		

1. See *Section 4.5: Input offset voltage drift over temperature on page 20*. Input offset voltage performance is enhanced by appropriate supply voltage decoupling, see *Section 4.7: PCB layout recommendations on page 20*.
2. Guaranteed by design.
3. Slew rate value is calculated as the average between positive and negative slew rates.

Figure 2. Supply current vs. supply voltage at $V_{icm} = V_{cc}/2$

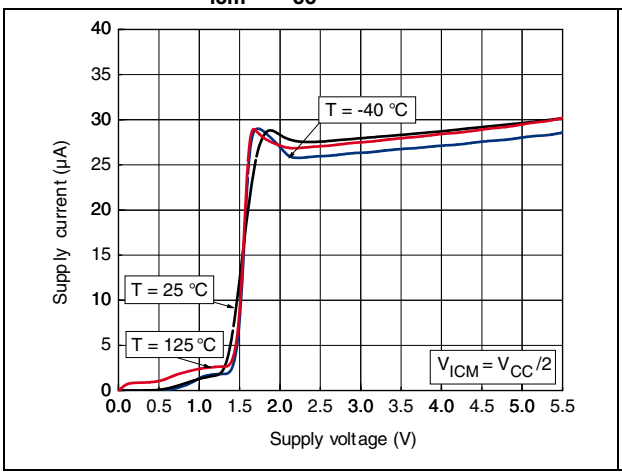


Figure 3. Input offset voltage distribution at $V_{CC} = 5$ V, $V_{icm} = V_{cc}/2$

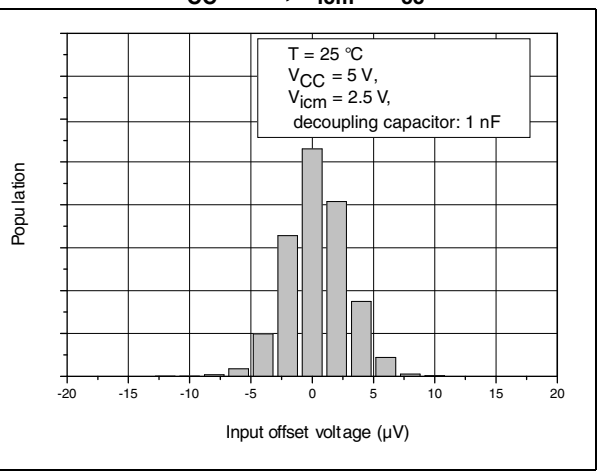


Figure 4. V_{io} temperature coefficient distribution (absolute value)

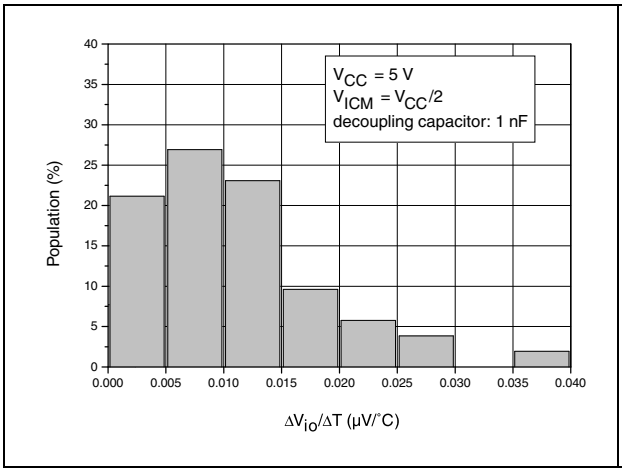


Figure 5. Input offset voltage vs. supply voltage at $V_{icm} = V_{CC}/2$

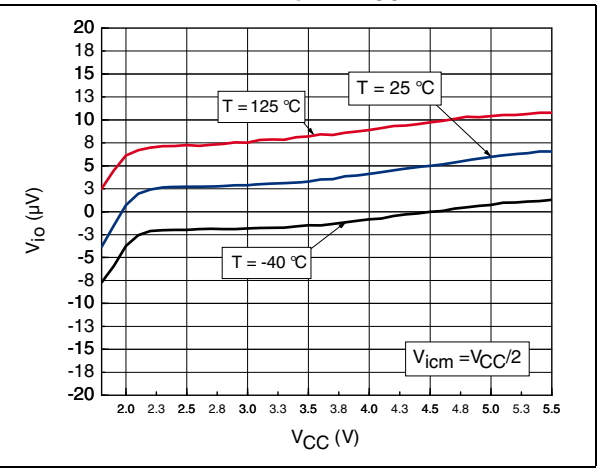


Figure 6. Input offset voltage vs. input common-mode at V_{CC}= 1.8 V

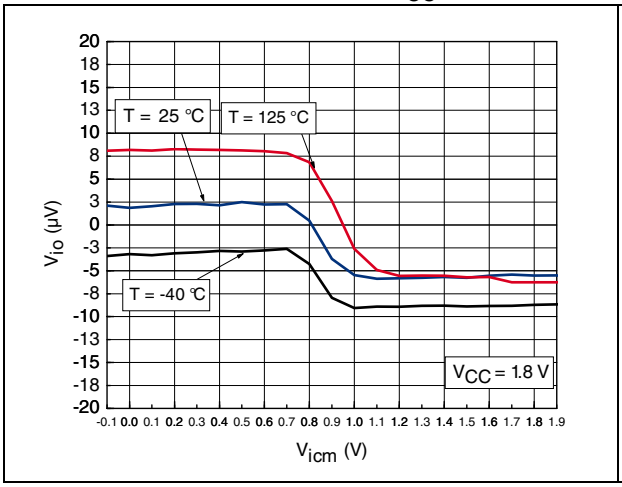


Figure 7. Input offset voltage vs. input common-mode at $V_{CC} = 2.7$ V

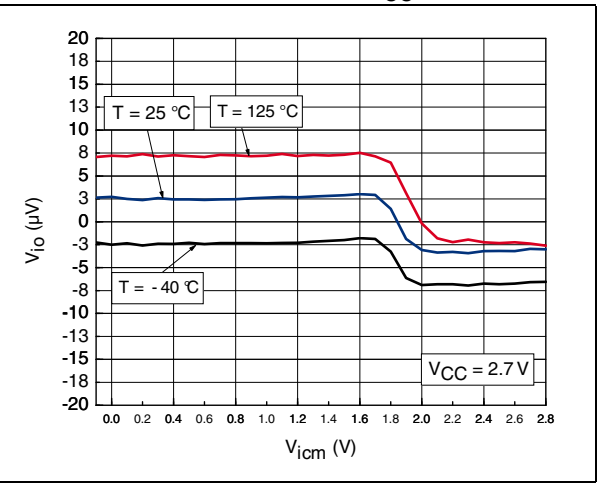


Figure 8. Input offset voltage vs. input common-mode at V_{CC}= 5.5 V

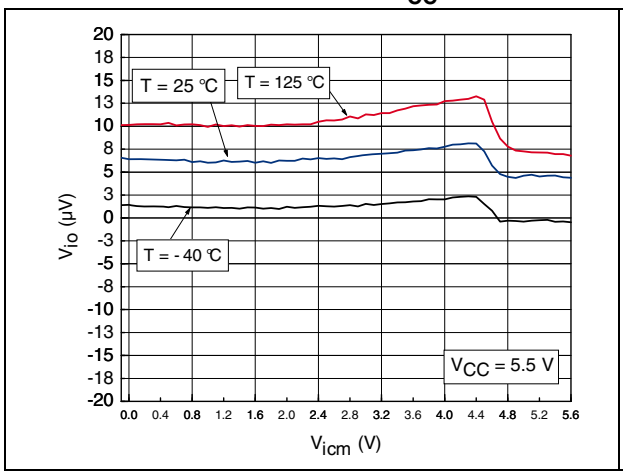


Figure 9. Input offset voltage vs. temperature

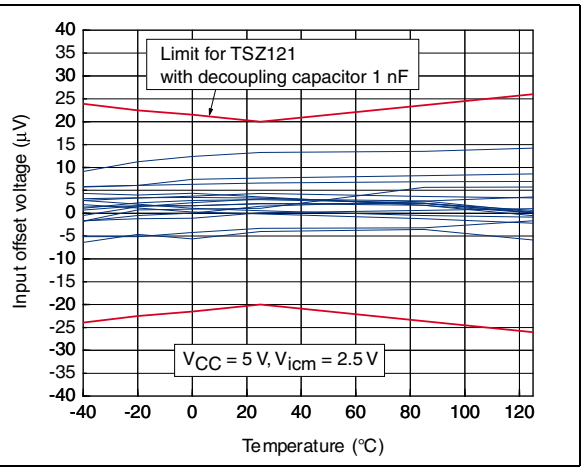


Figure 10. Output current vs. output voltage at V_{CC} = 1.8 V

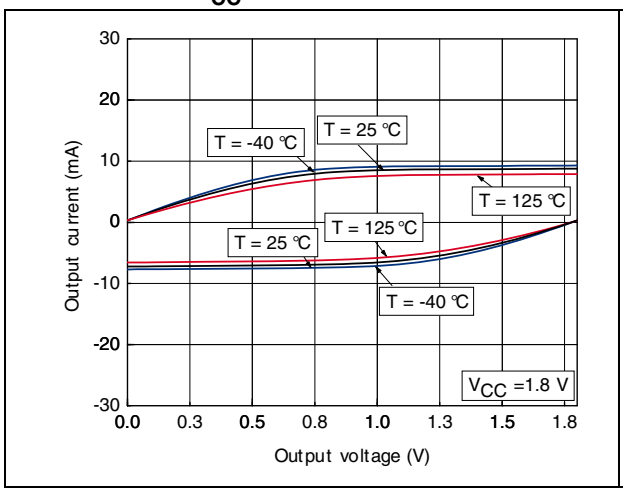


Figure 11. Output current vs. output voltage at V_{CC} = 5 V

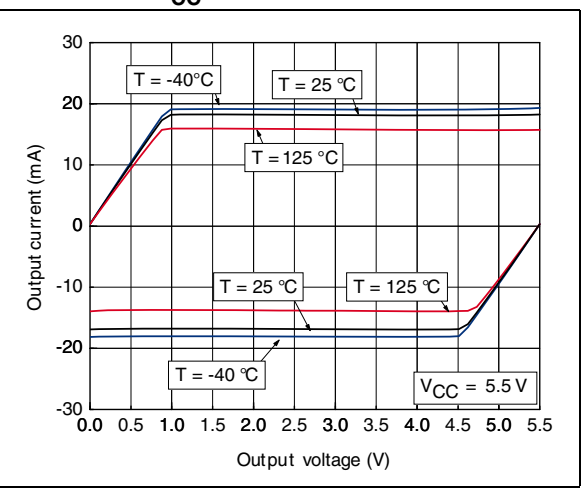


Figure 12. Input bias current vs. common mode at V_{CC} = 1.8 V

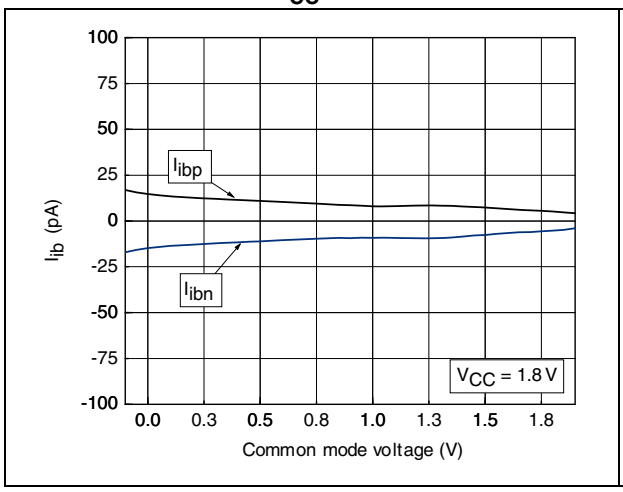


Figure 13. Input bias current vs. common mode at V_{CC} = 5 V

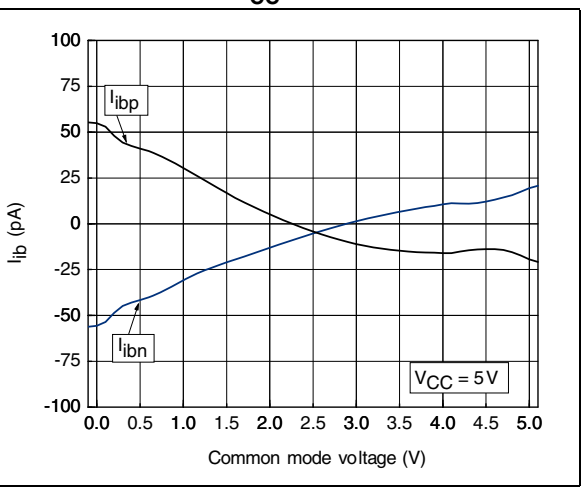


Figure 14. Output current vs. output voltage at V_{CC} = 1.8 V

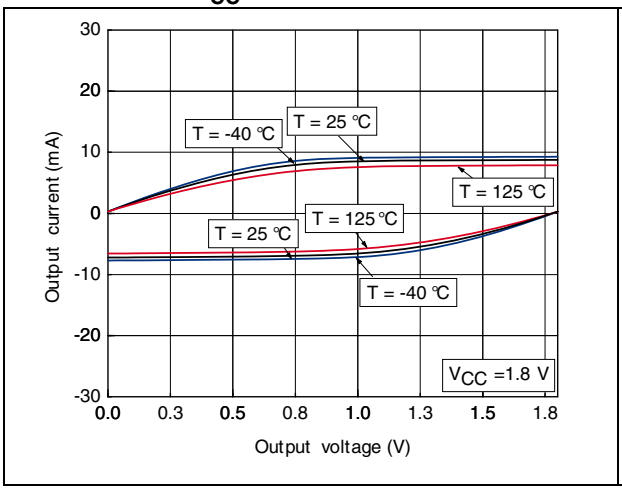


Figure 15. Output current vs. output voltage at V_{CC} = 5 V

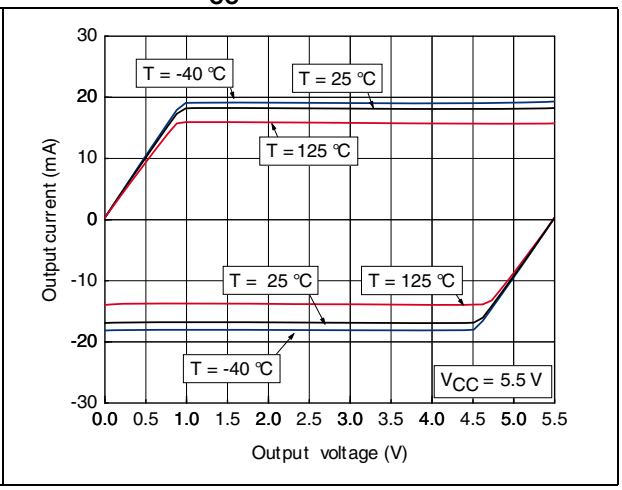


Figure 16. Bode diagram at V_{CC} = 1.8 V, R_L = 10 kΩ

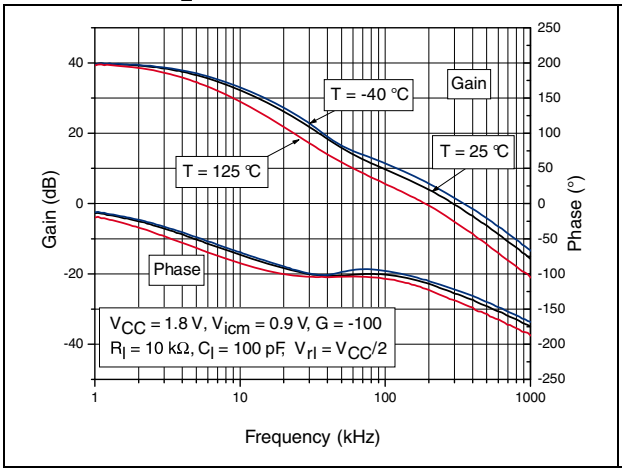


Figure 17. Bode diagram at V_{CC} = 2.7 V, R_L = 10 kΩ

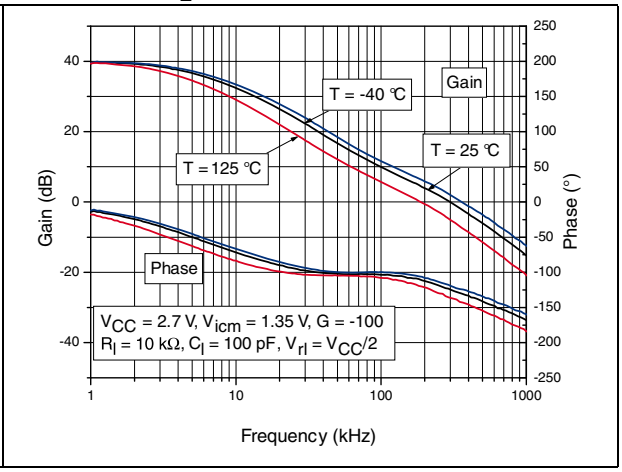


Figure 18. Bode diagram at V_{CC} = 5.5 V, R_L = 10 kΩ

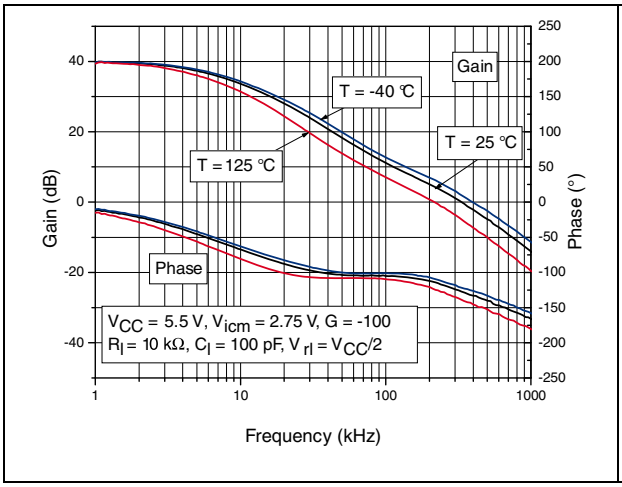


Figure 19. Open loop gain vs. frequency

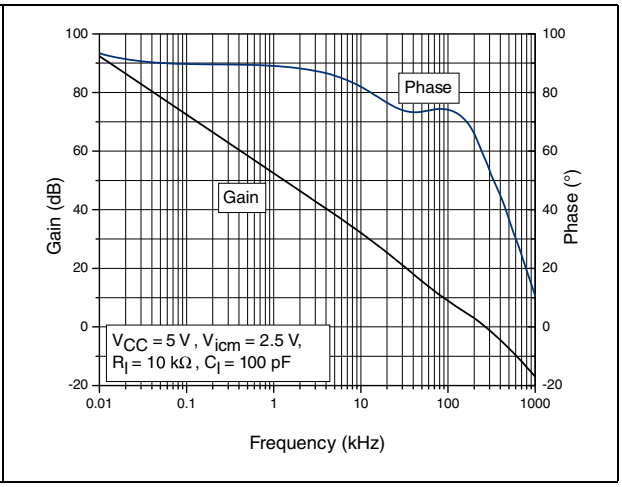


Figure 20. Output overshoot vs. load capacitance

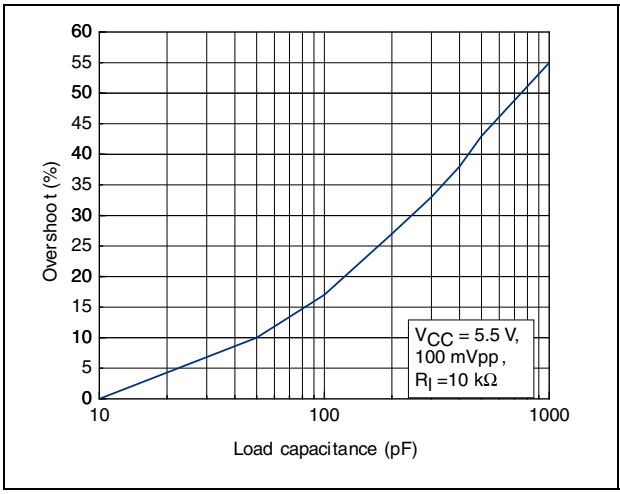


Figure 21. Output impedance vs. frequency

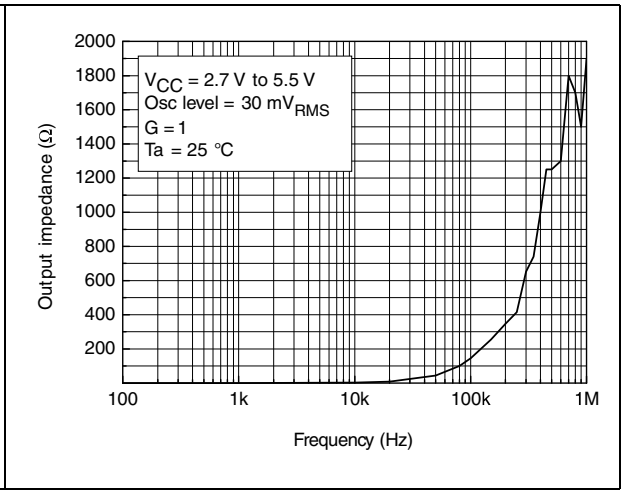


Figure 22. 0.1 Hz to 10 Hz noise

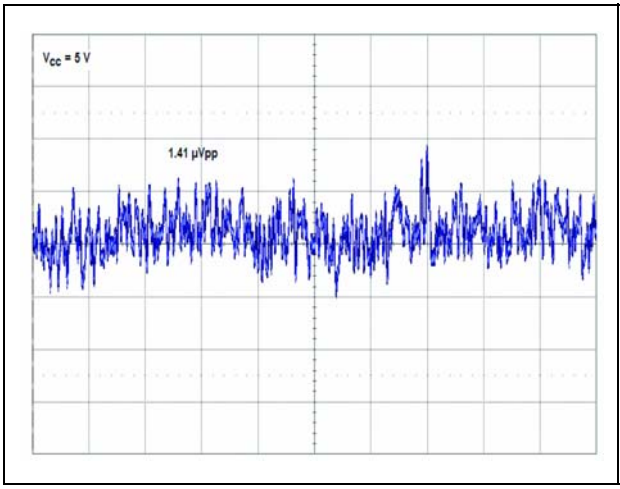


Figure 23. Noise vs. frequency

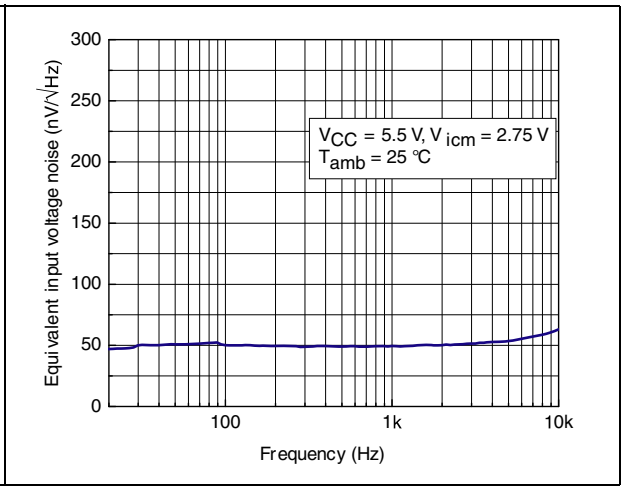


Figure 24. Small signal

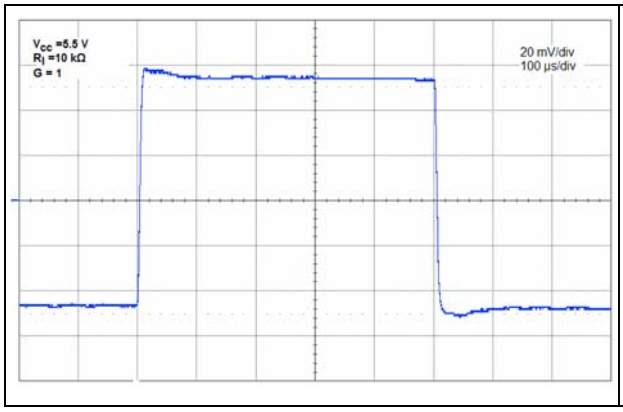


Figure 25. Large signal

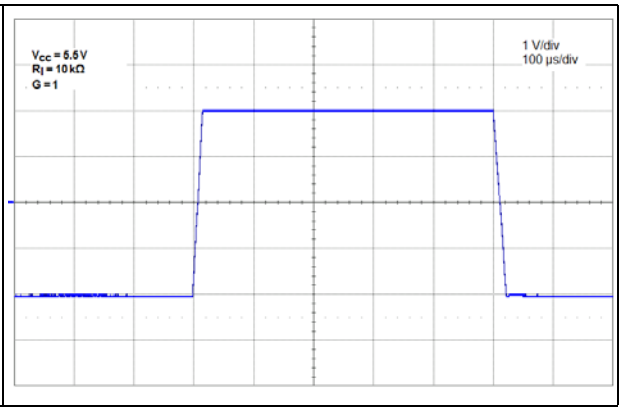


Figure 26. Positive overvoltage recovery at V_{CC} = 1.8 V

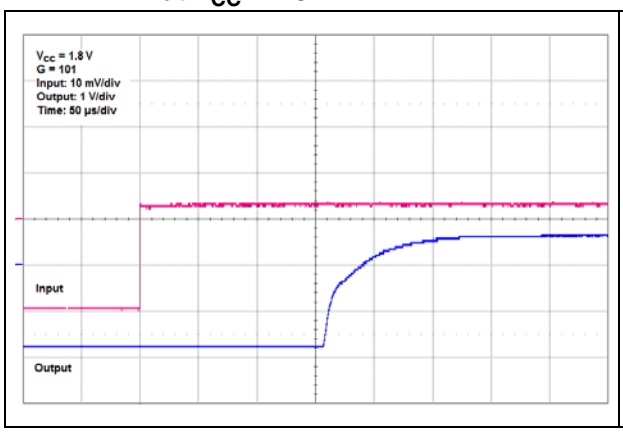


Figure 27. Positive overvoltage recovery at V_{CC} = 5 V

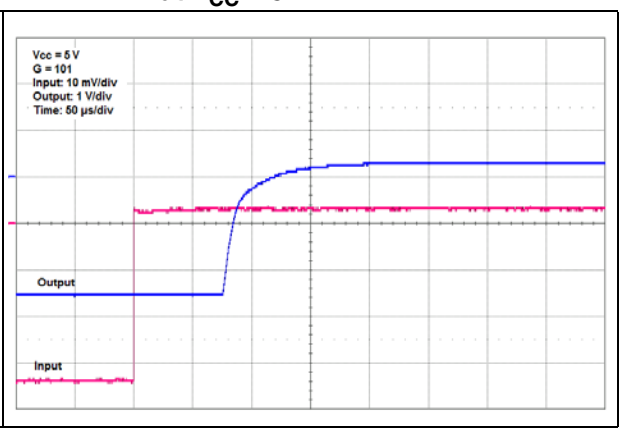


Figure 28. Negative overvoltage recovery at V_{CC} = 1.8 V

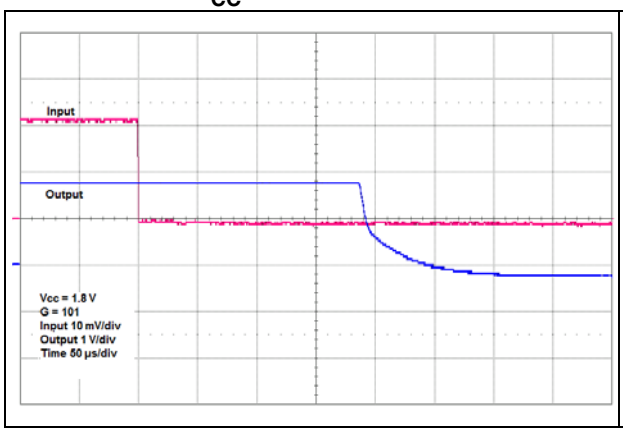


Figure 29. Negative overvoltage recovery at V_{CC} = 5 V

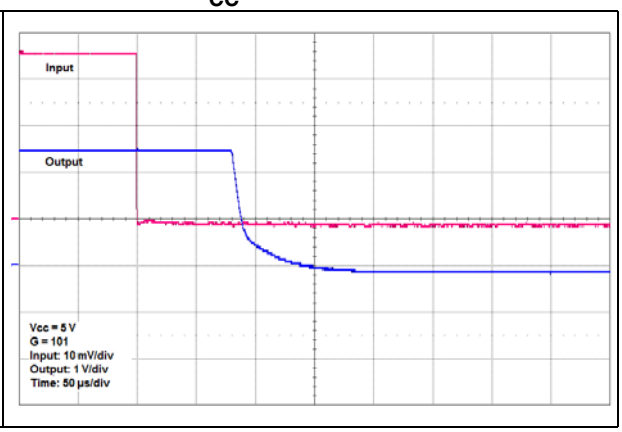


Figure 30. V_{OH} vs. supply voltage

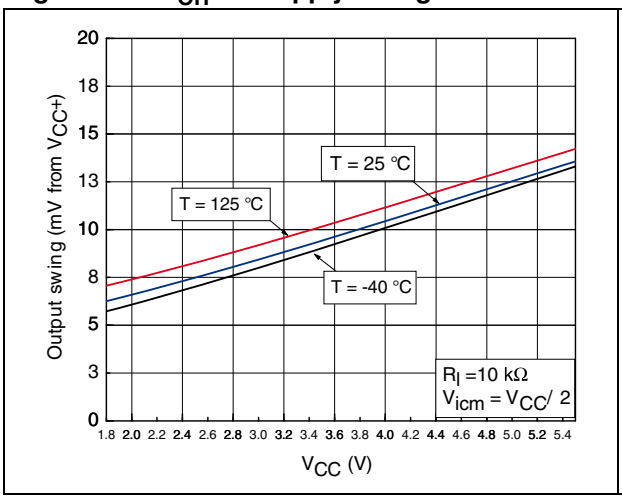


Figure 31. V_{OL} vs. supply voltage

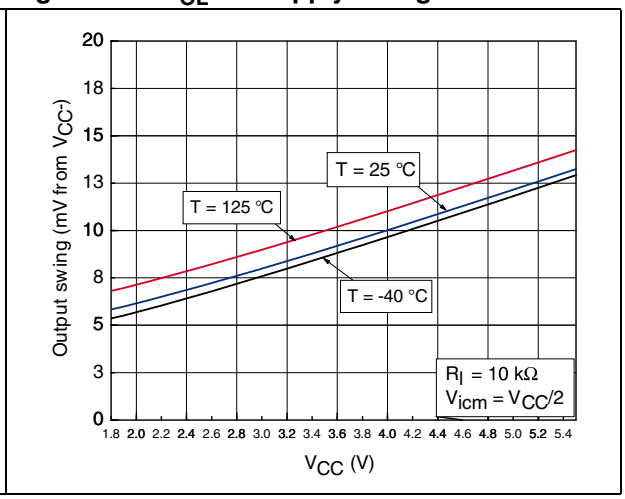


Figure 32. PSRR vs. frequency

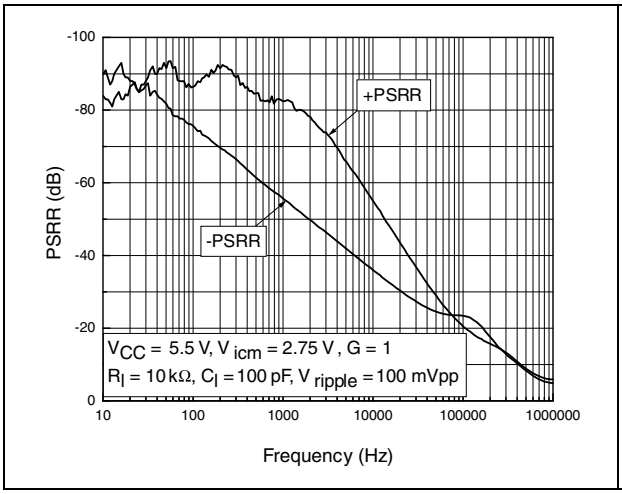


Figure 33. Input bias currents vs. temperature

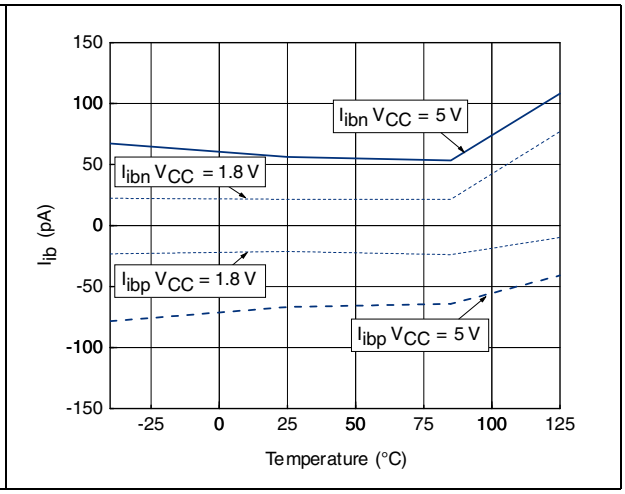


Figure 34. Positive slew rate vs. supply voltage

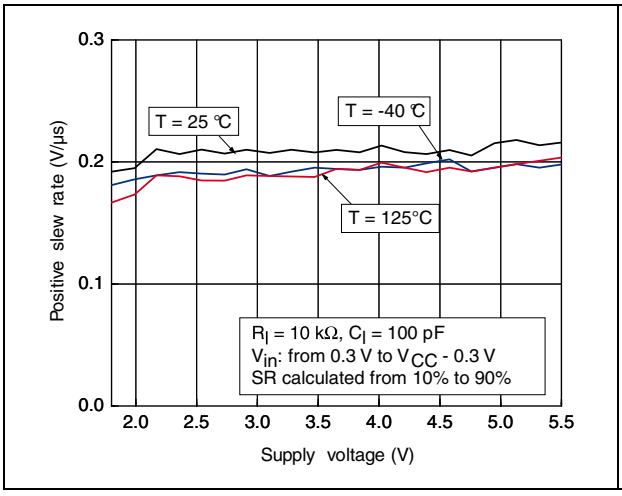
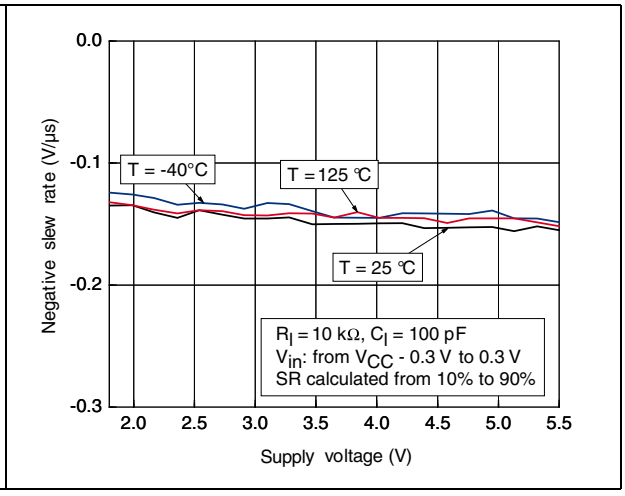


Figure 35. Negative slew rate vs. supply voltage



4 Application information

4.1 Theory of operation

The TSZ121 device is a high precision CMOS achieving a low offset drift and no 1/f noise, thanks to chopper architecture. Chopper-stabilized amps constantly correct low-frequency errors across the inputs of the amplifier.

How a chopper-stabilized amplifier works

There are two approaches to understanding the basic chopper technique; the time domain and the frequency domain.

4.1.1 Time domain

The basis of the chopper amplifier is realized in two steps. These steps are synchronized thanks to a clock running at 400 kHz.

Figure 36. Block diagram in the time domain (step 1)

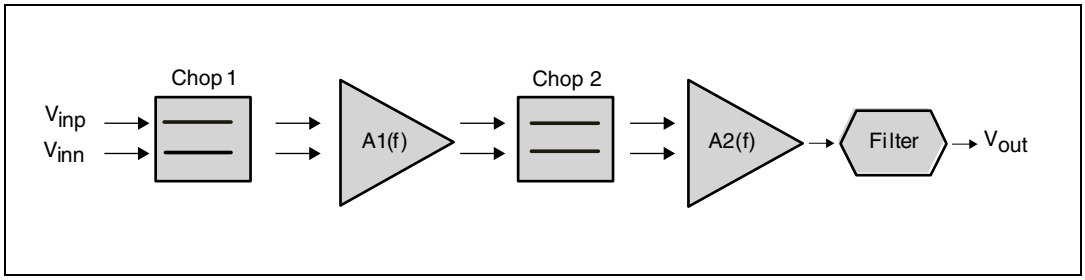
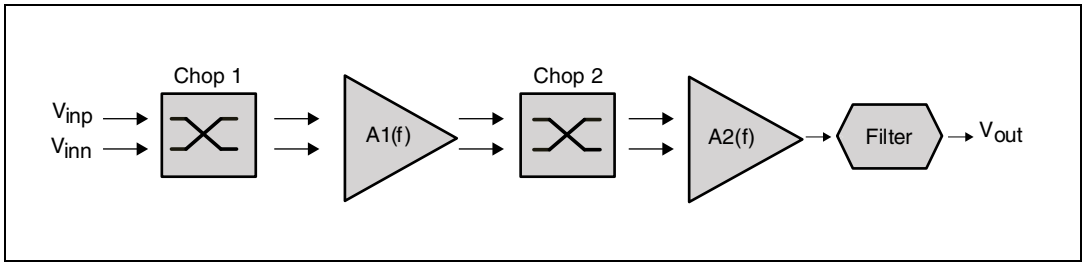


Figure 37. Block diagram in the time domain (step 2)



First, the V_{io} is amplified in a normal way during step 1 described in *Figure 36*.

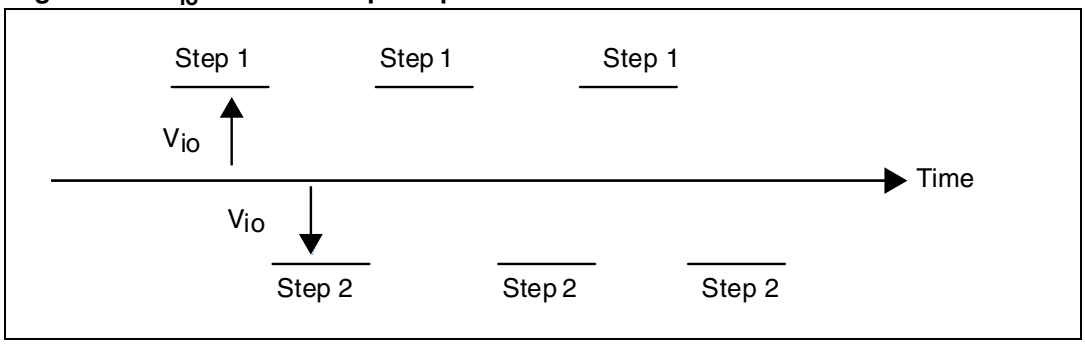
Next, on the second clock cycle, Chop1 and Chop2 inverse the path as described by step 2 in *Figure 37*. So at this time the V_{io} is amplified in a reverse way as compared to step 1.

At the end of these two steps, the average V_{io} is close to zero.

The A2(f) amplifier has a small impact on the V_{io}, as the V_{io} is expressed as the input offset, so divided by A1(f).

In the time domain the offset part of the output signal before filtering is represented by *Figure 38*.

Figure 38. V_{io} cancellation principle



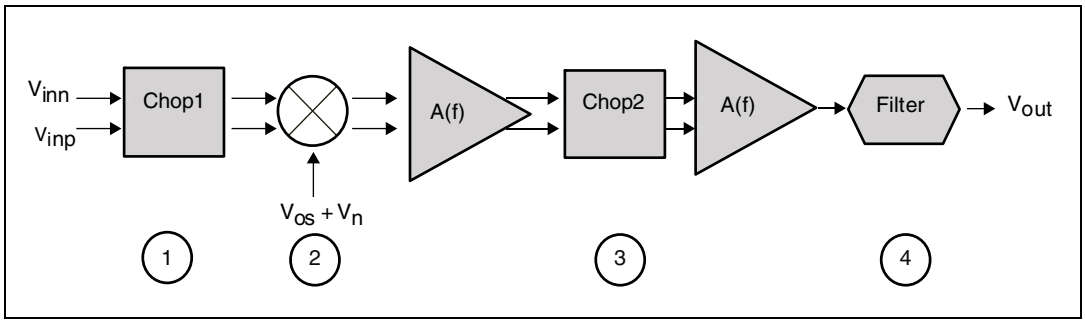
Then, the low pass filter averages the output value resulting in a null V_{io} offset.

The 1/f noise can be considered as an offset in low frequency and it is nulled like the V_{io}, thanks to the chopper technique.

4.1.2 Frequency domain

The chopper basic techniques can also be explained in the frequency domain, which gives a more accurate vision of the architecture.

Figure 39. Block diagram in the frequency domain



The modulation technique is to transpose the signal to a higher frequency where there is no 1/f noise, and then demodulate it back after amplification.

1. According to *Figure 39*, V_{in} is modulated one time (Chop1) so all the input signal is transposed in high frequency domain.
2. The amplifier adds its own error (V_{io} (output offset voltage) + the noise V_n (1/f noise)) to this modulated signal.
3. This signal is then demodulated (Chop2), but since the noise and the offset are modulated only once, they are transposed to the high frequency, leaving the output signal of the amplifier without any offset and low frequency noise.
   So the input signal is amplified with a very low offset and 1/f noise.
4. To get rid of the high frequency part of the output signal (which is useless) a low pass filter is implemented.

To further suppress the remaining ripple down to a desired level, another low pass filter may be added externally on the output of the TSZ121 device.

4.2 Operating voltages

The TSZ12x device can operate from 1.8 to 5.5 V. The parameters are fully specified for 1.8, 3.3 and 5 V power supplies. However, the parameters are very stable in the full V_{CC} range and several characterization curves show the TSZ12x device characteristics at 1.8 V. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 to +125 ° C.

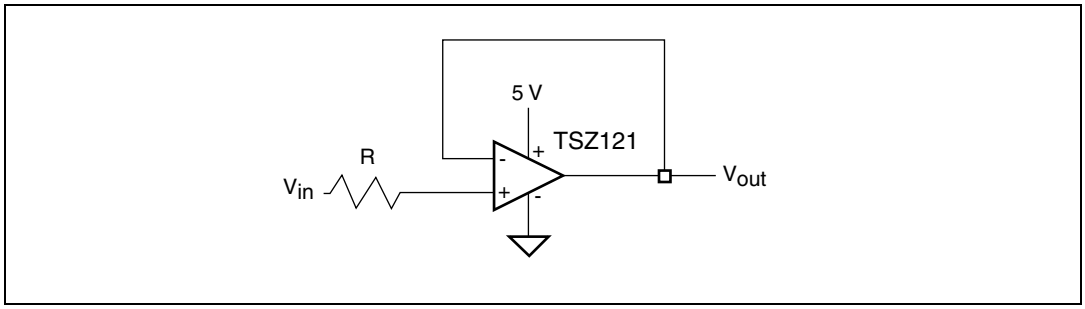
4.3 Input pins voltage range

The TSZ121 device has internal ESD diode protection on the inputs. These diodes are connected between the input and each supply rail to protect the input MOSFETs from electrical discharge.

If the input pin voltage exceeds the power supply by 0.5 V, the ESD diodes become conductive and excessive current can flow through them, and without limitation this overcurrent can damage the device.

In this case, it is important to limit the current to 10 mA, thanks to an added resistance on the input pin, as described in *Figure 40*.

Figure 40. Input current limitation



4.4 Rail-to-rail input

The TSZ12x device has a rail-to-rail input, and the input common mode range is extended from V_{CC-} - 0.1 V to V_{CC+} + 0.1 V.

4.5 Input offset voltage drift over temperature

The maximum input voltage drift over temperature variation is defined as the offset variation related to offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed with *Equation 1*:

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right|$$

with T = -40 °C and 125 °C.

The datasheet maximum value is guaranteed by measurement on a representative sample size ensuring a Cpk greater than 1.3.

4.6 Rail-to-rail output

The operational amplifiers output levels can go close to the rails: 50 mV maximum above and below the rail when connected to a 10 kΩ resistive load to $V_{CC}/2$.

4.7 PCB layout recommendations

Particular attention must be paid to the layout of the PCB, tracks connected to the amplifier, load and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. Good practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

Optimized application recommendation

The TSZ121 device is based on chopper architecture and, being a switched device, it is strongly recommended to place a 0.1 nF + 100 nF capacitor as close as possible to the supply pins.

A good decoupling has several advantages for an application. First, it helps to reduce electromagnetic interference. Due to the modulation of the chopper, the decoupling capacitance also helps to reject the small ripple that may appear on the output.

Moreover, the decoupling capacitor improves the V_{io}, I_{ib} parameter, as shown in *Figure 41* and *Figure 42*.

Figure 41. Influence of decoupling capacitor on V_{io} characteristics

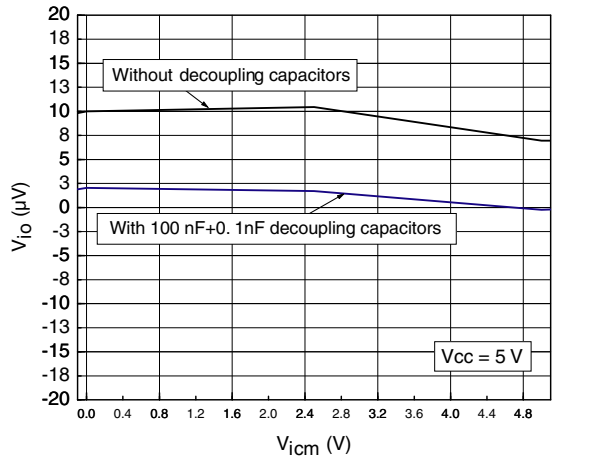
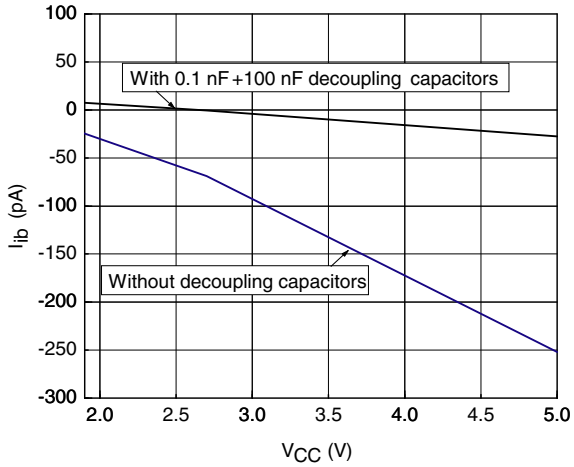


Figure 42. Influence of decoupling capacitor on I_{ib} characteristics



A good decoupling capacitor also improves $\Delta V_{io}/\Delta T$, CMRR, and SVR.

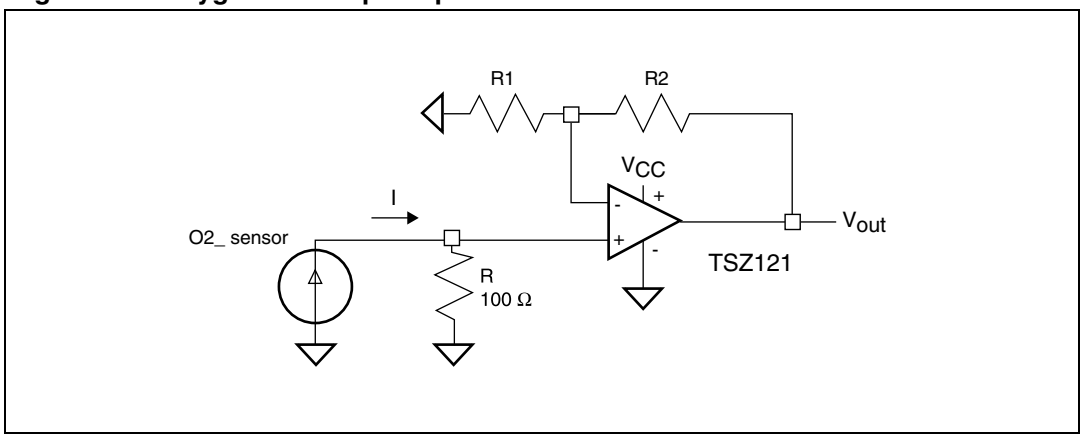
The TSZ121 device has been optimized to be used with 10 kΩ in the feedback loop gain. With this, or a higher value of resistance, the TSZ121 device offers the best performance.

4.8 Application examples

4.8.1 Oxygen sensor

The electrochemical sensor creates a current proportional to the concentration of the gas being measured. This current is converted into voltage thanks to *R* resistance. This voltage is then amplified by the TSZ121 device.

Figure 43. Oxygen sensor principle schematic



The output voltage is:

Equation 2

$$V_{out} = (I \times R - V_{io}) \times \left(\frac{R_2}{R_1} + 1\right)$$

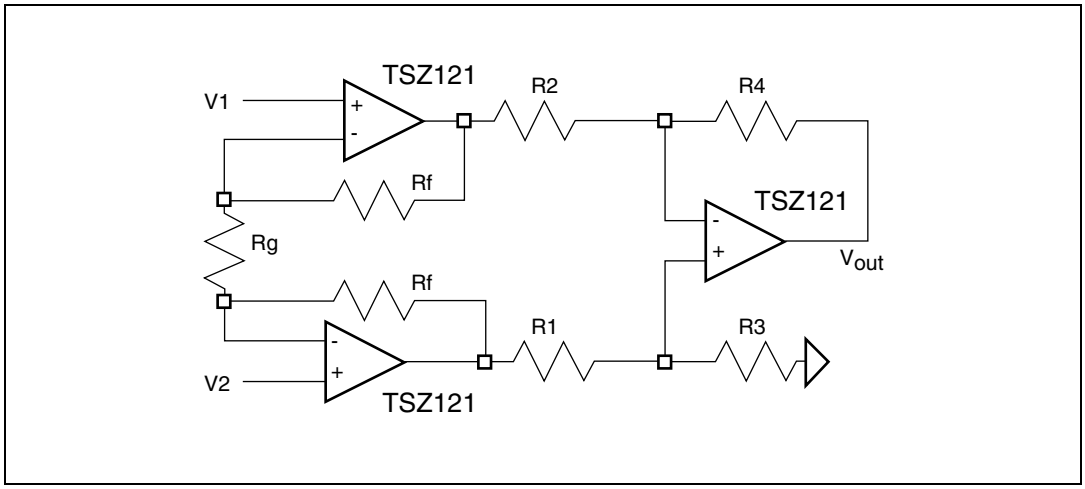
As the current delivered by the O2 sensor is extremely low, the impact of the V_{io} can become significant with a traditional operational amplifier. The use of the TSZ121chopper amplifier, is perfect for this application.

In addition, using the TSZ121 device for the O2 sensor application ensures that the measurement of the O2 concentration is stable even at different temperature thanks to a very good $\Delta V_{io}/\Delta T$.

4.8.2 Precision instrumentation amplifier

The instrumentation amplifier uses three op amps. The circuit, shown in *Figure 44*, exhibits high input impedance, so that source impedance of the connected sensor has no impact on the amplification.

Figure 44. Precision instrumentation amplifier schematic



The gain is set by tuning the Rg resistor. With R1=R2 and R3=R4, the output is given by the following formula:

Equation 3

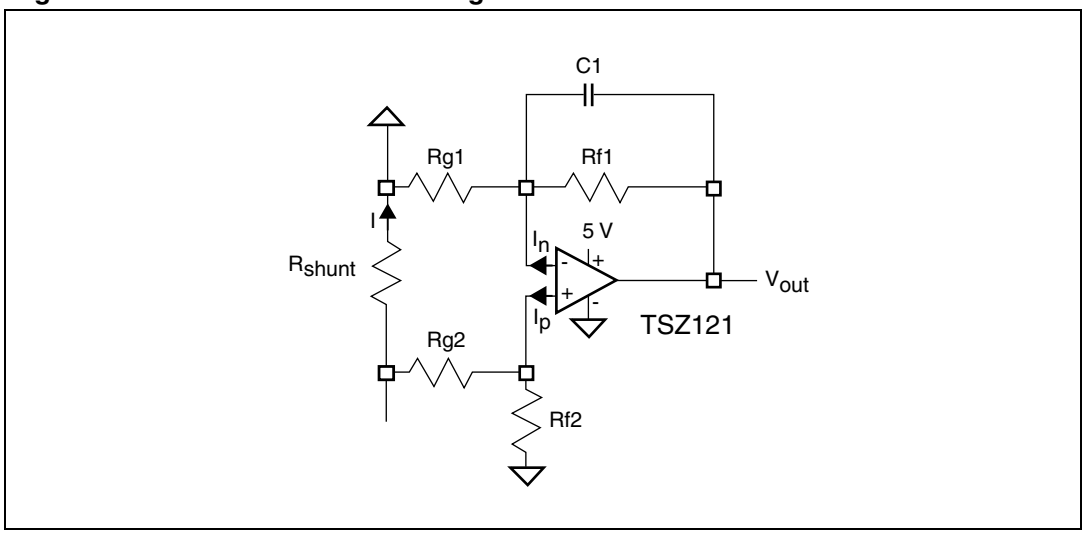
$$V_{out} = (V_2 - V_1) \cdot \left[\frac{R_4}{R_2} \cdot \left(\frac{2R_f}{R_g} + 1\right)\right]$$

The matching of R1, R2 and R3, R4 is important to ensure a good CMRR.

4.8.3 Low-side current sensing

Power management mechanisms are found in most electronic systems. Current sensing is useful for protecting the applications. The low-side current sensing method consists in placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using the TSZ121 device.

Figure 45. Low-side current sensing schematic



V_{out} can be expressed as follows:

Equation 4

$$V_{out} = R_{shunt} \times I\left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}}\right)\left(1 + \frac{R_{f1}}{R_{g1}}\right) + I_p\left(\frac{R_{g2} \times R_{f2}}{R_{g2} + R_{f2}}\right) \times \left(1 + \frac{R_{f1}}{R_{g1}}\right) - I_n \times R_{f1} - V_{io}\left(1 + \frac{R_{f1}}{R_{g1}}\right)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, the equation can be simplified as follows:

Equation 5

$$V_{out} = R_{shunt} \times I\left(\frac{R_f}{R_g}\right) - V_{io}\left(1 + \frac{R_f}{R_g}\right) + R_f \times I_{io}$$

The main advantage of using the TSZ121 chopper, for a low-side current sensing, is that the error due to V_{io} and I_{io} are extremely low and may be neglected.

Therefore, for the same accuracy, the shunt resistor can be chosen with a lower value, resulting in lower power dissipation, lower drop in the ground path and lower cost.

Particular attention must be paid on the matching and precision of R_{g1}, R_{g2}, R_{f1}, and R_{f2}, to maximize the accuracy of the measurement.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 46. SC70-5 package outline

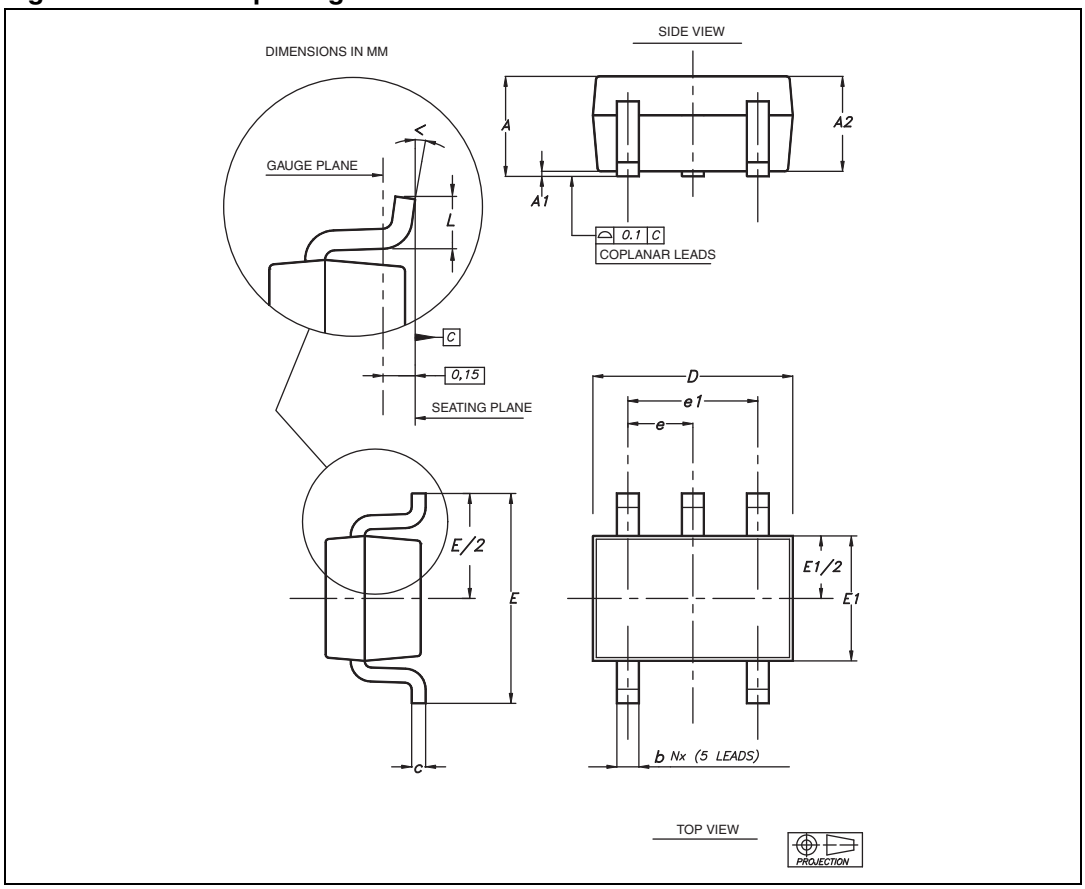


Table 6. SC70-5 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.032		0.043
A1	0		0.10			0.004
A2	0.80	0.90	1.00	0.032	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°			

Figure 47. SOT23 - 5-lead small outline transistor package outline

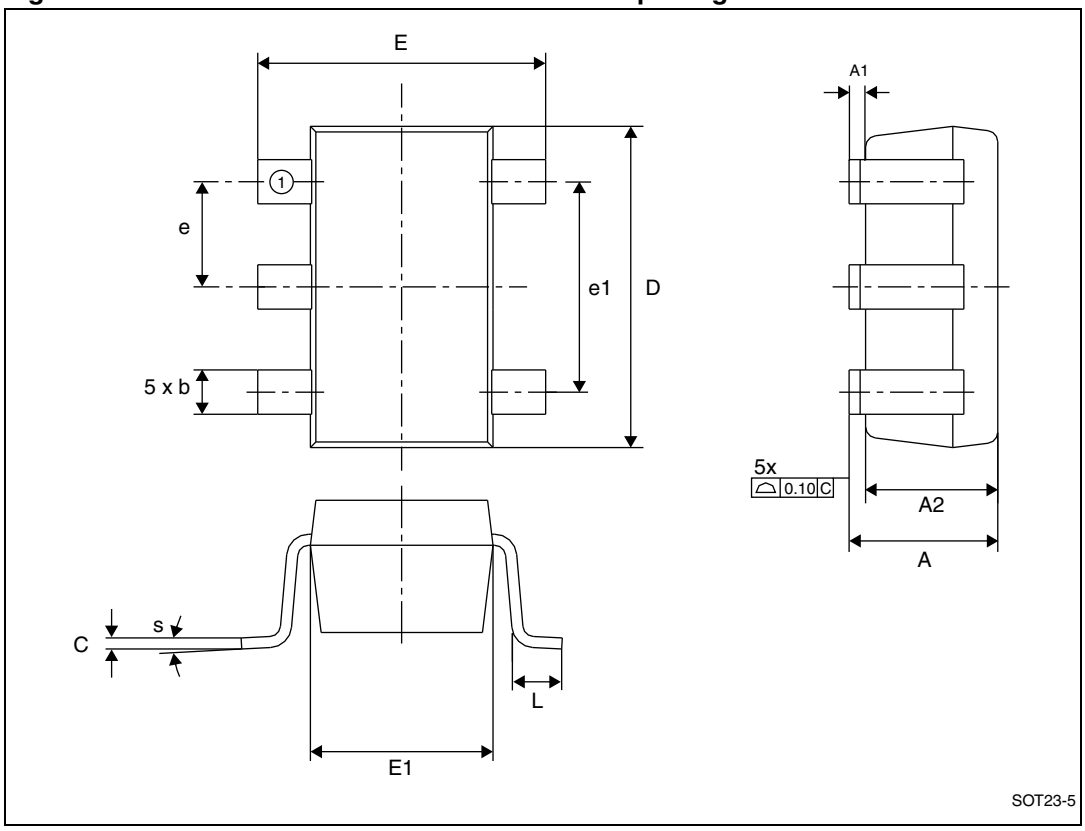
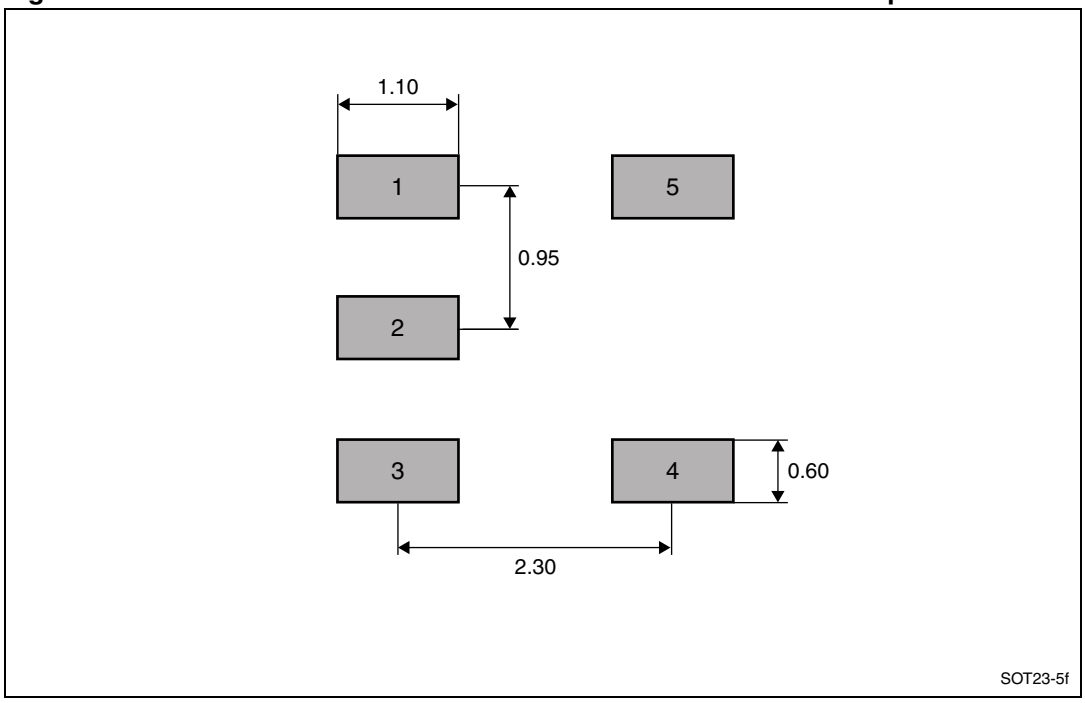


Table 7. SOT23 - 5-lead small outline transistor package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.45			0.057
A1		0.00	0.15		0.000	0.006
A2	1.15	0.90	1.30	0.045	0.035	0.051
b		0.30	0.50		0.012	0.020
c		0.08	0.22		0.003	0.009
D	2.90			0.114		
E	2.80			0.110		
E1	1.60			0.063		
e	0.95			0.037		
e1	1.90			0.075		
L	0.45	0.30	0.60	0.018	0.012	0.024
θ	4	0	8	4	0	8
N	5			5		

Figure 48. SOT23 - 5-lead small outline transistor recommended footprint



6 Ordering information

Table 8. Order codes

Order code	Temperature range	Package	Packaging	Marking
TSZ121ICT	-40 to +125 °C	SC70-5	Tape and reel	K44
TSZ121ILT		SOT23-5		K143

7 Revision history

Table 9. Document revision history

Date	Revision	Changes
16-Aug-2012	1	Initial release.