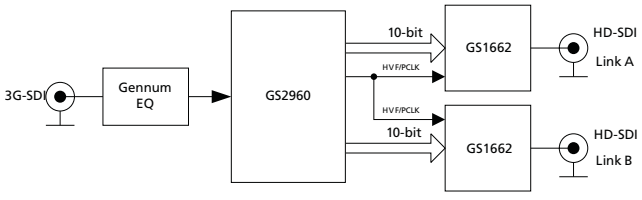
GS1662 HD/SD-SDI Serializer with Complete SMPTE Video Support

Key Features

- Operation at 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE 292, SMPTE 259M-C and DVB-ASI
- Integrated Cable Driver
- Integrated, low-noise VCO
- Integrated ClockCleaner™
- Ancillary data insertion
- Parallel data bus selectable as either 20-bit or 10-bit
- SMPTE video processing including TRS calculation and insertion, line number calculation and insertion, line based CRC calculation and insertion, illegal code re-mapping, SMPTE 352M payload identifier generation and insertion
- GSPI host interface
- 1.2V digital core power supply, 1.2V and 3.3V analog power supplies, and selectable 1.8V or 3.3V I/O power supply
- -20°C to +85°C operating temperature range
- Low power operation (typically at 330mW, including Cable Driver)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and RoHS compliant

Applications

Application: Single Link (3G-SDI) to Dual Link (HD-SDI) Converter



Description

The GS1662 is a complete SDI Transmitter, generating a SMPTE 292, SMPTE 259M-C or DVB-ASI compliant Serial Digital Output signal.

The integrated ClockCleaner™ allows the device to accept parallel clocks with greater than 300ps input jitter and still provide a SMPTE compliant serial digital output.

The device can operate in four basic user selectable modes: SMPTE mode, DVB-ASI mode, Data-Through mode, or Standby mode.

In SMPTE mode, the GS1662 performs SMPTE scrambling and NRZ to NRZI coding. In addition, the device can insert TRS words, calculate and insert line numbers and line based CRC's, re-map illegal code words, map 8-bit TRS to 10-bit TRS, calculate and insert EDH CRC's and flags, and insert SMPTE 352M payload identifier packets. All of the processing features are optional, and may be disabled via external control pins and/or via the Host Interface.

The GS1662 provides ancillary data insertion in SMPTE mode as well. The entire ancillary packet is programmed into internal registers through the GSPI Host Interface, including the Ancillary Data Flag (ADF), Data Identification words (DID and SDID) and checksum. The GS1662 then recalculates the checksum and inserts the complete ancillary packet into the video stream.

In DVB-ASI mode, the device will perform 8b/10b encoding prior to transmission.

In Data-Through mode, all SMPTE and DVB-ASI processing is disabled, and the device can be used as a simple parallel to serial converter.

The device can also operate in a lower power Standby mode. In this mode, no signal is generated at the output.

Parallel data inputs must be provided in 20-bit or 10-bit multiplexed format for HD and SD video rates. The associated Parallel Clock input signal operates at 148.5 or 148.5/1.001MHz (HD 10-bit multiplexed format), 74.25 or 74.25/1.001MHz (for HD 20-bit format), 27MHz (for SD 10-bit format) and 13.5MHz (for SD 20-bit format).

The GS1662 includes an integrated Cable Driver fully compliant with SMPTE 259M-C and SMPTE 292M. It features automatic dual slew-rate selection, depending on HD or SD operational requirements.

Functional Block Diagram

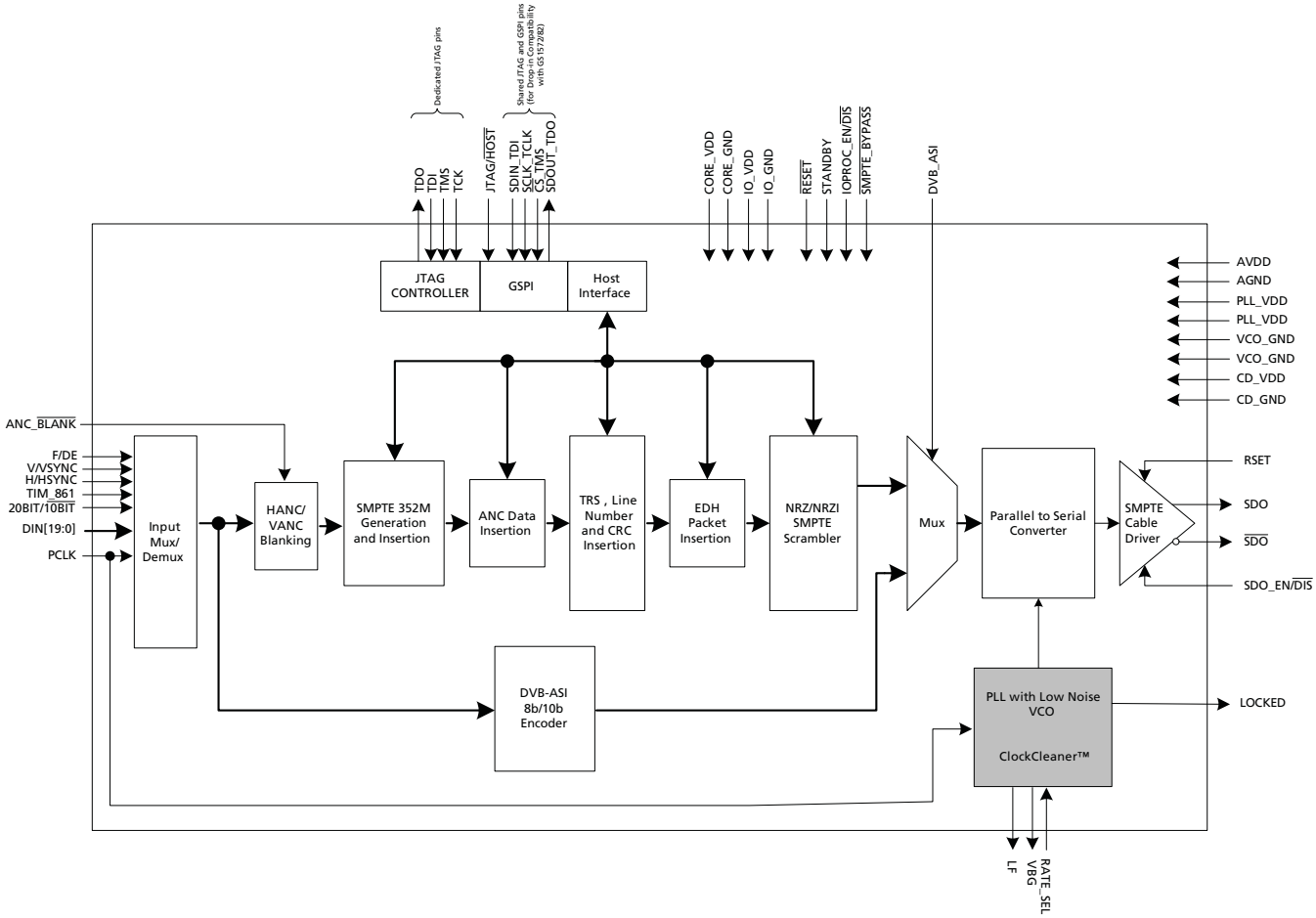


Figure A: GS1662 Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
3	155080	56060	October 2010	Revised power rating in standby mode. Documented CSUM behaviour in Section 4.7, Section 4.8.3 and Configuration and Status Registers.
2	153743	–	March 2010	Correction to ANC Data Insertion addresses 040h - 13Fh in Table 4-16: Configuration and Status Registers. Changed Reset Pulse width from 10ms to 1ms in Table 2-4: AC Electrical Characteristics and 4.16 Device Reset. Changed Pin E4 to IO_GND.
1	153472	–	January 2010	Converted to Data Sheet.
0	153210	–	November 2009	Converted to Preliminary Data Sheet. Changed pin E4 to RSV in Pin Assignment, Pin Descriptions and Typical Application Circuit.
A	152910	–	October 2009	New Document.

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1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	DIN17	DIN18	F/DE	H/HSYNC	CORE_VDD	PLL_VDD	LF	VBG	RSV	A_VDD
B	DIN15	DIN16	DIN19	PCLK	CORE_GND	PLL_VDD	VCO_VDD	VCO_GND	A_GND	A_GND
C	DIN13	DIN14	DIN12	V/VSYNC	CORE_GND	PLL_GND	PLL_GND	PLL_GND	CD_GND	SDO
D	DIN11	DIN10	STANDBY	SDO_EN/$\overline{DIS}$	CORE_GND	RSV	RSV	RSV	CD_GND	$\overline{SDO}$
E	CORE_VDD	CORE_GND	RATE_SEL	IO_GND	CORE_GND	CORE_GND	TDI	TMS	CD_GND	CD_VDD
F	DIN9	DIN8	DETECT_TRS	CORE_GND	CORE_GND	CORE_GND	CORE_GND	TDO	CD_GND	RSET
G	IO_VDD	IO_GND	TIM_861	20bit/$\overline{10bit}$	DVB_ASI	$\overline{SMPTE\_BYPASS}$	IOPROC_EN/$\overline{DIS}$	$\overline{RESET}$	CORE_GND	CORE_VDD
H	DIN7	DIN6	$\overline{ANC\_BLANK}$	LOCKED	CORE_GND	CORE_GND	RSV	JTAG/$\overline{HOST}$	IO_GND	IO_VDD
J	DIN5	DIN4	DIN1	RSV	RSV	RSV	RSV	TCK	SDOUT_TDO	SCLK_TCK
K	DIN3	DIN2	DIN0	RSV	RSV	RSV	RSV	CORE_VDD	$\overline{CS}$_TMS	SDIN_TDI

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description	
A1, A2, B1, B2, B3, C1, C2, C3, D1, D2	DIN[19:10]		Input	PARALLEL DATA BUS Signal levels are LVCMOS / LVTTL compatible.	
				20-bit mode 20BIT/$\overline{10BIT}$ = HIGH	Luma data input in SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH) Data input in data through mode ($\overline{SMPTE\_BYPASS}$ = LOW)
				10-bit mode 20BIT/$\overline{10BIT}$ = LOW	Multiplexed Luma and Chroma data input in SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH) Data input in data through mode ($\overline{SMPTE\_BYPASS}$ = LOW) DVB-ASI data input in DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW) (DVB_ASI = HIGH)
A3	F/DE	Synch-ronous with PCLK	Input	PARALLEL DATA TIMING. Signal levels are LVCMOS / LVTTL compatible. TIM_861 = LOW: Used to indicate the ODD / EVEN field of the video signal when DETECT_TRS is set LOW. The device will set the F bit in all outgoing TRS signals for the entire period that the F input signal is HIGH (IOPROC_EN/$\overline{DIS}$ must also be HIGH). The F signal should be set HIGH for the entire period of field 2 and should be set LOW for all lines in field 1 and for all lines in progressive scan systems. The F signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The DE signal is used to indicate the active video period when DETECT_TRS is set LOW. DE is HIGH for active data and LOW for blanking. See Section 4.3 and Section 4.3.2 for timing details. The DE signal is ignored when DETECT_TRS = HIGH.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
A4	H/HSYNC	Synch-ronous with PCLK	Input	PARALLEL DATA TIMING. Signal levels are LVCMOS / LVTTL compatible. TIM_861 is LOW: The H signal is used to indicate the portion of the video line containing active video data, when DETECT_TRS is set LOW. Active Line Blanking The H signal should be LOW for the active portion of the video line. The signal goes LOW at the first active pixel of the line, and then goes HIGH after the last active pixel of the line. The H signal should be set HIGH for the entire horizontal blanking period, including both EAV and SAV TRS words, and LOW otherwise. TRS Based Blanking (H_CONFIG = 1_h) The H signal should be set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words, and LOW otherwise. TIM_861 = HIGH: The HSYNC signal indicates horizontal timing. See Section 4.3. When DETECT_TRS is HIGH, this pin is ignored at all times. If DETECT_TRS is set HIGH and TIM_861 is set HIGH, the DETECT_TRS feature will take priority.
A5, E1, G10, K8	CORE_VDD		Input Power	Power supply connection for digital core logic. Connect to 1.2V DC digital.
A6, B6	PLL_VDD		Input Power	Power supply pin for PLL. Connect to 1.2V DC analog.
A7	LF		Analog Output	Loop Filter component connection.
A8	VBG		Output	Bandgap voltage filter connection.
A9, D6, D7, D8, H7, J4, J5, J6, J7, K4, K5, K6, K7	RSV		–	These pins are reserved and should be left unconnected.
A10	A_VDD		Input Power	VDD for sensitive analog circuitry. Connect to 3.3VDC analog.
B4	PCLK		Input	PARALLEL DATA BUS CLOCK. Signal levels are LVCMOS / LVTTL compatible. HD 20-bit mode: PCLK @ 74.25MHz HD 10-bit mode: PCLK @ 148.5MHz SD 20-bit mode: PCLK @ 13.5MHz SD 10-bit mode: PCLK @ 27MHz DVB-ASI mode: PCLK @ 27MHz
B5, C5, D5, E2, E5, E6, F4, F5, F6, F7, G9, H5, H6	CORE_GND		Input Power	Reserved. Connect to CORE_GND.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
B7	VCO_VDD		Input Power	Power pin for VCO. Connect to 1.2V DC analog followed by an RC filter (see Typical Application Circuit on page 68). VCO_VDD is nominally 0.7V.
B8	VCO_GND		Input Power	Ground connection for VCO. Connect to analog GND.
B9, B10	A_GND		Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.
C4	V/VSYNC	Synch-ronous with PCLK	Input	PARALLEL DATA TIMING. Signal levels are LVCMOS / LVTTL compatible. TIM_861 = LOW: The V signal is used to indicate the portion of the video field/frame that is used for vertical blanking, when DETECT_TRS is set LOW. The V signal should be set HIGH for the entire vertical blanking period and should be set LOW for all lines outside of the vertical blanking interval. The V signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The VSYNC signal indicates vertical timing. See Section 4.3 for timing details. The VSYNC signal is ignored when DETECT_TRS = HIGH.
C6, C7, C8	PLL_GND		Input Power	Ground connection for PLL. Connect to analog GND.
C9, D9, E9, F9	CD_GND		Input Power	Ground connection for the serial digital cable driver. Connect to analog GND.
C10, D10	SDO, $\overline{\text{SDO}}$		Output	Serial Data Output Signal. Serial digital output signal operating at 1.485Gb/s, 1.485 /1.001Gb/s or 270Mb/s. The slew rate of the output is automatically controlled to meet SMPTE 292 and 259M specifications according to the setting of the RATE_SEL pin.
D3	STANDBY		Input	Standby input. HIGH to place the device in Standby mode.
D4	SDO_EN/$\overline{\text{DIS}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Used to enable or disable the serial digital output stage. When SDO_EN/$\overline{\text{DIS}}$ is LOW, the serial digital output signals SDO and $\overline{\text{SDO}}$ are disabled and become high impedance. When SDO_EN/$\overline{\text{DIS}}$ is HIGH, the serial digital output signals SDO and $\overline{\text{SDO}}$ are enabled.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
E3	RATE_SEL		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to configure the operating data rate. RATE_SEL: 0 → Data Rate: 1.485 or 1.485/1.001Gb/s RATE_SEL: 1 → Data Rate: 270Mb/s
E7	TDI		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Dedicated JTAG pin. Test data in. This pin is used to shift JTAG test data into the device when the JTAG/$\overline{\text{HOST}}$ pin is LOW.
E8	TMS		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Dedicated JTAG pin. Test mode start. This pin is JTAG Test Mode Start, used to control the operation of the JTAG test when the JTAG/$\overline{\text{HOST}}$ pin is LOW.
E10	CD_VDD		Input Power	Power for the serial digital cable driver. Connect to 3.3V DC analog.
F1, F2, H1, H2, J1, J2, J3, K1, K2, K3	DIN[9:0]		Input	PARALLEL DATA BUS. Signal levels are LVCMOS / LVTTL compatible. In 10-bit mode, these pins are not used. 20-bit mode (20BIT/$\overline{\text{10BIT}}$ = HIGH): Chroma data input in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH, DVB_ASI = LOW); Data input in data through mode ($\overline{\text{SMPTE\_BYPASS}}$ = LOW, DVB_ASI = LOW); Not Used in DVB-ASI mode ($\overline{\text{SMPTE\_BYPASS}}$ = LOW, DVB_ASI = HIGH) 10-bit mode (20BIT/$\overline{\text{10BIT}}$ = LOW): Not used.
F3	DETECT_TRS		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Used to select external HVF timing mode or TRS extraction timing mode. When DETECT_TRS is LOW, the device extracts all internal timing from the supplied H:V:F or CEA-861 timing signals, dependent on the status of the TIM861 pin. When DETECT_TRS is HIGH, the device extracts all internal timing from TRS signals embedded in the supplied video stream.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
F8	TDO		Output	COMMUNICATION SIGNAL OUTPUT. Signal levels are LVCMOS/LVTTL compatible. Dedicated JTAG pin. JTAG Test Data Output. This pin is used to shift results from the device when the JTAG/$\overline{\text{HOST}}$ pin is LOW.
F10	RSET		Input	An external 1% resistor connected to this input is used to set the SDO/$\overline{\text{SDO}}$ output signal amplitude.
G1, H10	IO_VDD		Input Power	Power connection for digital I/O. Connect to 3.3V or 1.8V DC digital.
E4, G2, H9	IO_GND		Input Power	Ground connection for digital I/O. Connect to digital GND.
G3	TIM_861		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Used to select external CEA-861 timing mode. When DETECT_TRS is LOW and TIM-861 is LOW, the device extracts all internal timing from the supplied H:V:F timing signals. When DETECT_TRS is LOW and TIM-861 is HIGH, the device extracts all internal timing from the supplied HSYNC, VSYNC, DE timing signals. When DETECT_TRS is HIGH, the device extracts all internal timing from TRS signals embedded in the supplied video stream.
G4	20bit/$\overline{\text{10bit}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to select the input bus width.
G5	DVB_ASI		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable/disable the DVB-ASI data transmission. When DVB_ASI is set HIGH and $\overline{\text{SMPTE\_BYPASS}}$ is set LOW, then the device will carry out DVB-ASI word alignment, I/O processing and transmission. When $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in data-through mode.
G6	$\overline{\text{SMPTE\_BYPASS}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to enable / disable all forms of encoding / decoding, scrambling and EDH insertion. When set LOW, the device operates in data through mode (DVB_ASI= LOW), or in DVB-ASI mode (DVB_ASI = HIGH). No SMPTE scrambling takes place and none of the I/O processing features of the device are available when $\overline{\text{SMPTE\_BYPASS}}$ is set LOW. When set HIGH, the device carries out SMPTE scrambling and I/O processing.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G7	IOPROC_EN/$\overline{\text{DIS}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the I/O processing features. When IOPROC_EN/$\overline{\text{DIS}}$ is HIGH, the I/O processing features of the device are enabled. When IOPROC_EN/$\overline{\text{DIS}}$ is LOW, the I/O processing features of the device are disabled. Only applicable in SMPTE mode.
G8	$\overline{\text{RESET}}$		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG sequence. Normal mode (JTAG/$\overline{\text{HOST}}$ = LOW). When LOW, all functional blocks will be set to default conditions and all input and output signals become high impedance. When HIGH, normal operation of the device resumes. JTAG test mode (JTAG/$\overline{\text{HOST}}$ = HIGH). When LOW, all functional blocks will be set to default and the JTAG test sequence will be reset. When HIGH, normal operation of the JTAG test sequence resumes.
H3	$\overline{\text{ANC\_BLANK}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. When $\overline{\text{ANC\_BLANK}}$ is LOW, the Luma and Chroma input data is set to the appropriate blanking levels during the H and V blanking intervals. When $\overline{\text{ANC\_BLANK}}$ is HIGH, the blanking function is disabled. Only applicable in SMPTE mode.
H4	LOCKED		Output	STATUS SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. PLL lock indication. HIGH indicates PLL is locked. LOW indicates PLL is not locked.
H8	JTAG/$\overline{\text{HOST}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Used to select JTAG test mode or host interface mode. When JTAG/$\overline{\text{HOST}}$ is HIGH, the host interface port is configured for JTAG test. When JTAG/$\overline{\text{HOST}}$ is LOW, normal operation of the host interface port resumes and the separate JTAG pins become the JTAG port.
J8	TCK		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. JTAG Serial Data Clock Signal. This pin is the JTAG clock when the JTAG/$\overline{\text{HOST}}$ pin is LOW.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
J9	SDOUT_TDO		Output	COMMUNICATION SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. Shared JTAG/$\overline{\text{HOST}}$ pin. Provided for compatibility with the GS1582. Serial Data Output/Test Data Output. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) This pin operates as the host interface serial output, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is used to shift test results and operates as the JTAG test data output, TDO (for new designs, use the dedicated JTAG port). NOTE: If the host interface is not being used leave this pin unconnected. IO_VDD = 3.3V Drive Strength = 12mA IO_VDD = 1.8V Drive Strength = 4mA
J10	SCLK_TCK		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Shared JTAG/HOST pin. Provided for pin compatibility with GS1582. Serial data clock signal. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SCLK_TCK operates as the host interface burst clock, SCLK. Command and data read/write words are clocked into the device synchronously with this clock. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is the TEST MODE START pin, used to control the operation of the JTAG test clock, TCK (for new designs, use the dedicated JTAG port). NOTE: If the host interface is not being used, tie this pin HIGH.
K9	$\overline{\text{CS}}$_TMS		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Chip select / test mode start. JTAG Test mode (JTAG/$\overline{\text{HOST}}$ = HIGH) $\overline{\text{CS}}$_TMS operates as the JTAG test mode start, TMS, used to control the operation of the JTAG test, and is active HIGH (for new designs, use the dedicated JTAG port). Host mode (JTAG/$\overline{\text{HOST}}$ = LOW), $\overline{\text{CS}}$_TMS operates as the host interface Chip Select, $\overline{\text{CS}}$, and is active LOW.
K10	SDIN_TDI		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Shared JTAG/HOST pin. Provided for pin compatibility with GS1582. Serial data in/test data in. In JTAG mode, this pin is used to shift test data into the device (for new designs, use the dedicated JTAG port). In host interface mode, this pin is used to write address and configuration data words into the device.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +3.6V
Supply Voltage, Analog 1.2V (PLL_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (CD_VDD, A_VDD)	-0.3V to +3.6V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Operating Temperature Range	-20°C to +85°C
Functional Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

NOTES:

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	–	85	°C	–
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, VCO	VCO_VDD	–	–	0.7	–	V	1
Supply Voltage, Analog	A_VDD	–	3.13	3.3	3.47	V	–
Supply Voltage, CD	CD_VDD	–	3.13	3.3	3.47	V	–

NOTES:

1. This is 0.7V rather than 1.2V because there is a voltage drop across an external 105Ω resistor. See Typical Application Circuit on page 68.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = -20°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I_{1V2}	10/20bit HD	–	90	150	mA	–
		10/20bit SD	–	75	120	mA	–
		DVB_ASI	–	75	120	mA	–
+1.8V Supply Current	I_{1V8}	10/20bit HD	–	10	25	mA	–
		10/20bit SD	–	3	10	mA	–
		DVB_ASI	–	3	10	mA	–
+3.3V Supply Current	I_{3V3}	10/20bit HD	–	80	100	mA	–
		10/20bit SD	–	70	90	mA	–
		DVB_ASI	–	70	90	mA	–
Total Device Power (IO_VDD = 1.8V)	P_{1D8}	10/20bit HD	–	330	490	mW	–
		10/20bit SD	–	300	450	mW	–
		DVB_ASI	–	300	410	mW	–
		Reset	–	200	–	mW	–
		Standby	–	100	180	mW	–
Total Device Power (IO_VDD = 3.3V)	P_{3D3}	10/20bit HD	–	370	500	mW	–
		10/20bit SD	–	320	450	mW	–
		DVB_ASI	–	320	450	mW	–
		Reset	–	230	–	mW	–
		Standby	–	110	180	mW	–
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	IO_VSS-0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_VDD+0.3	V	–
Output Logic LOW	V_{OL}	IOL=5mA, 1.8V operation	–	–	0.2	V	–
		IOL=8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	IOH=-5mA, 1.8V operation	1.4	–	–	V	–
		IOH=-8mA, 3.3V operation	2.4	–	–	V	–
Serial Output							
Serial Output Common Mode Voltage	V_{CMOUT}	75Ω load, RSET = 750Ω SD and HD mode	2.5	SDI_VDD - (0.75/2)	SDI_VDD - (0.55/2)	V	–

NOTES:

1. Devices manufactured prior to April 1, 2011 consume 150mW of power in Standby mode.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = -20°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Device Latency	–	HD bypass (PCLK = 148MHz)	–	54	–	PCLK	–
	–	HD SMPTE without audio (PCLK = 148MHz)	–	95	–	PCLK	–
	–	HD SMPTE with audio (PCLK = 148MHz)	–	1106	–	PCLK	–
	–	SD bypass (PCLK = 27 MHz)	–	54	–	PCLK	–
	–	SD SMPTE without audio	–	112	–	PCLK	–
	–	SD SMPTE with audio	–	638	–	PCLK	–
	–	DVB-ASI	–	52	–	PCLK	–
Reset Pulse Width	t_{reset}	–	1	–	–	ms	–
Parallel Input							
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–
Input Data Setup Time	t_{su}	50% levels; 3.3V or 1.8V operation	1.2	–	–	ns	1
Input Data Hold Time	t_{ih}		0.8	–	–	ns	1
Serial Digital Output							
Serial Output Data Rate	DR_{SDO}	–	–	1.485	–	Gb/s	–
		–	–	1.485/1.001	–	Gb/s	–
		–	–	270	–	Mb/s	–
Serial Output Swing	V_{SDD}	RSET = 750Ω 75Ω load	750	800	850	mVp-p	–
Serial Output Rise/Fall Time 20% ~ 80%	trf_{SDO}	HD mode	–	120	135	ps	–
	trf_{SDO}	SD mode	400	660	800	ps	–
Mismatch in rise/fall time	$\Delta t_r, \Delta t_f$	–	–	–	35	ps	–
Duty Cycle Distortion	–	–	–	–	5	%	2
Overshoot	–	HD mode	–	5	10	%	2
	–	SD mode	–	3	8	%	2
Output Return Loss	ORL	5 MHz - 1.485 GHz	–	-18	–	dB	3

Table 2-4: AC Electrical Characteristics (Continued)

V_{CC} = 3.3V ±5%, T_A = -20°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Output Intrinsic Jitter	t_{OJ}	Pseudorandom and SMPTE Colour Bars HD signal	–	50	95	ps	4, 6
	t_{OJ}	Pseudorandom and SMPTE Colour Bars SD signal	–	200	400	ps	5
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	80	MHz	–
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	–
GSPI Input Data Setup Time	–		1.5	–	–	ns	–
GSPI Input Data Hold Time	–		1.5	–	–	ns	–
GSPI Output Data Hold Time	–	15pF load	1.5	–	–	ns	–
$\overline{CS}$ low before SCLK rising edge	t_0	50% levels 3.3V or 1.8V operation	1.5	–	–	ns	–
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	t_4	50% levels 3.3V or 1.8V operation	PCLK (MHz) / ns unlocked / 445 13.5 / 74.2 27.0 / 37.1 74.25 / 13.5 148.5 / 6.7	–	–	ns	–
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	t_5	50% levels 3.3V or 1.8V operation	PCLK (MHz) / ns unlocked / 1187 13.5 / 297 27.0 / 148.4 74.25 / 53.9 148.5 / 27	–	–	ns	–
$\overline{CS}$ high after SCLK falling edge	t_7	50% levels 3.3V or 1.8V operation	PCLK (MHz) / ns unlocked / 445 13.5 / 74.2 27.0 / 37.1 74.25 / 13.5 148.5 / 6.7	–	–	ns	–

NOTES:

1. Input setup and hold time is dependent on the rise and fall time on the parallel input. Parallel clock and data with rise time or fall time greater than 500ps require larger setup and hold times.
2. Single Ended into 75Ω external load.
3. ORL depends on board design.
4. Alignment Jitter = measured from 100kHz to serial data rate/10.
5. Alignment Jitter = measured from 1kHz to 27MHz.
6. This is the maximum jitter for a BER of 10-12. The equivalent jitter value as per RP184 is 40ps max.

3. Input/Output Circuits

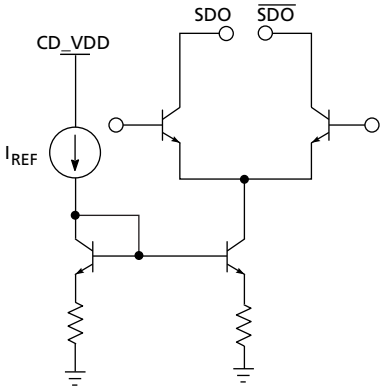


Figure 3-1: Differential Output Stage (SDO/SDO)

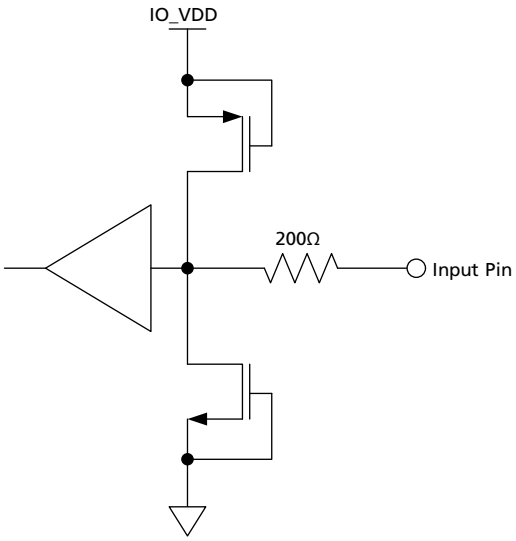


Figure 3-2: Digital Input Pin (20bit/10bit, ANC_BLANK, DETECT_TRS, DVB_ASI, RATE_SEL, SMPTE_BYPASS, TIM_861, F/DE, H/HSYNC, PCLK, V/VSYNC)

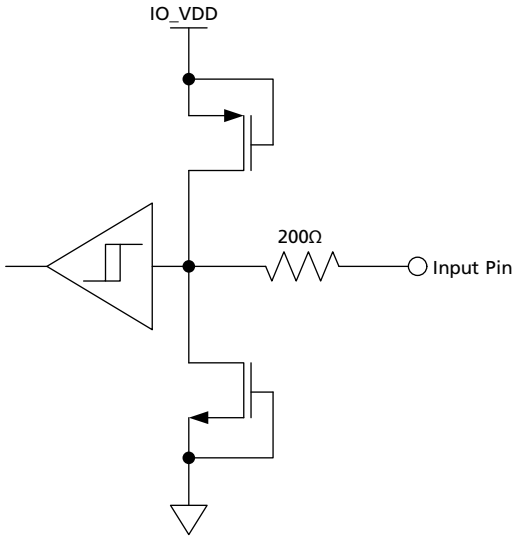


Figure 3-3: Digital Input Pin with Schmitt Trigger ($\overline{\text{RESET}}$)

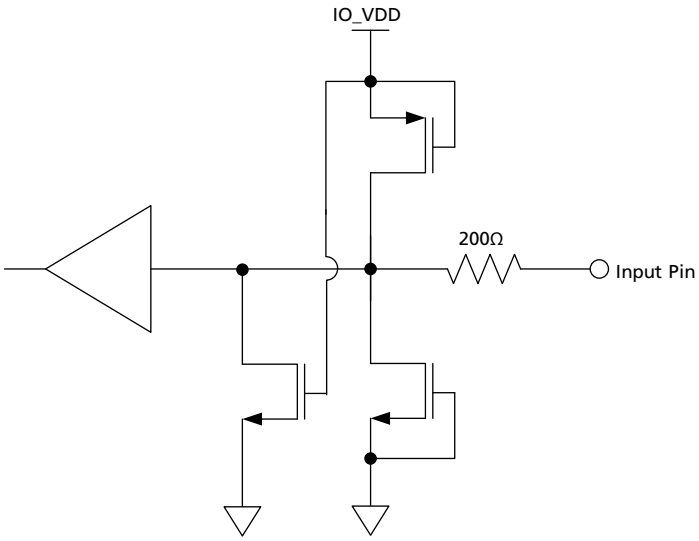


Figure 3-4: Digital Input Pin with weak pull-down - maximum pull-down current <110mA (JTAG/$\overline{\text{HOST}}$, STANDBY, SCLK_TCK, SDIN_TDI, TCK, TDI)

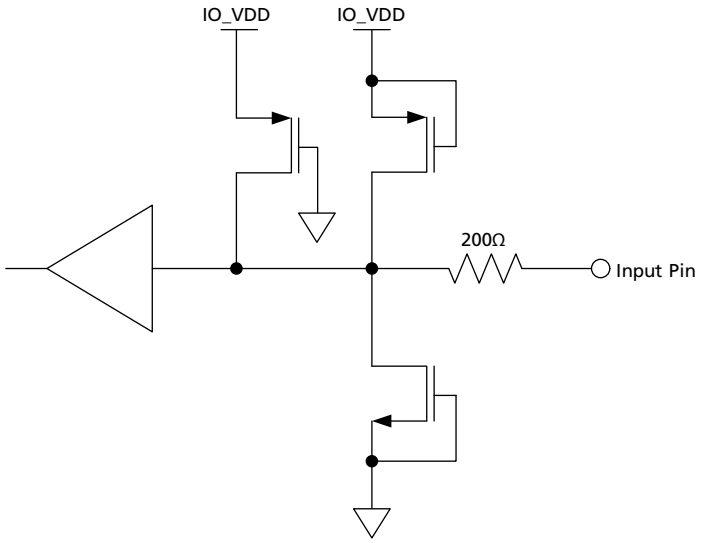


Figure 3-5: Digital Input Pin with weak pull-up - maximum pull-up current <110mA ($\overline{CS}$_TMS, SDO_EN/$\overline{DIS}$, TMS)

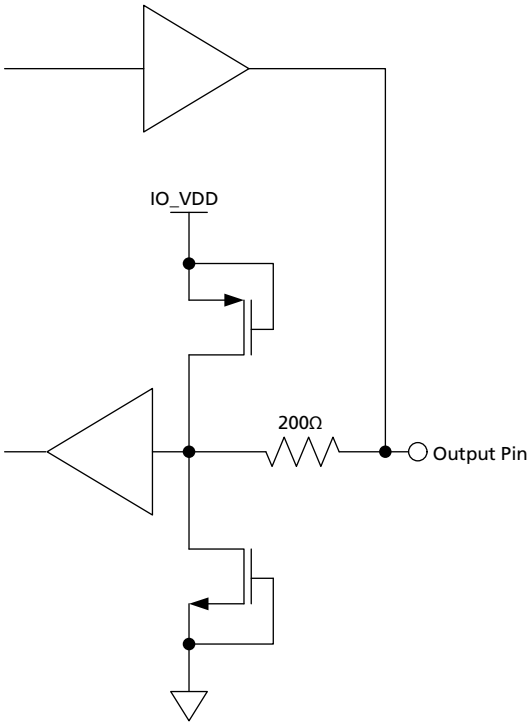


Figure 3-6: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to input at all times except in test mode. (DIN0, DIN2, DIN3, DIN4, DIN5, DIN6, DIN7, DIN8, DIN9, DIN10, DIN11, DIN12, DIN13, DIN14, DIN15, DIN16, DIN17, DIN18, DIN19, DIN1)

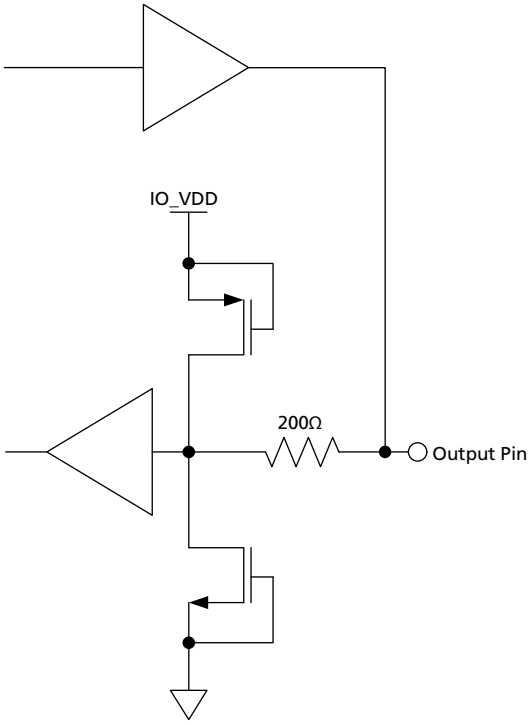


Figure 3-7: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to output at all times except in reset mode. (LOCKED, SDOUT_TDO, TDO)

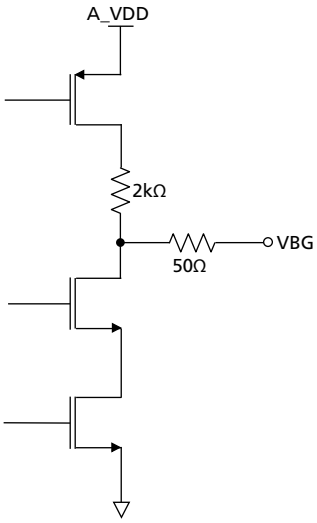


Figure 3-8: VBG

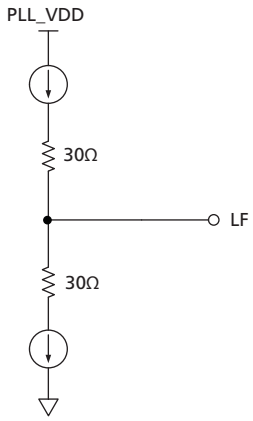


Figure 3-9: Loop Filter

4. Detailed Description

4.1 Functional Overview

The GS1662 is a multi-rate Transmitter with integrated SMPTE digital video processing and an integrated Cable Driver. It provides a complete transmit solution at 1.485Gb/s, 1.485/1.001Gb/s or 270Mb/s.

The device has four basic modes of operation that must be set through external device pins: SMPTE mode, DVB-ASI mode, Data-Through mode and Standby mode.

In SMPTE mode, the device will accept 10-bit multiplexed or 20-bit demultiplexed SMPTE compliant data. By default, the device's additional processing features will be enabled in this mode.

In DVB-ASI mode, the GS1662 will accept an 8-bit parallel DVB-ASI compliant transport stream on DIN[17:10]. The serial output data stream will be 8b/10b encoded with stuffing characters added as per the standard.

Data-Through mode allows for the serializing of data not conforming to SMPTE or DVB-ASI streams. No additional processing will be done in this mode.

In addition, the device may be put into Standby, to reduce power consumption.

The serial digital output features a high-impedance mode and adjustable signal swing. The output slew rate is automatically set by the RATE_SEL pin setting.

The GS1662 provides several data processing functions; including generic ANC insertion, SMPTE 352M and EDH data packet generation and insertion, automatic video standards detection, and TRS, CRC, ANC data checksum, and line number calculation and insertion. These features are all enabled/disabled collectively using the external I/O processing pin, but may be individually disabled via internal registers accessible through the GSPI host interface.

Finally, the GS1662 contains a JTAG interface for boundary scan test implementations.

4.2 Parallel Data Inputs

Data signal inputs enter the device on the rising edge of PCLK, as shown in Figure 4-1.

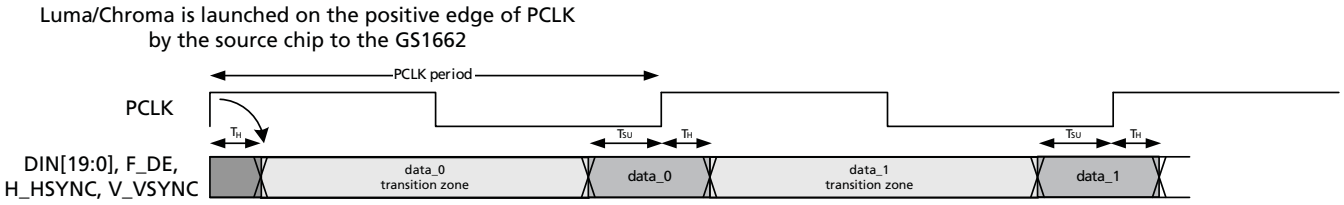


Figure 4-1: GS1662 Video Host Interface Timing Diagrams

Table 4-1: GS1662 Digital Input AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input data set-up time	t_{SU}	50% levels; 1.8V operation	1.2	–	–	ns
Input data hold time	t_{IH}		0.8	–	–	ns
Input data set-up time	t_{SU}	50% levels; 3.3V operation	1.3	–	–	ns
Input data hold time	t_{IH}		0.8	–	–	ns

Table 4-2: GS1662 Input Video Data Format Selections

Input Data Format	Pin/Register Bit Settings				DIN[9:0]	DIN[19:10]
	20BIT /10BIT	RATE _SEL	SMPTE _BYPASS	DVB_ASI		
20-bit demultiplexed HD format	HIGH	LOW	HIGH	LOW	Chroma	Luma
20-bit data Input HD format	HIGH	LOW	LOW	LOW	DATA	DATA
20-bit demultiplexed SD format	HIGH	HIGH	HIGH	LOW	Chroma	Luma
20-bit data input SD format	HIGH	HIGH	LOW	LOW	DATA	DATA
10-bit multiplexed HD format	LOW	LOW	HIGH	LOW	High Impedance	Luma/Chroma
10-bit data input HD format	LOW	LOW	LOW	LOW	High Impedance	DATA
10-bit multiplexed SD format	LOW	HIGH	HIGH	LOW	High Impedance	Luma/Chroma

Table 4-2: GS1662 Input Video Data Format Selections (Continued)

Input Data Format	Pin/Register Bit Settings				DIN[9:0]	DIN[19:10]
	20BIT /10BIT	RATE _SEL	SMPTE _BYPASS	DVB_ASI		
10-bit multiplexed SD format	LOW	HIGH	LOW	LOW	High Impedance	DATA
10-bit ASI input SD format	LOW	HIGH	LOW	HIGH	High Impedance	DVB-ASI data

The GS1662 is a high performance HD/SD capable transmitter. In order to optimize the output jitter performance across all operating conditions, input levels and overshoot at the parallel video data inputs of the device need to be controlled. In order to do this, source series termination resistors should be used to match the impedance of the PCB data trace line. IBIS models can be used to simulate the board effects and then optimize the output drive strength and the termination resistors to allow for the best transition (one that produces minimal overshoot). If this is not viable, Gennum recommends matching the source series resistance to the trace impedance, and then adjusting the output drive strength to the minimum value that will give zero errors.

The above also applies to the PCLK input line. HVF should also be well terminated, however due to the lower data rates and transition density, it is not as critical.

4.2.1 Parallel Input in SMPTE Mode

When the device is operating in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH), data must be presented to the input bus in either multiplexed or demultiplexed form, depending on the setting of the 20BIT/$\overline{\text{10BIT}}$ pin.

When operating in 20-bit mode (20BIT/$\overline{\text{10BIT}}$ = HIGH), the input data format must be word aligned, demultiplexed Luma and Chroma data (SD or HD).

When operating in 10-bit mode (20BIT/$\overline{\text{10BIT}}$ = LOW), the input data format must be multiplexed Luma (Y) and Chroma (C) data (SD, HD). C words precede Y words. In this mode, the data must be presented on the DIN[19:10] pins. The DIN[9:0] inputs are ignored.

4.2.1.1 Input Data Format in SDTI Mode

SDTI and HD-SDTI are a sub-set of SDI and HD-SDI formats. They may contain SDTI data on any line in the frame. Those lines which contain SDTI or HD-SDTI data are identified with an SDTI or HD-SDTI header packet in the HANC space.

The GS1662 does not differentiate between a signal carrying video and a signal carrying SDTI or HD-SDTI data in SD or HD formats. The user is responsible for ensuring that the headers and data are not corrupted.

4.2.2 Parallel Input in DVB-ASI Mode

The GS1662 is in DVB-ASI mode when the $\overline{\text{SMPTE\_BYPASS}}$ pin is set LOW, the DVB_ASI pin is set HIGH, and the RATE_SEL0 pin is set HIGH. In this mode, all SMPTE processing features are disabled.

When operating in DVB-ASI mode, the device must be set to 10-bit mode by setting the 20BIT/$\overline{\text{10BIT}}$ pin LOW. The device will accept 8-bit data words on DIN[17:10], where DIN17 = HIN is the most significant bit of the encoded transport stream data and DIN10 = AIN is the least significant bit. In addition, DIN19 and DIN18 will be configured as the DVB-ASI control signals INSSYNCIN and KIN respectively.

DIN19 = INSSYNCIN
DIN18 = KIN
DIN17~10 = HIN ~ AIN where AIN is the least significant bit of the transport stream data.

4.2.3 Parallel Input in Data-Through Mode

Data-Through mode is enabled when the $\overline{\text{SMPTE\_BYPASS}}$ pin and the DVB_ASI pin are LOW.

In this mode, data at the input bus is serialized without any encoding, scrambling or word alignment taking place.

The input data width is controlled by the setting of the 20BIT/$\overline{\text{10BIT}}$ pin as shown in Table 4-2 above.

NOTE: When in HD 10-bit mode, asserting the $\overline{\text{SMPTE\_BYPASS}}$ LOW to put the device in SMPTE-BYPASS mode will create video errors. If the user desires to use the device as a simple serializer in HD 10-bit mode, all video processing features may be disabled by setting the IOPROC_EN/$\overline{\text{DIS}}$ pin LOW.

4.2.4 Parallel Input Clock (PCLK)

The frequency of the PCLK input signal of the GS1662 is determined by the input data format and operating mode selection.

Table 4-3 below lists the input PCLK rates and input signal formats according to the external selection pins for the GS1662.

Table 4-3: GS1662 PCLK Input Rates

Input Data Format	Pin Settings				PCLK Rate
	20BIT/$\overline{\text{10BIT}}$	RATE_SEL	$\overline{\text{SMPTE\_BYPASS}}$	DVB-ASI	
20-bit demultiplexed HD format	HIGH	LOW	HIGH	X	74.25 or 74.25/1.001MHz
20-bit data input HD format	HIGH	LOW	LOW	LOW	74.25 or 74.25/1.001MHz

Table 4-3: GS1662 PCLK Input Rates (Continued)

Input Data Format	Pin Settings				PCLK Rate
	20BIT/$\overline{10BIT}$	RATE_SEL	$\overline{SMPTE\_BYPASS}$	DVB-ASI	
20-bit demultiplexed SD format	HIGH	HIGH	HIGH	LOW	13.5MHz
20-bit data input SD format	HIGH	HIGH	LOW	LOW	13.5MHz
10-bit multiplexed HD format	LOW	LOW	HIGH	LOW	148.5 or 148.5/1.001MHz
10-bit data input HD format	LOW	LOW	LOW	LOW	148.5 or 148.5/1.001MHz
10-bit multiplexed SD format	LOW	HIGH	HIGH	X	27MHz
10-bit data input SD format	LOW	HIGH	LOW	LOW	27MHz
10-bit ASI input SD format	LOW	HIGH	LOW	HIGH	27MHz

4.3 SMPTE Mode

The function of this block is to carry out data scrambling according to SMPTE 292M, and to carry out NRZ to NRZI encoding prior to presentation to the parallel to serial converter.

These functions are only enabled when the $\overline{SMPTE\_BYPASS}$ pin is HIGH.

In addition, the GS1662 requires the DVB_ASI pin to be set LOW to enable this feature.

4.3.1 H:V:F Timing

In SMPTE mode, the GS1662 can automatically detect the video standard and generate all internal timing signals. The total line length, active line length, total number of lines per field/frame and total active lines per field/frame are calculated for the received parallel video.

When DETECT_TRS is LOW, the video standard and timing signals are based on the externally supplied H_Blanking, V_Blanking, and F_Digital signals. These signals are supplied by the H/HSYNC, V/VSYNC and F/DE pins respectively. When DETECT_TRS is HIGH, the video standard timing signals will be extracted from the embedded TRS ID words in the parallel input data. Both 8-bit and 10-bit TRS code words will be identified by the device.

NOTE: I/O processing must be enabled for the device to remap 8-bit TRS words to the corresponding 10-bit value for transmission.

The GS1662 determines the video standard by timing the horizontal and vertical reference information supplied at the H/HSYNC, V/VSYNC, and F/DE input pins, or

contained in the TRS ID words of the received video data. Therefore, full synchronization to the received video standard requires at least one complete video frame.

Once synchronization has been achieved, the GS1662 will continue to monitor the received TRS timing or the supplied H, V, and F timing information to maintain synchronization. The GS1662 will lose all timing information immediately following loss of H, V and F.

The H signal timing should also be configured via the H_CONFIG bit of the internal IOPROC register as either active line based blanking or TRS based blanking.

Active line based blanking is enabled when the H_CONFIG bit is set LOW. In this mode, the H input should be HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words. This is the default H timing used by the device.

The timing of these signals is shown in Figure 4-2.

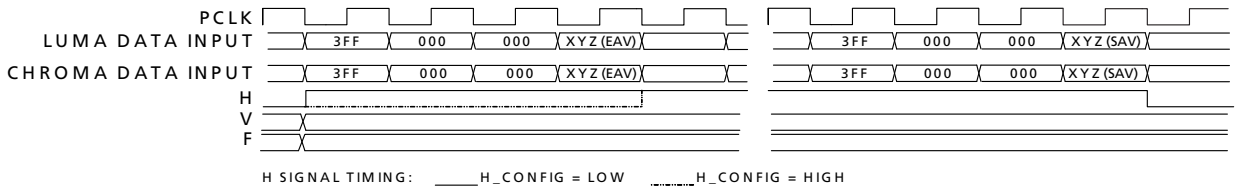


Figure 4-2: H:V:F Input Timing - HD 20-bit Input Mode

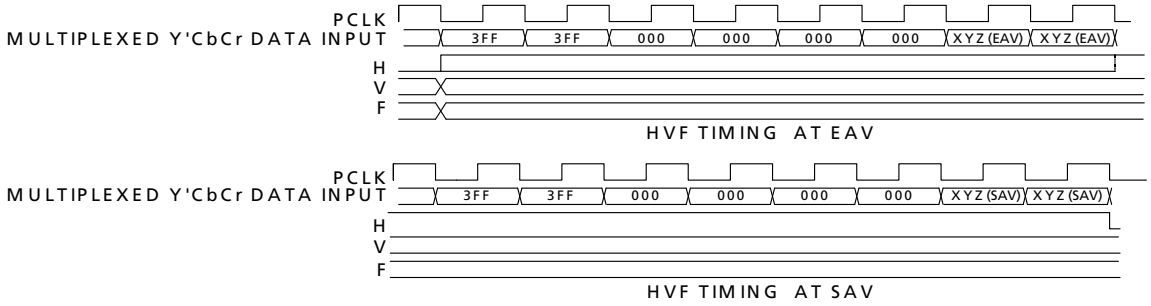


Figure 4-3: H:V:F Input Timing - HD 10-bit Input Mode

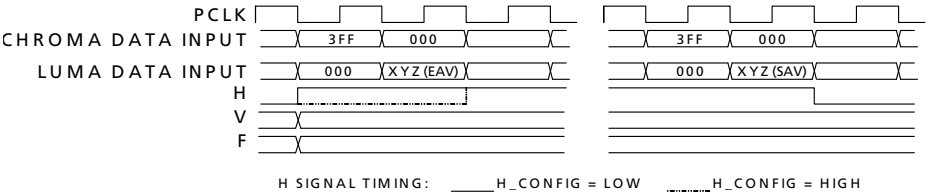


Figure 4-4: H:V:F Input Timing - SD 20-bit Mode

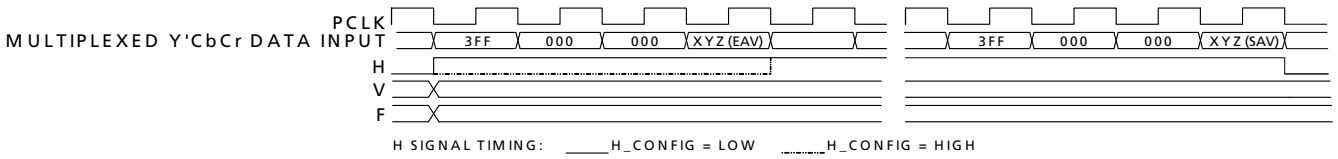


Figure 4-5: H:V:F Input Timing - SD 10-bit Mode

4.3.2 CEA 861 Timing

The GS1662 extracts timing information from externally provided HSYNC, VSYNC, and DE signals when CEA 861 timing mode is selected by setting DETECT_TRS = LOW and TIM_861 = HIGH.

Horizontal sync (H), Vertical sync (V), and Data Enable (DE) timing must be provided via the H/HSYNC, V/VSYNC and F/DE input pins. The host interface register bit H_CONFIG is ignored in CEA 861 input timing mode.

The GS1662 determines the EIA/CEA-861 standard and embeds EAV and SAV TRS words in the output serial video stream.

Video standard detection is not dependent on the HSYNC pulse width or the VSYNC pulse width and therefore the GS1662 tolerates non-standard pulse widths. In addition, the device can compensate for up to ±1 PCLK cycle of jitter on VSYNC with respect to HSYNC and sample VSYNC correctly.

NOTE 1: The period between the leading edge of the HSYNC pulse and the leading edge of Data Enable (DE) must follow the timing requirements described in the EIA/CEA-861 specification. The GS1662 embeds TRS words according to this timing relationship to maintain compatibility with the corresponding SMPTE standard.

NOTE 2: When CEA 861 standards 6 & 7 [720(1440)x480i] are presented to the GS1662, the device embeds TRS words corresponding to the timing defined in SMPTE 125M to maintain SMPTE compatibility.

CEA 861 standards 6 & 7 [720(1440)x480i] define the active area on lines 22 to 261 and 285 to 524 inclusive (240 active lines per field). SMPTE 125M defines the active area on lines 20 to 263 and 283 to 525 inclusive (244 lines on field 1, 243 lines on field 2).

Therefore, in the first field, the GS1662 adds two active lines above and two active lines below the original active image. In the second field, it adds two lines above and one line below the original active image.

The CEA861 Timing Formats are summarized in Table 4-4. and are shown in Figure 4-6 to Figure 4-14.

Table 4-4: CEA861 Timing Formats

Format	Parameters
4	H:V:DE Input Timing 1280 x 720p @ 59.94/60Hz
5	H:V:DE Input Timing 1920 x 1080i @ 59.94/60Hz
6&7	H:V:DE Input Timing 720 (1440) x 480i @ 59.94/60Hz
19	H:V:DE Input Timing 1280 x 720p @ 50Hz
20	H:V:DE Input Timing 1920 x 1080i @ 50Hz
21&22	H:V:DE Input Timing 720 (1440) x 576 @ 50Hz
32	H:V:DE Input Timing 1920 x 1080p @ 23.94/24Hz
33	H:V:DE Input Timing 1920 x 1080p @ 25Hz
34	H:V:DE Input Timing 1920 x 1080p @ 29.97/30Hz

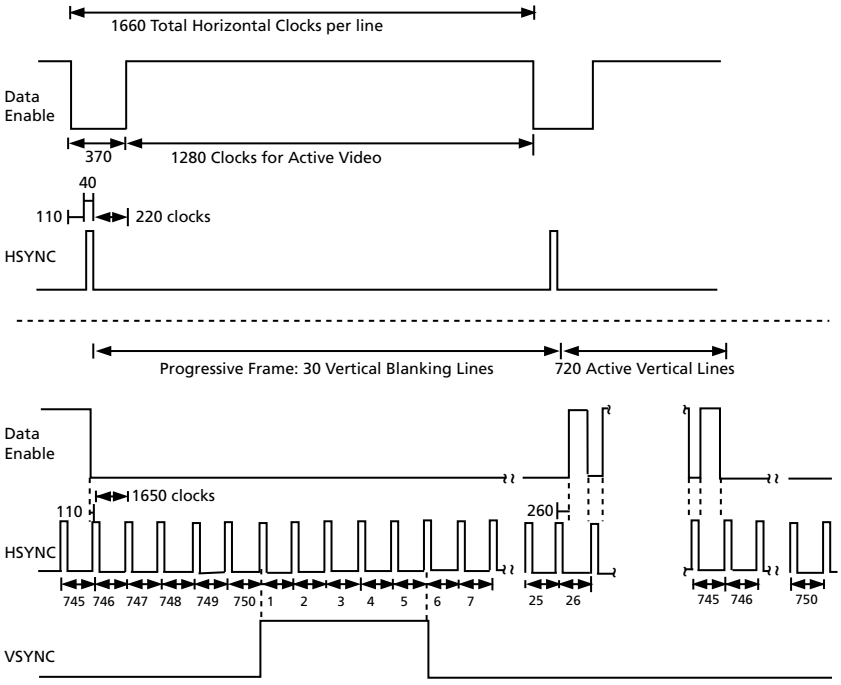


Figure 4-6: H:V:DE Input Timing 1280 x 720p @ 59.94/60 (Format 4)

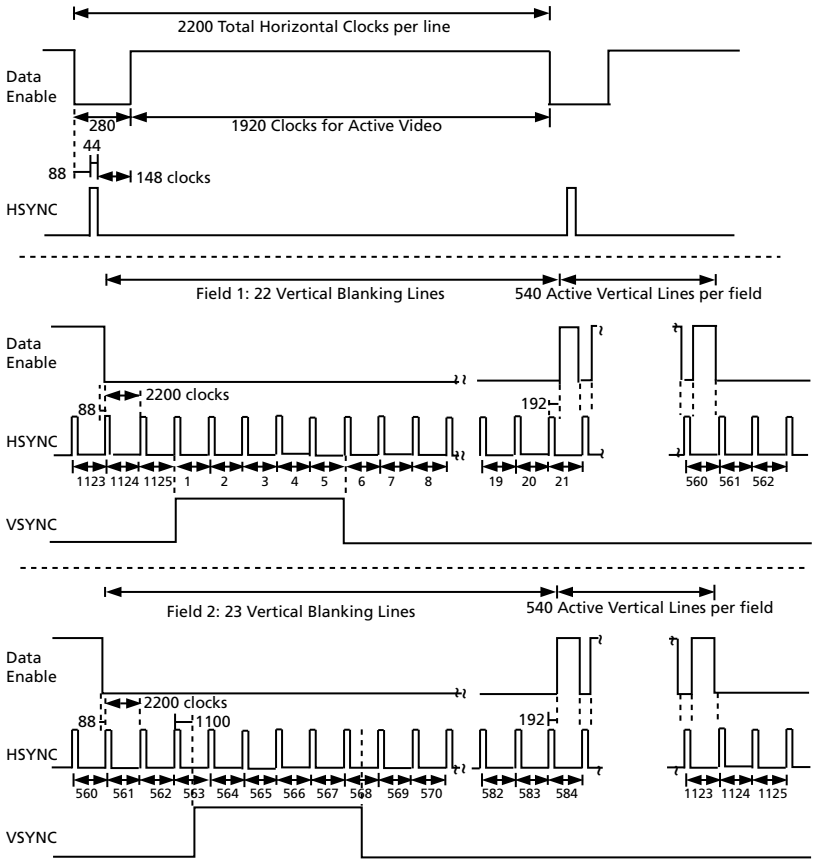


Figure 4-7: H:V:DE Input Timing 1920 x 1080i @ 59.94/60 (Format 5)

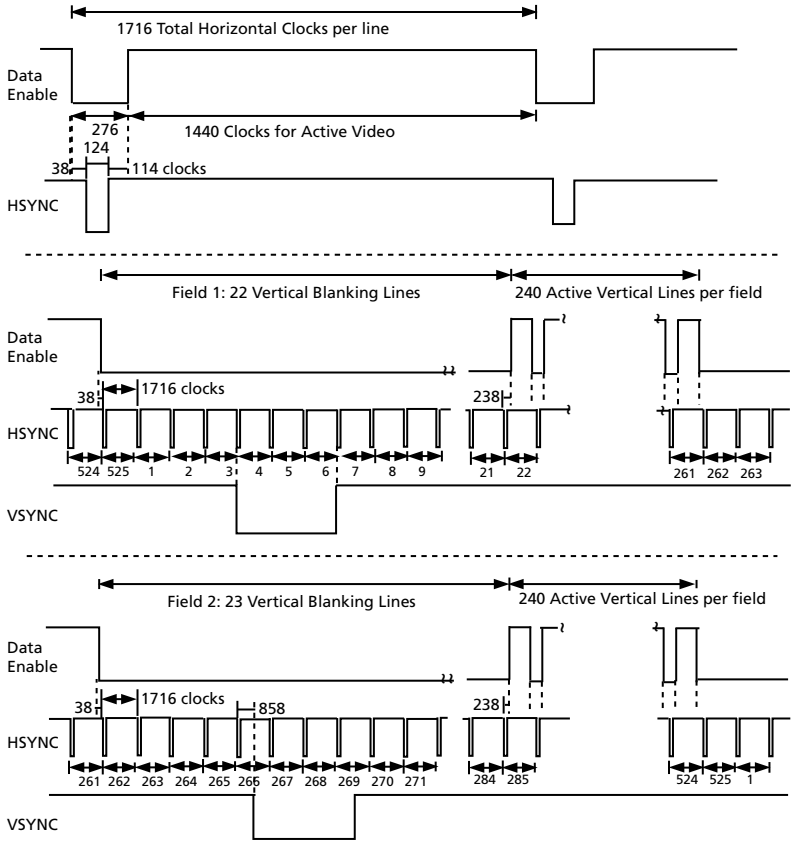


Figure 4-8: H:V:DE Input Timing 720 (1440) x 480i @ 59.94/60 (Format 6&7)

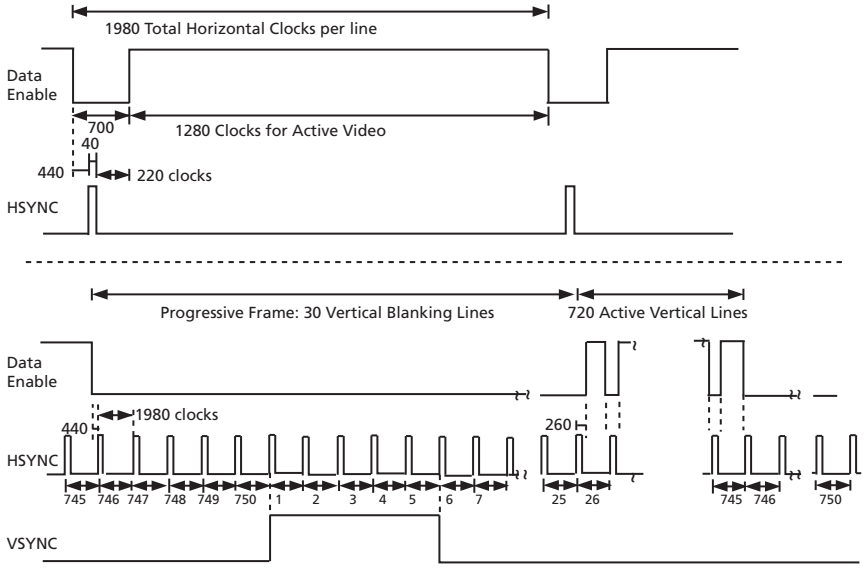


Figure 4-9: H:V:DE Input Timing 1280 x 720p @ 50 (Format 19)

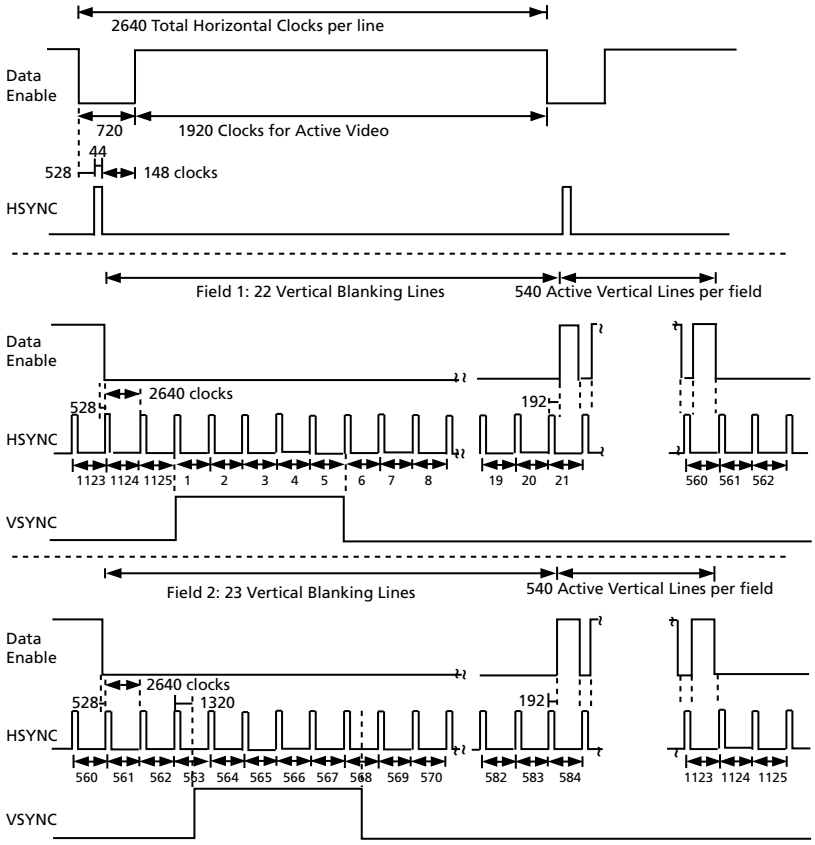


Figure 4-10: H:V:DE Input Timing 1920 x 1080i @ 50 (Format 20)

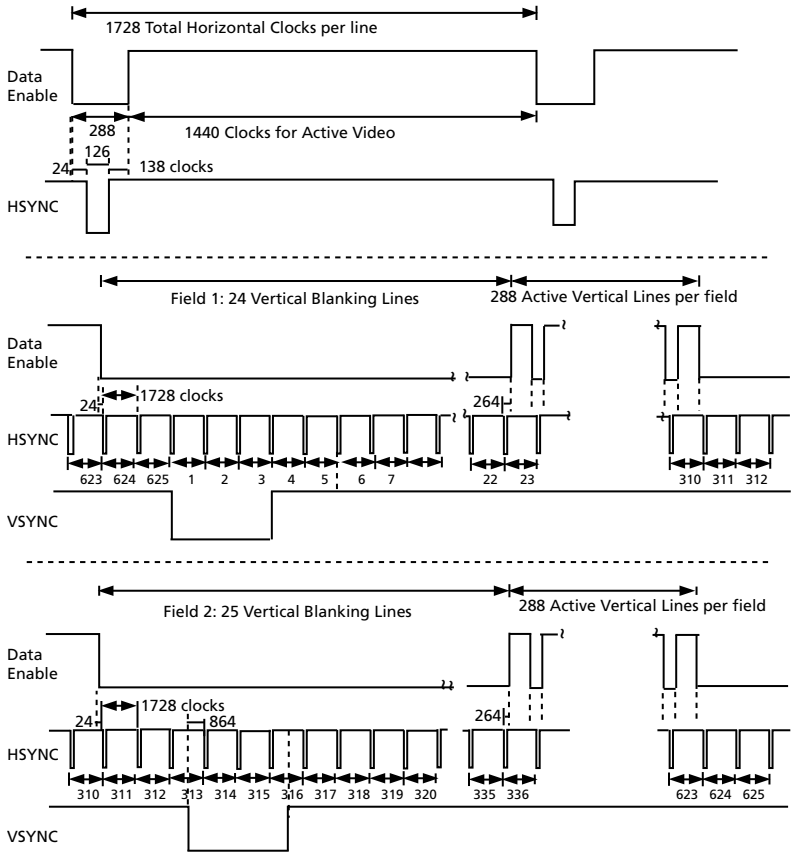


Figure 4-11: H:V:DE Input Timing 720 (1440) x 576 @ 50 (Format 21 & 22)

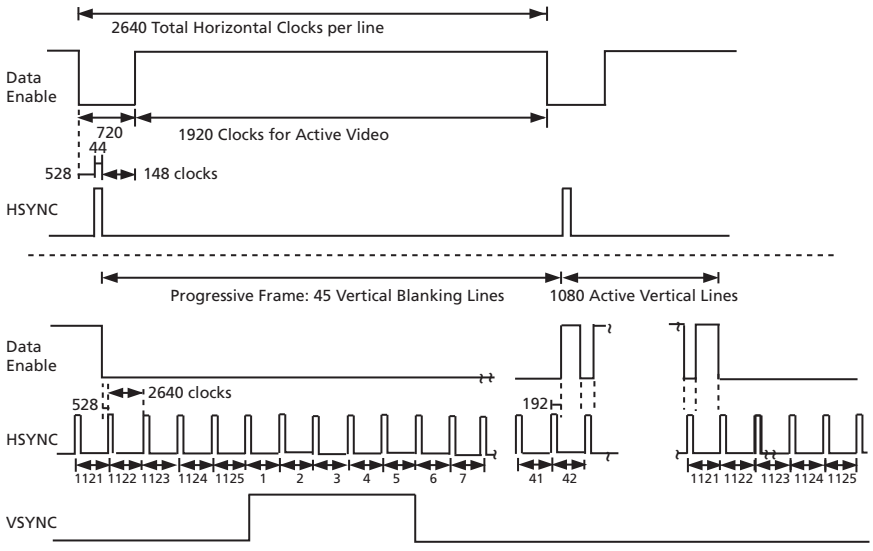


Figure 4-12: H:V:DE Input Timing 1920 x 1080p @ 23.94/24 (Format 32)

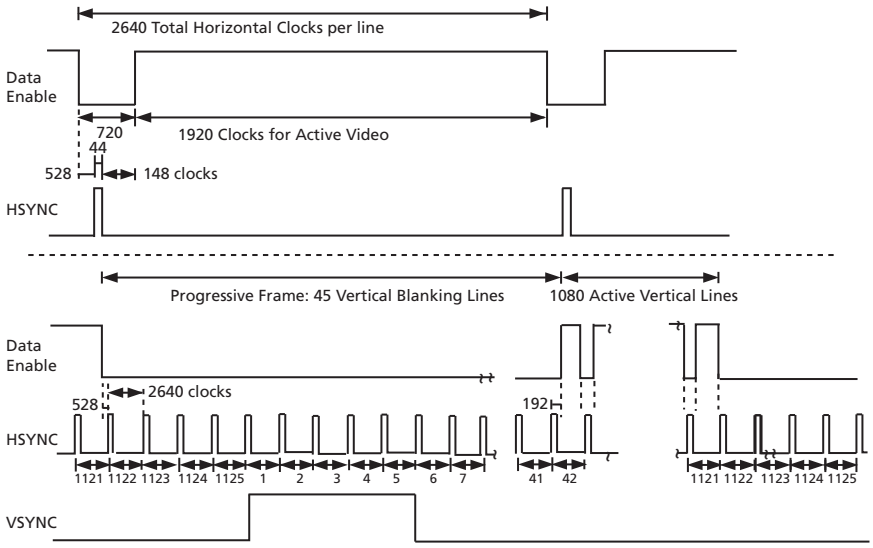


Figure 4-13: H:V:DE Input Timing 1920 x 1080p @ 25 (Format 33)

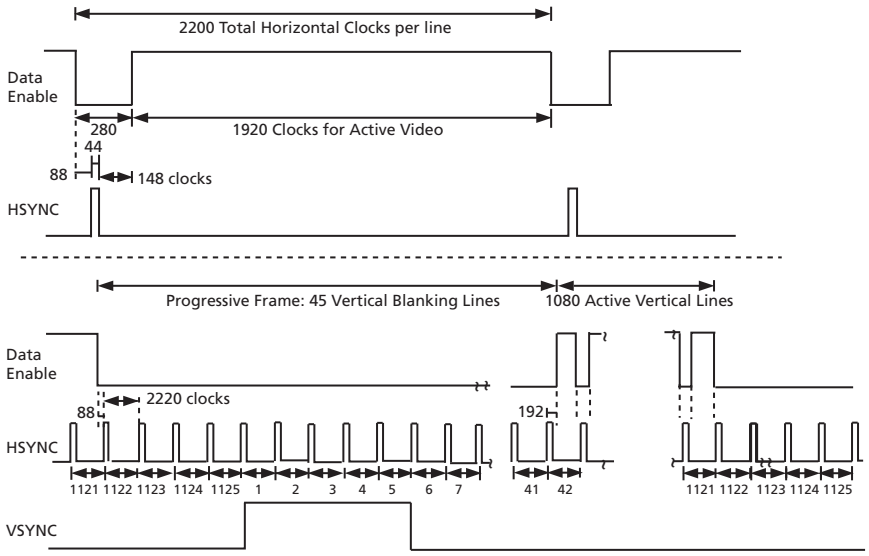


Figure 4-14: H:V:DE Input Timing 1920 x 1080p @ 29.97/30 (Format 34)

4.4 DVB-ASI Mode

When operating in DVB-ASI mode, all SMPTE processing features are disabled, and the device accepts 8-bit transport stream data and control signal inputs on the DIN[19:10] port.

This mode is only enabled when $\overline{\text{SMPTE\_BYPASS}}$ pin is LOW, DVB_ASI pin is HIGH and the RATE_SEL pin is HIGH.

The interface consists of eight data bits and two control signals, INSSYNCIN and KIN.

When INSSYNCIN is set HIGH, the GS1662 inserts K28.5 sync characters into the data stream. This function is used to assist system implementations where the GS1662 may be preceded by a data FIFO.

The FIFO can be fed data at a rate somewhat less than 27MHz. The 'FIFO empty' signal could be used to feed the INSSYNCIN pin, causing the GS1662 to pad the data up to the transmission rate of 27MHz.

When KIN is set HIGH the data input is interpreted as a special character (such as a K28.5 sync character), as defined by the DVB-ASI standard. When KIN is set LOW the input is interpreted as data.

After sync signal insertion, the GS1662 8b/10b encodes the data, generating a 10-bit data stream for the parallel to serial conversion and transmission process.

4.5 Data-Through Mode

The GS1662 may be configured to operate as a simple parallel-to-serial converter. In this mode, the device passes data to the serial output without performing any scrambling or encoding.

Data-through mode is enabled only when both the $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI pins are set LOW.

4.6 Standby Mode

The STANDBY pin reduces power to a minimum by disabling all circuits except for the register configuration. Upon removal of the signal to the STANDBY pin, the device returns to its previous operating condition within 1 second, without requiring input from the host interface.

In addition, the serial digital output signals becomes high-impedance when the device is powered-down.

4.7 ANC Data Insertion

Horizontal or vertical ancillary data words may be inserted on up to four different lines per video frame.

Up to 512 data words may be inserted per frame with all Data Words - including the ANC packet ADF, DBN, DCNT, DID, SDID and CSUM words - being provided by the user via host interface configuration.

The CSUM word is re-calculated and inserted by the ANC Data Checksum Calculation and Insertion function.

Note that any value may be used for the CSUM word, provided that it is outside the protected ranges from 000h to 003h and from 3FCh to 3FFh. If a CSUM value in either of these ranges is used, it will not be corrected by the device.

The GS1662 does not provide error checking or correction to the ANC data provided by user via the host interface. It is the responsibility of the user to ensure that all data provided for insertion is fully standard compliant.

In HD mode, ANC data packets are inserted into the Y or C video stream, as selected via the host interface. The default insertion will be in the Y stream. For Y or C, see Registers 026h, 028h, 02Ah and 02Ch.

In SD mode, the ANC data packets are inserted into the multiplexed CbYCr data stream.

ANC data insertion only takes place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and $\overline{\text{SMPTE\_BYPASS}}$ is HIGH.

In addition to this, the GS1662 requires the ANC_INS bit to be set LOW in the IOPROC register.

4.7.1 ANC Insertion Operating Modes

User selection of one of the two operating modes is provided through host interface configuration, using the ANC_INS_MODE register bit (see Table 4-16: Configuration and Status Registers).

The supported operating modes are Concatenated mode and Separate Line operating mode.

By default (at power up or after system reset), the Separate Line operating mode is enabled.

Ancillary data packets are programmed into the ANC_PACKET_BANK host register at addresses 040h to BFFh.

4.7.1.1 Separate Line Operating Mode

In Separate Line mode, it is possible to insert horizontal or vertical ancillary data on up to four lines per video frame. HANC or VANC can be specified, independently of each other, on a per-line basis. 025h FIRST_LINE_NUMBER, 027h SECOND_LINE_NUMBER, 029h THIRD_LINE_NUMBER and 02Bh FOURTH_LINE_NUMBER. For each of the four video lines, up to 128 8-bit HANC or VANC data words can be inserted. Separate Line mode is selected by setting the ANC_INS_MODE bit in the host interface LOW. By default, at power up, Separate Line mode is selected.

The lines on which ancillary data is to be inserted is programmed in the host register addresses 025h to 02Ch.

For HD formats, the stream into which the ancillary data is to be inserted (Luma or Chroma) is also programmed in these register addresses.

The non-zero video line numbers on which to insert the ancillary data, the ancillary data type (HANC or VANC), and the total number of words to insert per line must be provided via the host interface (see Section 4.12). At power up, or after system reset, all ancillary data insertion line numbers and total number of words default to zero.

If the total number of Data Words specified per line exceeds 128 only the first 128 Data Words will be inserted, the rest will be ignored.

The data words are programmed as two 8-bit values per address, starting at host interface address 040h in the ANC_PACKET_BANK register (see Table 4-16).

The device automatically converts the provided 8-bit Data Words into the 10-bit data, formatted according to SMPTE 291M prior to insertion.

4.7.1.2 Concatenated Operating Mode

In Concatenated mode, it is possible to insert up to 512 8-bit horizontal or vertical ancillary Data Words on one line per video frame. Concatenated Line mode can be selected by setting the ANC_INS_MODE bit in the host interface HIGH. By default, at power up, Separate Line mode is selected.

In Concatenated mode, only the FIRST_LINE registers of the host interface need to be programmed (addresses 025h and 026h). See Table 4-16.

The non-zero video line number on which to insert the ancillary data, the ancillary data type (HANC or VANC), and the total number of words to insert must be provided via the host interface. At power up, or after system reset, the ancillary data insertion line number and total number of words default to zero.

If the total number of data words specified exceeds 512 only the first 512 Data Words will be inserted, the rest will be ignored.

The data words are programmed as two 8-bit values per address, starting at host interface address 040h in the ANC_PACKET_BANK register. See Table 4-16.

The device automatically converts the provided 8-bit data words into the 10-bit data formatted according to SMPTE 291M prior to insertion.

4.7.2 HD ANC Insertion

When operating in HD mode (RATE_SEL = LOW), the GS1662 inserts VANC or HANC data packets into either the Y data stream or C data stream.

By default (at power up or after system reset), all ANC data insertion takes place in the Y data stream.

The user can select between Y or C data stream for insertion on a per line basis in Separate Line mode. The Y data stream is selected when the STREAM_TYPE_0 bit is LOW (default). The C data stream is selected when the STREAM_TYPE_0 bit is HIGH.

The user can select between Y or C data stream for insertion on a single line basis in Concatenated mode. The Y data stream is selected when the STREAM_TYPE_0 bit is LOW (default). The C data stream is selected when the STREAM_TYPE_0 bit is HIGH.

Horizontal Ancillary data (HANC), is inserted into the Y or C data stream on the video line(s) defined by the user.

Data insertion starts at the first available location in the HANC space, following any pre-existing arbitrary data packets. All Data Words identified by the user are inserted in a contiguous fashion starting at the first available data space.

HANC data insertion terminates when all Data Words identified by the user have been inserted; or by the start of the four word TRS SAV code, regardless of the number of Data Words actually inserted.

Vertical Ancillary data (VANC), is inserted into the Y or C data stream on the video line(s) defined by the user.

Data insertion starts at the first active pixel immediately following the last word of the TRS SAV code. All Data Words identified by the user are inserted in a contiguous fashion, starting at the first active pixel.

VANC data insertion terminates when all Data Words identified by the user have been inserted; or by the start of the four word TRS EAV code, regardless of the number of Data Words actually inserted.

The total number of Data Words to be inserted and the line number on which ANC data insertion takes place is provided by the user via the host interface as part of the configuration of the ANC data insertion function.

The user data for insertion is provided via host interface configuration. STREAM_TYPE_1 = address 02Dh, STREAM_TYPE_0 for the four lines of insertion is at addresses 026h (bit 14), 028h (bit 14), 02Ah (bit 14) and 02Ch (bit 14).

4.7.3 SD ANC Insertion

When operating in SD mode (RATE_SEL = HIGH), the GS1662 inserts VANC or HANC data packets into the multiplexed CbYCr data stream.

Horizontal Ancillary data (HANC), is inserted on the video line(s) defined by the user.

Data insertion starts at the first available location in the HANC space following any pre-existing arbitrary data packets. All Data Words identified by the user are inserted in a contiguous fashion, starting at the first available data space.

HANC data insertion terminates when all Data Words identified by the user have been inserted; or by the start of the four word TRS SAV code, regardless of the number of Data Words actually inserted.

For the case where HANC data insertion is required on the same line as the EDH packet, data insertion is terminated by the start of the EDH packet, regardless of the number of Data Words actually inserted.

Vertical Ancillary data (VANC), is inserted into the data stream on the video line(s) defined by the user.

Data insertion starts at the first active Cb pixel immediately following the last word of the TRS SAV code. All data words identified by the user are inserted in a contiguous fashion, starting at the first active pixel.

VANC data insertion terminates when all Data Words identified by the user have been inserted; or by the start of the four word TRS EAV code, regardless of the number of Data Words actually inserted.

The total number of data words to be inserted and the line number on which ANC data insertion takes place is provided by the user via the host interface as part of the configuration of the ANC data insertion function.

The user data for insertion is provided via host interface configuration. STREAM_TYPE_1 = address 02Dh, STREAM_TYPE_0 for the four lines of insertion is at addresses 026h (bit 14), 028h (bit 14), 02Ah (bit 14) and 02Ch (bit 14).

ANC data checksum insertion only takes place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH, the $\overline{\text{SMPTE\_BYPASS}}$ is HIGH and the ANC_CSUM_INS bit is set LOW in the IOPROC register.

4.8 Additional Processing Functions

The GS1662 contains a number of signal processing features. These features are only enabled in SMPTE mode of operation ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH), and when I/O processing is enabled (IOPROC_EN/$\overline{\text{DIS}}$ = HIGH).

Signal processing features include:

- TRS generation and insertion
- Line number calculation and insertion
- Line based CRC calculation and insertion
- Illegal code re-mapping
- SMPTE 352M payload identifier packet insertion
- ANC checksum calculation and correction
- EDH generation and insertion

To enable these features in the GS1662, the $\overline{\text{SMPTE\_BYPASS}}$ pin must be HIGH, the IOPROC_EN/$\overline{\text{DIS}}$ pin must be HIGH and the individual feature must be enabled via bits set in the IOPROC register of the host interface. By default, all of the processing features are enabled.

4.8.1 Video Format Detection

By using the timing parameters extracted from the received TRS signals, or the supplied external timing signals, the GS1662 calculates the video format.

The total samples per line, active samples per line, total lines per field/frame, and active lines per field/frame are measured and reported to the user via the four RASTER_STRUC_X registers in the host interface.

These line and sample count registers are updated once per frame at the end of line 12.

The RASTER_STRUC_X registers also contain two status bits: STD_LOCK and INT/$\overline{\text{PROG}}$.

The STD_LOCK bit is set HIGH whenever the automatic video format detection circuit has achieved full synchronization.

The INT/$\overline{\text{PROG}}$ bit is set LOW if the detected video standard is Progressive, and is set HIGH if the detected video standard is Interlaced.

The Gennum video standard code (VD_STD), as used in the GS1582 and GS1572, is included in Table 4-5 for reference purposes.

NOTE: If proper SMPTE video is applied and then removed from the input, the device does not flag that the H_LOCK, V_LOCK, VD_SDT etc. has changed (been lost). This is the case for either TRS detect or HVF modes. This problem occurs only when the video data is removed, but not the PCLK. Usually, when a video signal is removed, it includes the clock, the video data, as well as the H, V, F as a whole. So the scenario is not likely to occur, but the user should be aware of this issue.

Table 4-5: Supported Video Standards

SMPTE STANDARD	ACTIVE VIDEO AREA	LENGTH OF HANC	LENGTH OF ACTIVE VIDEO	TOTAL SAMPLES	SMPTE 352M LINES	Gennum VD_STD [4:0]	RATE_ SEL1
428.1M	2048x1080/24 (1:1)	690	2048	2750	10	1Ch	1
428.1M	2048x1080/25 (1:1)	580	2048	2640	10	1Ch	1
260M (HD)	1920x1035/60 (2:1)	268	1920	2200	10, 572	15h	0
295M (HD)	1920x1080/50 (2:1)	444	1920	2376	10, 572	14h	0
274M (HD)	1920x1080/60 (2:1) or 1920x1080/30 (PsF)	268	1920	2200	10, 572	0Ah	0
	1920x1080/50 (2:1) or 1920x1080/25 (PsF)	708	1920	2640	10, 572	0Ch	0
	1920x1080/30 (1:1)	268	1920	2200	10 (18)[1]	0Bh	0
	1920x1080/25 (1:1)	708	1920	2640	10 (18)[1]	0Dh	0
	1920x1080/24 (1:1)	818	1920	2750	10 (18)[1]	10h	0
	1920x1080/24 (PsF)	818	1920	2750	10, 572	11h	0
	1920x1080/25 (1:1) – EM	324	2304	2640	10 (18)[1]	0Eh	0
	1920x1080/25 (PsF) – EM	324	2304	2640	10, 572	0Fh	0
	1920x1080/24 (1:1) – EM	338	2400	2750	10 (18)[1]	12h	0
	1920x1080/24 (PsF) – EM	338	2400	2750	10, 572	13h	0

Table 4-5: Supported Video Standards (Continued)

SMPTE STANDARD	ACTIVE VIDEO AREA	LENGTH OF HANC	LENGTH OF ACTIVE VIDEO	TOTAL SAMPLES	SMPTE 352M LINES	Gennum VD_STD [4:0]	RATE_ SEL1
296M (HD)	1280x720/30 (1:1)	2008	1280	3300	10 (13)[1]	02h	0
	1280x720/30 (1:1) – EM	408	2880	3300	10 (13)[1]	03h	0
	1280x720/50 (1:1)	688	1280	1980	10 (13)[1]	04h	0
	1280x720/50 (1:1) – EM	240	1728	1980	10 (13)[1]	05h	0
	1280x720/25 (1:1)	2668	1280	3960	10 (13)[1]	06h	0
	1280x720/25 (1:1) – EM	492	3456	3960	10 (13)[1]	07h	0
	1280x720/24 (1:1)	2833	1280	4125	10 (13)[1]	08h	0
	1280x720/24 (1:1) – EM	513	3600	4125	10 (13)[1]	09h	0
	1280x720/60 (1:1)	358	1280	1650	10 (13)[1]	00h	0
	1280x720/60 (1:1) – EM	198	1440	1650	10 (13)[1]	01h	0
125M (SD)	1440x487/60 (2:1) (Or dual link progressive)	280	1440	1716	13, 276	16h	X
	1440x507/60 (2:1)	280	1440	1716	13, 276	17h	X
	525-line 487 generic	–	–	1716	13, 276	19h	X
	525-line 507 generic	–	–	1716	13, 276	1Bh	X
ITU-R BT.656 (SD)	1440x576/50 (2:1) (Or dual link progressive)	280	1440	1728	9, 322	18h	X
	625-line generic (EM)	–	–	1728	9, 322	1Ah	X
Unknown HD	RATE_SEL = 0	–	–	–	–	1Dh	
Unknown SD	RATE_SEL = 1	–	–	–	–	1Eh	X

NOTE 1: The part may provide full or limited functionality with standards that are not included in this table. Please consult a Gennum technical representative.

By default (at power up or after system reset), the four RASTER_STRUC_X, STD_LOCK and INT/$\overline{\text{PROG}}$ registers are set to zero. These registers are also cleared when the $\overline{\text{SMPTE\_BYPASS}}$ pin is LOW, or the LOCKED pin is LOW.

NOTE 2: The Line Numbers in brackets refer to Version zero SMPTE 352M packet locations, if they are different from the Version one locations.

4.8.2 ANC Data Blanking

The GS1662 can blank the video input data during the H and V blanking periods. This function will be enabled by setting the $\overline{\text{ANC\_BLANK}}$ pin LOW.

This function is only available when the device is operating in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH).

In this mode, input video data in the horizontal and vertical blanking periods will be replaced by SMPTE compliant blanking values.

The blanking function will operate only on the video input signal and will remove all ancillary data already embedded in the input video stream.

In SD mode, SAV and EAV code words already embedded in the input video stream will be protected and will not be blanked.

In HD mode, SAV and EAV code words, line numbers and line based CRC's already embedded in the input video stream will be protected and will not be blanked.

The above two statements are really implementation specific, and are provided only to ensure that the “Detect TRS” function for timing generation is supported by the device, even when the blanking function is enabled.

From a system perspective, use of the input blanking function is not recommended unless TRS, line number and CRC generation and insertion functions are enabled.

The active image area will not be blanked.

The input blanking function will not blank any of the ancillary data, TRS words, line numbers, CRC's, EDH or SMPTE 352M payload identifiers inserted by the device itself.

4.8.3 ANC Data Checksum Calculation and Insertion

The GS1662 calculates checksums for all detected ancillary data packets presented to the device.

ANC data checksum insertion only takes place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH, the $\overline{\text{SMPTE\_BYPASS}}$ is HIGH and the ANC_CSUM_INS bit is set LOW in the IOPROC register.

NOTE: The device will correct any CSUM value outside the protected ranges from 000h to 003h and from 3FCh to 3FFh. If a CSUM value in either of these ranges is presented to the device, it will not be corrected.

4.8.4 TRS Generation and Insertion

The GS1662 is capable of generating and inserting TRS codes.

TRS word generation and insertion are performed in accordance with the timing parameters generated by the timing circuits, which is locked to the externally provided H:V:F or CEA-861 signals, or the TRS signals embedded in the input data stream. The GS1662 will overwrite the TRS signals if they're already embedded.

10-bit TRS code words are inserted at all times.

The insertion of TRS ID words only take place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and the $\overline{\text{SMPTE\_BYPASS}}$ pin is HIGH.

In addition to this, the GS1662 requires the TRS_INS bit to be set LOW in the IOPROC register.

If the TIM_861 pin is HIGH, then the timing circuits are locked to CEA-861 timing.

4.8.5 HD Line Number Calculation and Insertion

The GS1662 is capable of line number generation and insertion, in accordance with the relevant HD video standard, as determined by the automatic video standard detector. Line numbers are inserted into both the Y and C channels.

NOTE: Line number generation and insertion only occurs in HD mode (RATE_SEL = LOW).

The insertion of line numbers only take place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and $\overline{\text{SMPTE\_BYPASS}}$ pin is HIGH.

In addition to this, the GS1662 requires the LNUM_INS bit to be set LOW in the IOPROC register.

4.8.6 Illegal Code Re-Mapping

The GS1662 detects and corrects illegal code words within the active picture area.

All codes within the active picture (outside the horizontal and vertical blanking periods), between the values of 3FCh and 3FFh are re-mapped to 3FBh. All codes within the active picture area between the values of 000h and 003h are remapped to 004h.

8-bit TRS code words and ancillary data preambles are also re-mapped to 10-bit values.

The illegal code re-mapping will only take place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and $\overline{\text{SMPTE\_BYPASS}}$ is HIGH.

In addition to this, the GS1662 requires the ILLEGAL_REMAP bit to be set LOW in the IOPROC register.

4.8.7 SMPTE 352M Payload Identifier Packet Insertion

When enabled by the 352M_INS bit in the IOPROC register, new SMPTE 352M payload identifier packets are inserted into the data stream. These packets are supplied by the user via the host interface. Setting the 352M_INS bit LOW enables this insertion.

The device will automatically calculate the checksum and generate Version One compliant 352M ancillary data preambles: DID, SDID, DBN, DC.

The SMPTE 352M packet is inserted into the data stream according to the line number and sample position rules defined in the 2002 standard.

For HDTV video systems the SMPTE 352M packet is placed in the Y channel only.

By default (at power up or after system reset), the four VIDEO_FORMAT_IN_DS1 registers and the four VIDEO_FORMAT_OUT_DS1 registers are set to zero.

4.8.8 Line Based CRC Generation and Insertion (HD)

When operating in HD mode (RATE_SEL pin = LOW), the GS1662 generates and inserts line based CRC words into both the Y and C channels of the data stream.

The line based CRC insertion only takes place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and $\overline{\text{SMPTE\_BYPASS}}$ is HIGH.

In addition to this, the GS1662 requires the CRC_INS bit to be set LOW in the IOPROC register.

4.8.9 EDH Generation and Insertion

When operating in SD mode, the GS1662 generates and inserts EDH packets into the data stream.

The EDH packet generation and insertion only takes place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH, $\overline{\text{SMPTE\_BYPASS}}$ pin is HIGH, the RATE_SEL pin is HIGH and the EDH_CRC_INS bit is set LOW in the IOPROC register.

Calculation of both Full Field (FF) and Active Picture (AP) CRCs is carried out by the device.

EDH error flags EDH, EDA, IDH, IDA and UES for ancillary data, full field and active picture are also inserted.

- When the EDH_CRC_UPDATE bit of the host interface is set LOW, these flags are sourced from the ANC_EDH_FLAG, FF_EDH_FLAG and AP_EDH_FLAG registers of the device, where they are programmed by the application layer
- When the EDH_CRC_UPDATE bit of the host interface is set HIGH, incoming EDH flags are preserved and inserted in the outgoing EDH packets. In this mode the ANC_EDH_FLAG, FF_EDH_FLAG and AP_EDH_FLAG registers contain the incoming EDH flags, and will be read only

The GS1662 generates all of the required EDH packet data including all ancillary data preambles: DID, DBN, DC, reserved code words and checksum.

The prepared EDH packet is inserted at the appropriate line of the video stream (in accordance with RP165). The start pixel position of the inserted packet is based on the SAV position of that line, such that the last byte of the EDH packet (the checksum) is placed in the sample immediately preceding the start of the SAV TRS word.

NOTE 1: When the EDH_CRC_UPDATE bit of the host interface is set LOW, it is the responsibility of the application interface to ensure that the EDH flag registers are updated regularly (once per field).

NOTE 2: It is also the responsibility of the application interface to ensure that there is sufficient space in the horizontal blanking interval for the EDH packet to be inserted.

4.8.10 Processing Feature Disable

The GS1662 contains an IOPROC register. This register contains one bit for each processing feature, allowing the user to enable/disable each process individually.

By default (at power up or after system reset), all of the IOPROC register bits are LOW.

To disable an individual processing feature, the application interface must set the corresponding bit HIGH in the IOPROC register. To enable these features, the IOPROC_EN/$\overline{\text{DIS}}$ pin must be HIGH, and the individual feature must be enabled by setting bits LOW in the IOPROC register of the host interface.

The I/O processing functions supported by the GS1662 are shown in Table 4-6 below.

Table 4-6: IOPROC Register Bits

I/O Processing Feature	IOPROC Register Bit
TRS insertion	TRS_INS (000h Bit 0)
Y and C line number insertion	LNUM_INS (000h Bit 1)
Y and C line based CRC insertion	CRC_INS (000h Bit 2)
Ancillary data checksum correction	ANC_CSUM_INS (000h Bit 3)
EDH CRC error calculation and insertion	EDH_ CRC_INS (000h Bit 4)
Illegal word re-mapping	ILLEGAL_WORD_REMAP (000h Bit 5)
SMPTE 352M packet insertion	SMPTE_352M_INS (000h Bit 6)
Ancillary data insertion	ANC_INS (000h Bit 11)

4.9 Serial Digital Output

The GS1662 has a single, low-impedance current mode differential output driver, capable of driving at least 800mV into a 75Ω single-ended load.

The output signal amplitude, or swing, will be user-configurable using an external resistor on the RSET pin.

The serial digital output data rate supports SMPTE 292 and SMPTE 259M-C operation. This is summarized in Table 4-7:

Table 4-7: Serial Digital Output - Serial Output Data Rate

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Serial Output Data Rate	BRSDO	SMPTE 292 signal	–	1.485, 1.485/1.001	–	Gb/s
		SMPTE 259M-C signal	–	270	–	Mb/s
		DVB-ASI signal	–	270	–	Mb/s

The SDO and $\overline{\text{SDO}}$ pins of the device provide the serial digital output.

Compliance with all requirements defined in Section 4.9.1 through Section 4.9.4 is guaranteed when measured across a 75Ω terminated load at the output of 1m of Belden 1694A cable, including the effects of the Gennum recommended ORL matching network, BNC and coaxial cable connection, except where otherwise stated.

Figure 4-15 illustrates this requirement, which is in accordance with the measurement methodology defined in SMPTE 292 and SMPTE 259M.

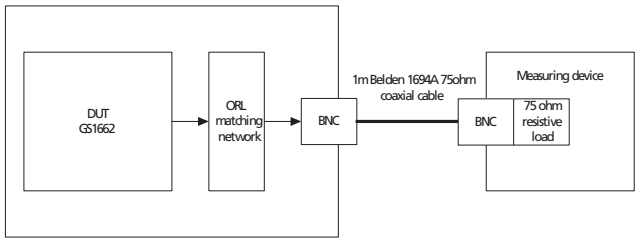


Figure 4-15: ORL Matching Network, BNC and Coaxial Cable Connection

4.9.1 Output Signal Interface Levels

The Serial Digital Output signals (SDO and $\overline{\text{SDO}}$ pins), of the device meet the amplitude requirements as defined in SMPTE 292 for an unbalanced generator (single-ended).

The signal amplitude is controlled to better than +/-7% of the nominal level defined in SMPTE 292, when an external 750Ω 1% resistor is connected between the RSET pin of the device and VCC.

The output signal amplitude can be reduced to less than 1/10th of the nominal amplitude, defined above, by increasing the value of the resistor connected between the RSET pin of the device and VCC.

These requirements are met across all ambient temperature and power supply operating conditions described in the Electrical Characteristics on page 16.

The output amplitude of the GS1662 can be adjusted by changing the value of the RSET resistor as shown in Table 4-8. For a 800mVp-p output a value of 750Ω is required. A ±1% SMT resistor should be used.

The RSET resistor is part of the high speed output circuit of the GS1662. The resistor should be placed as close as possible to the RSET pin. In addition, an anti-pad should be used underneath the resistor.

Table 4-8: R_{SET} Resistor Value vs. Output Swing

R_{SET} Resistor Values (Ω)	Output Swing (mV_{p-p})
995	608
824	734
750	800
680	884

4.9.2 Overshoot/Undershoot

The serial digital output signal overshoot and undershoot is controlled to be less that 7% of the output signal amplitude, when operating as an unbalanced generator (single-ended).

This requirement is met for nominal signal amplitudes as defined by SMPTE 292.

This requirement is met regardless of the output slew rate setting of the device.

This requirement is met across all ambient temperature and power supply operating conditions described in the Electrical Characteristics on page 16.

This requirement is summarized in Table 4-9:

Table 4-9: Serial Digital Output - Overshoot/Undershoot

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Serial output overshoot /undershoot	–	–	–	0	7	%

4.9.3 Slew Rate Selection

The GS1662 supports two user-selectable output slew rates.

Control of the slew rate is determined by the setting of the RATE_SEL input pin.

When this pin is set HIGH, the output slew rate matches the requirements as defined by the SMPTE 259M-C standard.

When this pin is set LOW, the output slew rate is better than the requirements as defined by the SMPTE 292 standard.

These requirements is met across all ambient temperature and power supply operating conditions described in the Electrical Characteristics on page 16.

This requirement is summarized in Table 4-10:

Table 4-10: Serial Digital Output - Rise/Fall Time

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Serial Output Rise/Fall Time 20% ~ 80%	SDO_{TR}	SMPTE 292 signal	–	–	135	ps
		SMPTE 259M-C signal	400	–	800	ps

4.9.4 Serial Digital Output Mute

When the SDO_EN/$\overline{DIS}$ pin is LOW, the serial digital output signals of the device become high-impedance, reducing system power.

The serial digital output is also placed in the high-impedance state when the LOCKED pin is LOW, or when the STANDBY pin is HIGH.

4.10 Serial Clock PLL

An internal VCO provides the transmission clock rates for the GS1662.

The power supply to the VCO is provided to the VCO_VDD/VCO_GND pins of the device.

This VCO is locked to the input PCLK via an on-chip PLL and Charge Pump.

Internal division ratios for the PCLK are determined by the setting of the RATE_SEL pin and the 20BIT/$\overline{10BIT}$ pin as shown in Table 4-11:

Table 4-11: PCLK and Serial Digital Clock Rates

External Pin Setting		Supplied PCLK Rate	Serial Digital Output Rate
RATE_SEL	20BIT/$\overline{10BIT}$		
LOW	HIGH	74.25 or 74.25/1.001MHz	1.485 or 1.485/1.001Gb/s
LOW	LOW	148.5 or 148.5/1.001MHz	1.485 or 1.485/1.001Gb/s
HIGH	HIGH	13.5MHz	270Mb/s
HIGH	LOW	27MHz	270Mb/s

As well as generating the serial digital output clock signals, the PLL is also responsible for generating all internal clock signals required by the device.

4.10.1 PLL Bandwidth

Table 4-12 shows the GS1662 PLL loop bandwidth variations. PLL bandwidth is a function of the external loop filter resistor and the charge pump current. We recommend using a 200Ω loop filter resistor, however, this value can be varied from 100Ω to 380Ω, depending on application. Values other than 200Ω are not guaranteed. As the resistor is changed, the bandwidth will scale proportionately (for example, a change from a 200Ω to 300Ω resistor will cause a 50% increase in bandwidth). The charge pump current is preset to 100µA and should not be changed. The external loop filter capacitor does not affect the PLL loop bandwidth. The external loop filter capacitor affects PLL loop settling time, phase margin and noise. It is selectable from 1µF to 33µF. However, it should be kept at 10µF for optimal performance. A smaller capacitor results in shorter lock time but less stability. A larger capacitor results in longer lock time but more stability. Narrower loop bandwidths require a larger capacitor to be stable. In other words, a small loop filter resistor requires a larger loop capacitor.

Table 4-12: GS1662 PLL Bandwidth

Mode	PCLK Frequency (MHz)	Filter Resistor (Ω)	Charge Pump Current (μA)	Bandwidth (kHz)
SD	13.50	200	100	4.78
SD	27.00	200	100	9.57
HD	74.25	200	100	26.32
HD	148.50	200	100	52.63

4.10.2 Lock Detect

The Lock Detect block controls the serial digital output signal and indicates to the application layer the lock status of the device.

The LOCKED output pin is provided to indicate the device operating status.

The LOCKED output signal is set HIGH by the lock detect block under the following conditions (see Table 4-13):

Table 4-13: GS1662 Lock Detect Indication

$\overline{\text{RESET}}$	PLL Lock	$\overline{\text{SMPTE\_BYPASS}}$	DVB_ASI	RATE_SEL
HIGH	HIGH	HIGH	LOW	X
HIGH	HIGH	LOW	HIGH	HIGH
HIGH	HIGH	LOW	LOW	X

Any other combination of signal states not included in the above table results in the LOCKED pin being LOW.

NOTE: When the LOCKED pin is LOW, the serial digital output is in the muted state.

4.11 GSPI Host Interface

The GSPI, or Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the application layer to access additional status information through configuration registers in the GS1662.

The GSPI comprises a Serial Data Input signal (SDIN), Serial Data Output signal (SDOUT), an active low Chip Select ($\overline{\text{CS}}$) and a Burst Clock (SCLK).

Because these pins can be shared with the JTAG interface port for compatibility with the GS1582, an additional control signal pin JTAG/$\overline{\text{HOST}}$ is provided.

When JTAG/$\overline{\text{HOST}}$ is LOW, the GSPI interface is enabled. When JTAG/$\overline{\text{HOST}}$ is HIGH, the JTAG interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ signals are provided by the application interface. The SDOUT pin is a non-clocked loop-through of SDIN, and may be connected to the SDIN of another device, allowing multiple devices to be connected to the GSPI chain. The interface is illustrated in Figure 4-16 below.

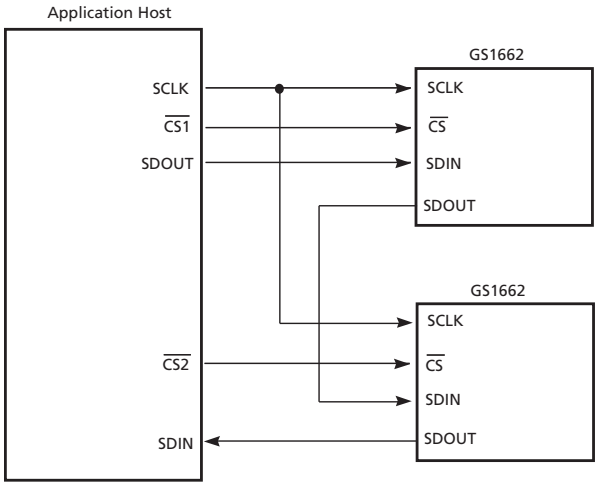


Figure 4-16: GSPI Application Interface Connection

All read or write access to the GS1662 is initiated and terminated by the application host processor. Each access always begins with a Command/Address Word followed by a data read to or written from the GS1662.

4.11.1 Command Word Description

The Command Word consists of a 16-bit word transmitted MSB first and contains a read/write bit, an Auto-Increment bit and a 12-bit address. Figure 4-17 shows the command word format and bit configurations.

Command Words are clocked into the GS1662 on the rising edge of the Serial Clock SCLK, which operates in a burst fashion.

When the Auto-Increment bit is set LOW, each Command Word must be followed by only one Data Word to ensure proper operation. If the Auto-Increment bit is set HIGH, the following Data Word will be written into the address specified in the Command Word, and subsequent data words will be written into incremental addresses from the previous Data Word. This facilitates multiple address writes without sending a Command Word for each Data Word.

NOTE: All registers can be written to through single address access or through the Auto-increment feature. However, the LSB of the video registers cannot be read through single address read-back. Single address read-back will return a zero value for the LSB. If auto-increment is used to read back the values from at least two registers, the LSB value read will always be correct. Therefore, for register read-back, it is recommended that auto-increment be used and that at least two registers be read back at a time.

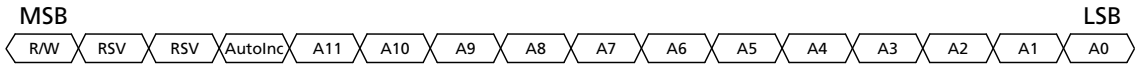


Figure 4-17: Command Word Format

4.11.2 Data Read or Write Access

Serial data is transmitted or received MSB first synchronous with the rising edge of the Serial Clock, SCLK. The Chip Select ($\overline{CS}$) signal must be active LOW a minimum of 1.5ns (t0 in Figure 4-19) before the first clock edge to ensure proper operation.

During a Read sequence (Command Word R/W bit set HIGH), a wait state of 148ns (4 x 1/fPCLK, t5 in Figure 4-19) is required between writing the Command Word and reading the following Data Word. The read bits are clocked out on the negative edges of SCLK.

NOTE 1: Where several devices are connected to the GSPI chain, only one $\overline{CS}$_TMS may be asserted during a read sequence.

During a Write sequence (Command Word R/W bit set LOW), a wait state of 37ns (1 x 1/fPCLK, t4 in Figure 4-19) is required between the Command Word and the following Data Word. This wait state must also be maintained between successive Command Word/Data Word write sequences. When Auto-increment mode is selected (AutoInc = 1), the wait state must be maintained between successive Data Words after the initial Command Word/Data Word sequence.

During the write sequence, all command and following Data Words input at the SDIN pin are output at the SDOUT pin as is.

When several devices are connected to the GSPI chain, data can be written simultaneously to all the devices which have $\overline{CS}$ set LOW.

NOTE 2: If the application interface performs a Read or Write access after power-up, prior to the application of a valid serial video input signal, the SCLK frequency must not exceed 10MHz.

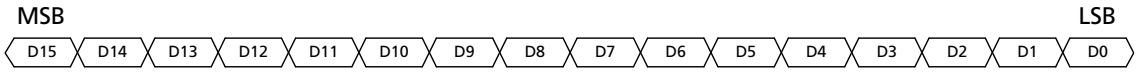


Figure 4-18: Data Word Format

4.11.3 GSPI Timing

Write and Read Mode timing for the GSPI interface is as shown in the following diagrams:

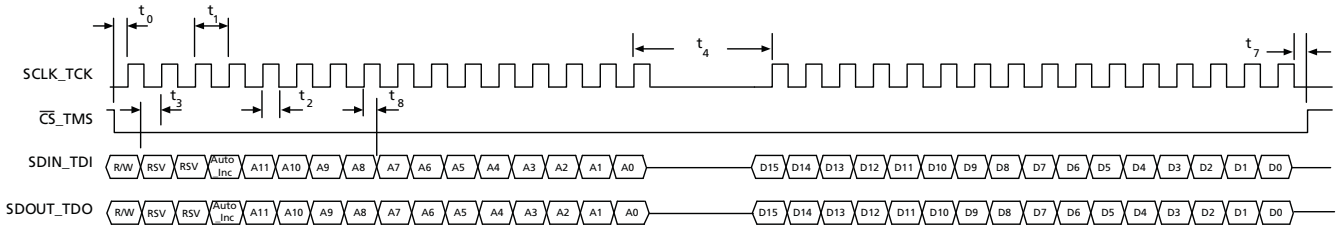


Figure 4-19: Write Mode

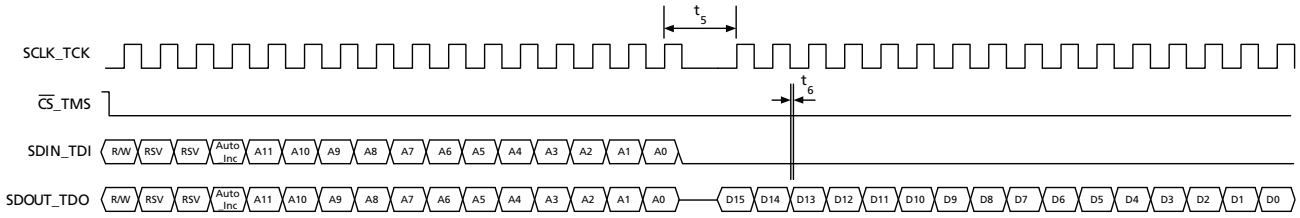


Figure 4-20: Read Mode

SDIN_TDI to SDOUT_TDO combinational path for daisy chain connection of multiple GS1662 devices.

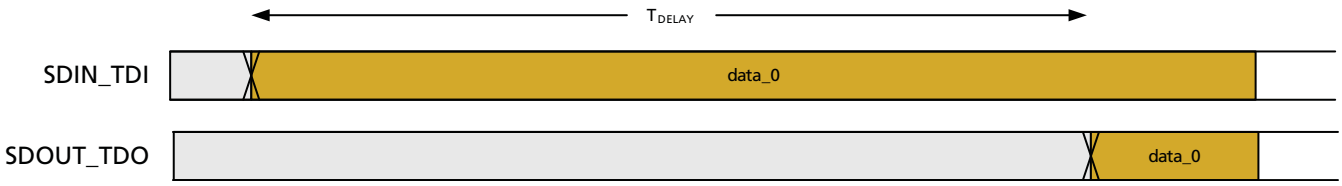


Figure 4-21: GSPI Time Delay

Table 4-14: GSPI Time Delay

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Delay time	t_{DELAY}	50% levels; 1.8V operation	–	–	10.5	ns
Delay time	t_{DELAY}	50% levels; 3.3V operation	–	–	8.7	

Table 4-15: GSPI AC Characteristics

Parameter	Symbol	Conditions	Min		Typ	Max	Units
$\overline{CS}$ low before SCLK rising edge	t_0	50% levels; 3.3V or 1.8V operation	1.5		–	–	ns
SCLK period	t_1		12.5		–	–	ns
SCLK duty cycle	t_2		40		50	60	%
Input data setup time	t_3		1.5		–	–	ns
Time between end of Command Word (or data in Auto-Increment mode) and the first SCLK of the following Data Word – write cycle.	t_4		PCLK (MHz)	ns	–	–	ns
			unlocked	445			
			13.5	74.2			
			27.0	37.1			
			74.25	13.5			
			148.5	6.7			
Time between end of Command Word (or data in Auto-Increment mode) and the first SCLK of the following Data Word – read cycle.	t_5		PCLK (MHz)	ns	–	–	ns
			unlocked	1187			
			13.5	297			
			27.0	148.5			
			74.25	53.9			
			148.5	27			
Output hold time (15pF load)	t_6		1.5		–	–	ns
$\overline{CS}$ HIGH after last SCLK falling edge	t_7		PCLK (MHz)	ns	–	–	ns
			unlocked	445			
			74.2	74.2			
			37.10	37.1			
			74.25	13.5			
			148.5	6.7			
Input data hold time	t_8		1.5		–	–	ns

NOTE: If the application interface performs a Read or Write access after power-up, prior to the application of a valid serial video input signal, the SCLK frequency must not exceed 10MHz.

4.12 Host Interface Register Maps

Table 4-16: Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
000h	IOPROC	RSVD	15	Reserved.	R	0
		DELAY_LINE_ENABLE	14	HIGH - enables the delay line delay.	R/W	0
		RSVD	13	Reserved.	R	0
		EDH_CRC_UPDATE	12	HIGH - preserve incoming EDH flags and insert into outgoing EDH packets. LOW - embed flags from 003 in EDH packet.	R/W	0
		ANC_INS	11	HIGH - disable ancillary data insertion. LOW - enable ancillary data insertion.	R	0
		RSVD	10 - 9	Reserved.	R/W	0
		H_CONFIG	8	Chooses H configuration; LOW - Active Picture timing HIGH - SMPTE H timing	R/W	0
		RSVD	7	Reserved.	R/W	0
		SMPTE_352M_INS	6	HIGH - disables insertion of SMPTE 352M packets.	R/W	0
		ILLEGAL_WORD_REMAP	5	HIGH - disables illegal word remapping.	R/W	0
		EDH_CRC_INS	4	HIGH - disables EDH CRC error correction and insertion.	R/W	0
		ANC_CSUM_INS	3	HIGH - disables insertion of ancillary data checksums.	R/W	0
		CRC_INS	2	HIGH - disables insertion of HD CRC words.	R/W	0
		LNUM_INS	1	HIGH - disables insertion of HD line numbers.	R/W	0
		TRS_INS	0	HIGH - disables insertion of TRS words.	R/W	0

Table 4-16: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
001h	ERROR_STAT	RSVD	15-7	Reserved.	R	0
		TRS_PERR	6	TRS protection error. LOW - No errors in TRS. HIGH - Errors in TRS.	R	0
		Y1_EDH_CS_ERR	5	Same as CS_ERR but only updates its state when packet being inspected is an EDH packet.	R	0
		Y1_CS_ERR	4	HIGH indicates that a checksum error is detected. It is updated every time a $\overline{CS}$ word is present on the output. **NOTE:** This bit will not be set for CSUM values in the protected ranges (from 000h to 003h and from 3FCh to 3FFh).	R	0
		FORMAT_ERR	3	HIGH indicates standard is not recognized for 861D conversion.	R	0
		TIMING_ERR	2	HIGH indicates that the RASTER measurements do not line up with the extracted 352M packet information.	R	0
		NO_352M_ERR	1	HIGH indicates no 352M packet embedded in incoming video.	R	0
		LOCK_ERR	0	HIGH indicates PLL lock error indication.	R	0

Table 4-16: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
002h	EDH_FLAG_EXT	RSVD	15	Reserved.	R	0
		ANC_UES_EXT	14	Ancillary data - unknown error status flag.	R	0
		ANC_IDA_EXT	13	Ancillary data - internal error detected already flag.	R	0
		ANC_IDH_EXT	12	Ancillary data - internal error detected here flag.	R	0
		ANC_EDA_EXT	11	Ancillary data - error detected already flag.	R	0
		ANC_EDH_EXT	10	Ancillary data - error detected here flag.	R	0
		FF_UES_EXT	9	EDH Full Field - unknown error status flag.	R	0
		FF_IDA_EXT	8	EDH Full Field - internal error detected already flag.	R	0
		FF_IDH_EXT	7	EDH Full Field - internal error detected here flag.	R	0
		FF_EDA_EXT	6	EDH Full Field - error detected already flag.	R	0
		FF_EDH_EXT	5	EDH Full Field - error detected here flag.	R	0
		AP_UES_EXT	4	EDH Active Picture - unknown error status flag.	R	0
		AP_IDA_EXT	3	EDH Active Picture - internal error detected already flag.	R	0
		AP_IDH_EXT	2	EDH Active Picture - internal error detected here flag.	R	0
		AP_EDA_EXT	1	EDH Active Picture - error detected already flag.	R	0
		AP_EDH_EXT	0	EDH Active Picture - error detected here flag.	R	0

Table 4-16: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
003h	EDH_FLAG_PGM	RSVD	15	Reserved.	R	0
		ANC_UES_PGM	14	Ancillary data - unknown error status flag.	R	0
		ANC_IDA_PGM	13	Ancillary data - internal error detected already flag.	R/W	0
		ANC_IDH_PGM	12	Ancillary data - internal error detected here flag.	R/W	0
		ANC_EDA_PGM	11	Ancillary data - error detected already flag.	R/W	0
		ANC_EDH_PGM	10	Ancillary data - error detected here flag.	R/W	0
		FF_UES_PGM	9	EDH Full Field - unknown error status flag.	R/W	0
		FF_IDA_PGM	8	EDH Full Field - internal error detected already flag.	R/W	0
		FF_IDH_PGM	7	EDH Full Field - internal error detected here flag.	R/W	0
		FF_EDA_PGM	6	EDH Full Field - error detected already flag.	R/W	0
		FF_EDH_PGM	5	EDH Full Field - error detected here flag.	R/W	0
		AP_UES_PGM	4	EDH Active Picture - unknown error status flag.	R/W	0
		AP_IDA_PGM	3	EDH Active Picture - internal error detected already flag.	R/W	0
		AP_IDH_PGM	2	EDH Active Picture - internal error detected here flag.	R/W	0
		AP_EDA_PGM	1	EDH Active Picture - error detected already flag.	R/W	0
		AP_EDH_PGM	0	EDH Active Picture - error detected here flag.	R/W	0

Table 4-16: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
004h	DATA_FORMAT	RSVD	15-10	Reserved.	R	0
		VD_STD	9-5	Detected video standard.	R	0
		INT_PROGB	4	HIGH - interlaced signal LOW - progressive signal	R	0
		RSVD	3	Reserved.	R	0
		STD_LOCK	2	Standard lock indication. Active HIGH.	R	0
		V_LOCK	1	Vertical lock indication. Active HIGH.	R	0
		H_LOCK	0	Horizontal lock indication. Active HIGH.	R	0
005h	RSVD	RSVD	15-0	Reserved.	R	0
006h	VSD_FORCE	RSVD	15-6	Reserved.	R	0
		VSD_FORCE	5	Use the CSR register STD value rather than the flywheels STD value. Active HIGH.	R/W	0
		VID_STD_FORCE	4-0	Force VID STD CSR.	R/W	0
007h	EDH_STATUS	RSVD	15-2	Reserved.	R	0
		FF_CRC_V	1	Full Field extracted V bit.	R	0
		AP_CRC_V	0	Active Picture extracted V bit.	R	0
008h	FIRST_AVAIL_POSITION	RSVD	15-1	Reserved.	R	0
		FIRST_AVAIL_POSITION	0	HIGH - 352M insertion occurs on first available ANC space. LOW - insert 352M packets right after EAV/CRC1.	R/W	1
009h	RSVD	RESERVED_7	15-0	–	R	0
00Ah	VIDEO_FORMAT_352_OUT_WORD_1	VIDEO_FORMAT_OUT_DS1_2	15-8	SMPTE 352M luma embedded packet - byte 2.	R/W	0
		VIDEO_FORMAT_OUT_DS1_1	7-0	SMPTE 352M luma embedded packet - byte 1.	R/W	0
00Bh	VIDEO_FORMAT_352_OUT_WORD_2	VIDEO_FORMAT_OUT_DS1_4	15-8	SMPTE 352M luma embedded packet - byte 4.	R/W	0
		VIDEO_FORMAT_OUT_DS1_3	7-0	SMPTE 352M luma embedded packet - byte 3.	R/W	0
00Ch	VIDEO_FORMAT_352_OUT_WORD_3	VIDEO_FORMAT_OUT_DS2_2	15-8	SMPTE 352M chroma embedded packet - byte 2.	R/W	0
		VIDEO_FORMAT_OUT_DS2_1	7-0	SMPTE 352M chroma embedded packet - byte 1.	R/W	0

Table 4-16: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
00Dh	VIDEO_FORMAT_352_OUT_WORD_4	VIDEO_FORMAT_OUT_DS2_4	15-8	SMPTE 352M chroma embedded packet - byte 4.	R/W	0
		VIDEO_FORMAT_OUT_DS2_3	7-0	SMPTE 352M chroma embedded packet - byte 3.	R/W	0
00Eh	VIDEO_FORMAT_352_IN_WORD_1	VIDEO_FORMAT_IN_DS1_2	15-8	SMPTE 352M luma extracted packet - byte 2.	R	0
		VIDEO_FORMAT_IN_DS1_1	7-0	SMPTE 352M luma extracted packet - byte 1.	R	0
00Fh	VIDEO_FORMAT_352_IN_WORD_2	VIDEO_FORMAT_IN_DS1_4	15-8	SMPTE 352M luma extracted packet - byte 4.	R	0
		VIDEO_FORMAT_IN_DS1_3	7-0	SMPTE 352M luma extracted packet - byte 3.	R	0
010h	VIDEO_FORMAT_352_IN_WORD_3	VIDEO_FORMAT_IN_DS2_2	15-8	SMPTE 352M chroma extracted packet - byte 2.	R	0
		VIDEO_FORMAT_IN_DS2_1	7-0	SMPTE 352M chroma extracted packet - byte 1.	R	0
011h	VIDEO_FORMAT_352_IN_WORD_4	VIDEO_FORMAT_IN_DS2_4	15-8	SMPTE 352M chroma extracted packet - byte 4.	R	0
		VIDEO_FORMAT_IN_DS2_3	7-0	SMPTE 352M chroma extracted packet - byte 3.	R	0
012h	RASTER_STRUC_1	RSVD	15-11	Reserved.	R	0
		LINES_PER_FRAME	10-0	Total lines per frame.	R	0
013h	RASTER_STRUC_2	RSVD	15-14	Reserved.	R	0
		WORDS_PER_LINE	13-0	Total words per line.	R	0
014h	RASTER_STRUC_3	RSVD	15-13	Reserved.	R	0
		ACTIVE_WORDS_PER_LINE	12-0	Words per active line.	R	0
015h	RASTER_STRUC_4	RSVD	15-11	Reserved.	R	0
		ACTIVE_LINES_PER_FIELD	10-0	Active lines per frame.	R	0
016h - 023h	RSVD	RSVD	–	Reserved.	R	0

Table 4-16: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
024h	FIRST_LINE_ NUMBER_ STATUS	RSVD	15-2	Reserved.	R	0
		PACKET_MISSED	1	ANC data packet could not be inserted in its entirety. HIGH - ANC packet cannot be inserted in it's entirety.	R	0
		RW_CONFLICT	0	Same RAM address was read and written to at the same time. HIGH - one of the addresses from 040h to 13Fh was read and written to at the same time.	R	0
025h	FIRST_LINE_ NUMBER	RSVD	15-12	Reserved.	R	0
		ANC_INS_MODE	11	ANC data insertion mode. HIGH - Concatenate LOW - Separate	R/W	0
		FIRST_LINE_NUMBER	10-0	First line number to insert ANC packet on.	R/W	0
026h	FIRST_LINE_ NUMBER_OF_ WORDS	FIRST_LINE_NUMBER_ANC_T YPE	15	ANC region to insert packet in HIGH - VANC, LOW - HANC.	R/W	0
		FIRST_LINE_NUMBER _STREAM_TYPE	14	Stream to insert packet in HIGH - C stream, LOW - Y stream.	R/W	0
		RSVD	13-10	Reserved.	R	0
		FIRST_LINE_NUMBER _OF_WORDS	9-0	Total number of words in ANC packet to be inserted in first line.	R/W	0
027h	SECOND_LINE_ NUMBER	RSVD	15-11	Reserved.	R	0
		SECOND_LINE_NUMBER	10-0	Second line number to insert ANC packet on in Separate Line mode.	R/W	0
028h	SECOND_LINE_ NUMBER_OF_ WORDS	SECOND_LINE_NUMBER _ANC_TYPE	15	ANC region to insert packet in HIGH - VANC, LOW - HANC.	R/W	0
		SECOND_LINE_NUMBER _STREAM_TYPE	14	Stream to insert packet in HIGH - C stream, LOW - Y stream.	R/W	0
		RSVD	13-10	Reserved.	R	0
		SECOND_LINE_NUMBER _OF_WORDS	9-0	Total number of words in ANC packet to be inserted in second line.	R/W	0
029h	THIRD_LINE_ NUMBER	RSVD	15-11	Reserved.	R	0
		THIRD_LINE_NUMBER	10-0	Third line number to insert ANC packet on in Separate Line mode.	R/W	0

Table 4-16: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
02Ah	THIRD_LINE_NUMBER_OF_WORDS	THIRD_LINE_NUMBER_ANC_TYPE	15	ANC region to insert packet in. HIGH - VANC, LOW - HANC.	R/W	0
		THIRD_LINE_NUMBER_STREAM_TYPE	14	Stream to insert packet in. HIGH - C stream, LOW - Y stream.	R/W	0
		RSVD	13-10	Reserved.	R	0
		THIRD_LINE_NUMBER_OF_WORDS	9-0	Total number of words in ANC packet to be inserted in third line.	R/W	0
02Bh	FOURTH_LINE_NUMBER	RSVD	15-11	Reserved.	R	0
		FOURTH_LINE_NUMBER	10-0	Fourth line number to insert ANC packet on in Seperate Line mode.	R/W	0
02Ch	FOURTH_LINE_NUMBER_OF_WORDS	FOURTH_LINE_NUMBER_ANC_TYPE	15	ANC region to insert packet in HIGH - VANC, LOW - HANC.	R/W	0
		FOURTH_LINE_NUMBER_STREAM_TYPE	14	Stream to insert packet in 1-C stream, 0-Y stream.	R/W	0
		RSVD	13-10	Reserved.	R	0
		FOURTH_LINE_NUMBER_OF_WORDS	9-0	Total number of words in ANC packet to be inserted in fourth line.	R/W	0
02Dh	STREAM_TYPE_1	RSVD	15-5	Reserved.	R	0
		EDH_LINE_CHECK_EN	4	HIGH - ANC block will not insert data into the EDH region of the HANC space. LOW - ANC block will insert data into the EDH region.	R/W	1
		STREAM_TYPE1_LINE_4	3	HIGH - data for the fourth line in separate mode is inserted into the Chroma Stream. LOW - Luma Stream.	R/W	0
		STREAM_TYPE1_LINE_3	2	HIGH - data for the third line in separate mode is inserted into the Chroma Stream. LOW - Luma Stream.	R/W	0
		STREAM_TYPE1_LINE_2	1	HIGH - data for the second line in separate mode is inserted into the Chroma Stream. LOW - Luma Stream.	R/W	0
		STREAM_TYPE1_LINE_1	0	HIGH - data for the first line in separate mode is inserted into the Chroma Stream. LOW - Luma Stream.	R/W	0
02Eh - 03Fh	RSVD	RSVD	15-0	Reserved.	R	0

Table 4-16: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
040h - 07Fh	ANC_PACKET _BANK_1	ANC_PACKET_BANK	15-0	First bank of user-defined 8-bit ancillary data. Bit 15 - 8: 2nd byte (MSB to LSB) Bit 7 - 0: 1st byte (MSB to LSB) See 4.7 ANC Data Insertion.	R/W	–
080h - 0BFh	ANC_PACKET _BANK_2	ANC_PACKET_BANK	15-0	First bank of user-defined 8-bit ancillary data. Bit 15 - 8: 2nd byte (MSB to LSB) Bit 7 - 0: 1st byte (MSB to LSB) See 4.7 ANC Data Insertion.	R/W	–
0C0h - 0FFh	ANC_PACKET _BANK_3	ANC_PACKET_BANK	15-0	First bank of user-defined 8-bit ancillary data. Bit 15 - 8: 2nd byte (MSB to LSB) Bit 7 - 0: 1st byte (MSB to LSB) See 4.7 ANC Data Insertion.	R/W	–
100h - 13Fh	ANC_PACKET _BANK_4	ANC_PACKET_BANK	15-0	First bank of user-defined 8-bit ancillary data. Bit 15 - 8: 2nd byte (MSB to LSB) Bit 7 - 0: 1st byte (MSB to LSB) See 4.7 ANC Data Insertion.	R/W	–
140h - 209h	RSVD	RSVD	–	Reserved.	R	0
20Ah	SDTI_TDM	RSVD	15-8	Reserved.	R	0
		SDTI_TDM_DS2	7	HIGH indicates an SDTI type signal on input for the Chroma Stream.	R/W	0
		SDTI_TDM_DS1	6	HIGH indicates an SDTI type signal on input for the Luma Stream.	R/W	0
		RSVD	5-0	Reserved.	R	0
20Bh - 20Dh	RSVD	RSVD	15-0	Reserved.	R	0
20Eh	DRIVE_ STRENGTH	RSVD	15-4	Reserved.	R/W	0
		LOCKED_DS	3-2	Drive strength value for LOCKED pin. 00: 4mA; 01: 6mA; 10: 8mA(1.8V), 10mA(3.3V); 11: 10mA(1.8V), 12mA(3.3V)	R/W	0
		SDOUT_TDO_DS	1-0	Drive strength value for SDOUT_TDO pin. 00: 4mA; 01: 6mA; 10: 8mA(1.8V), 10mA(3.3V); 11: 10mA(1.8V), 12mA(3.3V)	R/W	2
20Fh	RSVD	RSVD	15-0	Reserved.	R/W	0

Table 4-16: Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
210h	DRIVE_ STRENGTH2	TDO_DS	15-14	Drive strength value for TDO pin. 00: 4mA; 01: 6mA; 10: 8mA(1.8V), 10mA(3.3V); 11: 10mA(1.8V), 12mA(3.3V)	R/W	0
		RSVD	13-0	Reserved.	R/W	0
211h - 232h	RSVD	RSVD	15-0	Reserved.	R	0

4.13 JTAG ID Codeword

The Platform ID for the GS16x2 family is 0Fh.

The part number field of the JTAG ID codeword for the GS1662 is set to 0F00h.

4.14 JTAG Test Operation

When the JTAG/$\overline{\text{HOST}}$ pin is HIGH, the GSPI host interface port is configured for JTAG test operation.

In this mode the SCLK, SDIN, SDOUT and $\overline{\text{CS}}$ become TCK, TDI, TDO and TMS. In addition, the TRST pin becomes active.

Boundary scan testing using the JTAG interface is enabled in this mode. When the JTAG/$\overline{\text{HOST}}$ pin is LOW, the dedicated JTAG interface is used. In this mode the TCK, TDI, TDO and TMS pins are active. This is the recommended mode for new designs.

4.15 Device Power-Up

Because the GS1662 is designed to operate in a multi-voltage environment, any power-up sequence is allowed. The Charge Pump, Phase Detector, Core Logic, Serial Digital Output and I/O Buffers can all be powered up in any order.

4.16 Device Reset

NOTE: At power-up, the device must be reset to operate correctly.

In order to initialize all internal operating conditions to their default states, hold the $\overline{\text{RESET}}$ signal LOW for a minimum of t_{reset} = 1ms after all power supplies are stable. There are no requirements for power supply sequencing.

When held in reset, all device outputs will be driven to a high-impedance state.

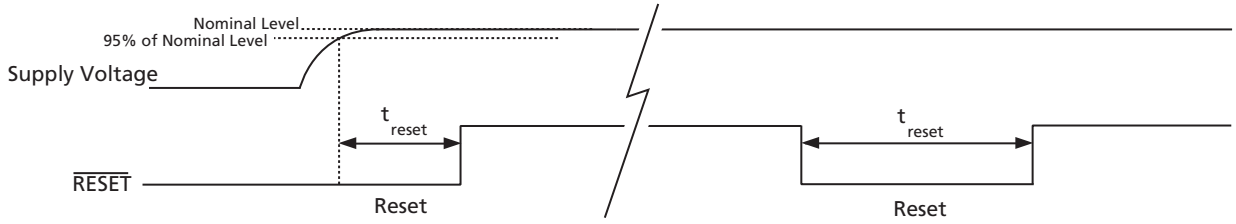
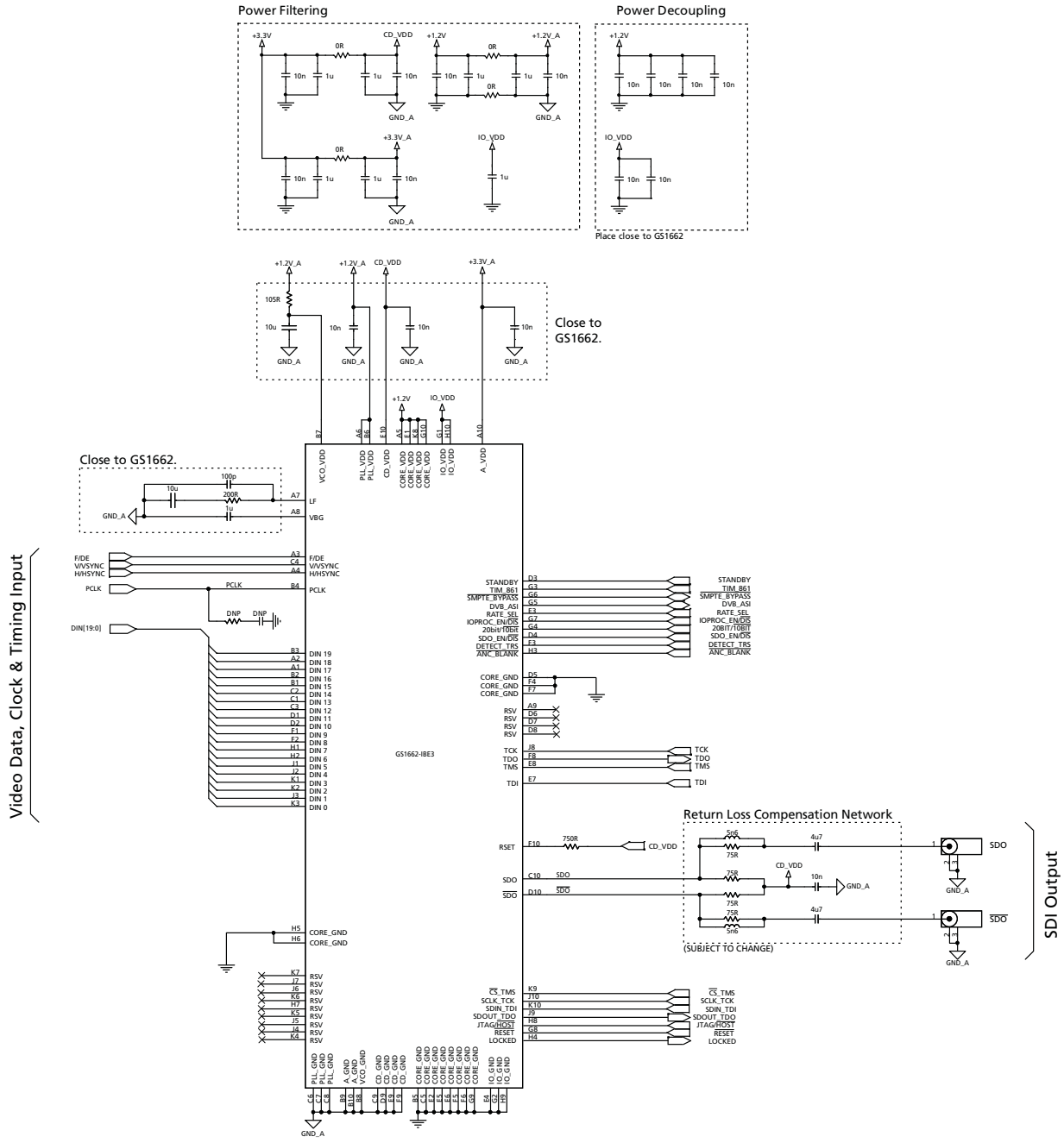


Figure 4-22: Reset Pulse

5. Application Reference Design

5.1 Typical Application Circuit

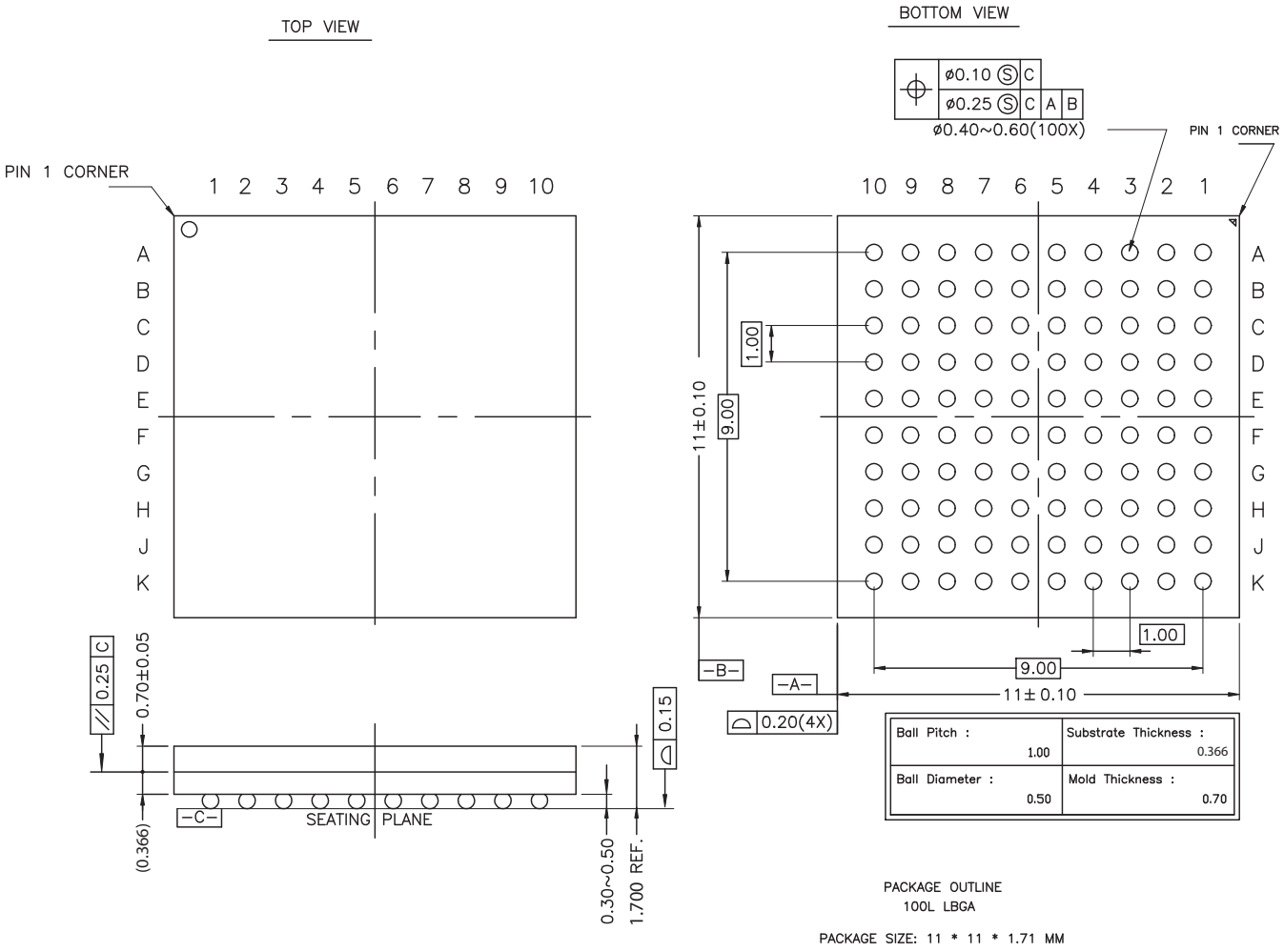


6. References & Relevant Standards

SMPTE 125M	Component video signal 4:2:2 – bit parallel interface
SMPTE 259M	10-bit 4:2:2 Component and 4fsc Composite Digital Signals - Serial Digital Interface
SMPTE 260M	1125 / 60 high definition production system – digital representation and bit parallel interface
SMPTE 267M	Bit parallel digital interface – component video signal 4:2:2 16 x 9 aspect ratio
SMPTE 272M	Formatting AES/EBU Audio and Auxiliary Data into Digital Video Ancillary Data Space
SMPTE 274M	1920 x 1080 scanning analog and parallel digital interfaces for multiple picture rates
SMPTE 291M	Ancillary Data Packet and Space Formatting
SMPTE 292	Bit-Serial Digital Interface for High-Definition Television Systems
SMPTE 293M	720 x 483 active line at 59.94Hz progressive scan production – digital representation
SMPTE 296M	1280 x 720 scanning, analog and digital representation and analog interface
SMPTE 305M	Serial Data Transport Interface
SMPTE 348M	High Data-Rate Serial Data Transport Interface (HD-SDTI)
SMPTE 352M	Video Payload Identification for Digital Television Interfaces
SMPTE 372	Dual Link 292M Interface for 1920 x 1080 Picture Raster
SMPTE RP165	Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television
SMPTE RP168	Definition of Vertical Interval Switching Point for Synchronous Video Switching
CEA 861	Video Timing Requirements

7. Package & Ordering Information

7.1 Package Dimensions



PACKAGE OUTLINE
100L LBGA

PACKAGE SIZE: 11 * 11 * 1.71 MM

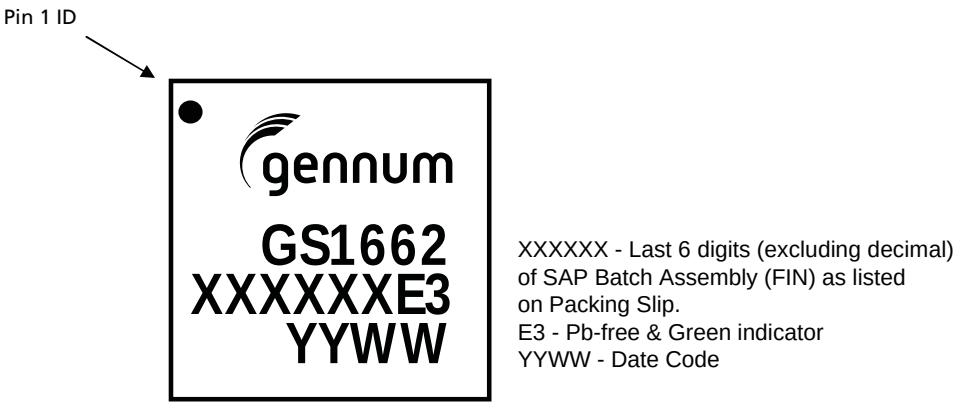
* THE BALL DIAMETER, BALL PITCH, STAND–OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC M0192 (LOW PROFILE BGA FAMILY)

7.2 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	11mm x 11mm 100-ball LBGA
Package Drawing Reference	JEDEC M0192 (with exceptions noted in Package Dimensions on page 70).
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	10.4°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	37.1°C/W
Junction to Board Thermal Resistance, θ_{j-b}	26.4°C/W
Psi, ψ	0.4°C/W
Pb-free and RoHS Compliant	Yes

7.3 Marking Diagram



7.4 Solder Reflow Profiles

The GS1662 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 7-1.

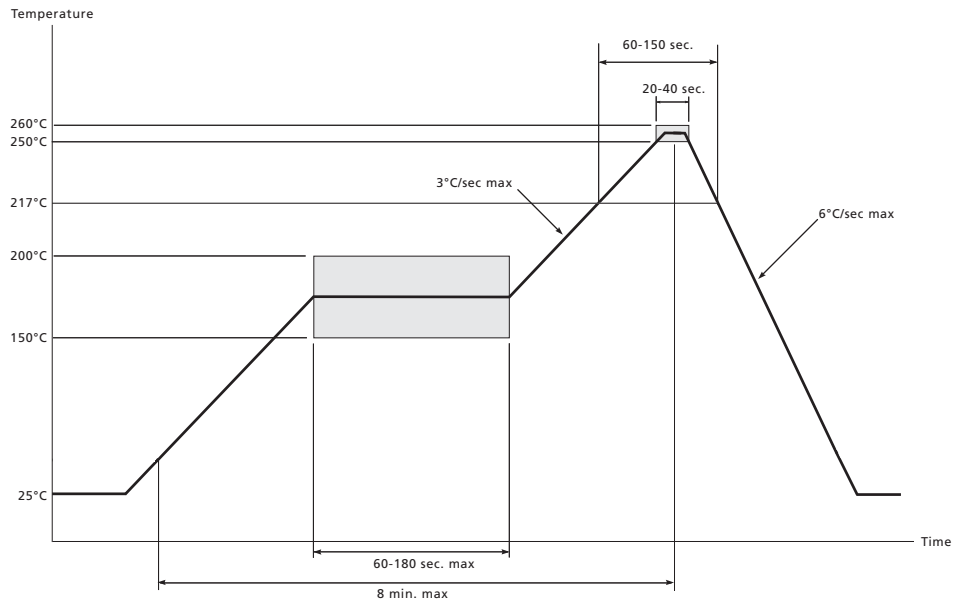


Figure 7-1: Pb-free Solder Reflow Profile

7.5 Ordering Information

Part Number	Package	Pb-free	Temperature Range
GS1662-IBE3	100-ball BGA	Yes	-20°C to 85°C

DOCUMENT IDENTIFICATION

DATA SHEET

The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION

ELECTROSTATIC SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

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