Low Cost 10-Bit, 6-Channel Output Decimating LCD DecDriver®

AD8383

FEATURES

High voltage drive to within 1.3 V of supply rails
Output short-circuit protection
High update rates
Fast, 100 Ms/s, 10-bit input data update rate
Low static power dissipation: 0.7 W
Includes STBY function
Voltage-controlled video reference (brightness) and full-scale (contrast) output levels
INV bit reverses polarity of video signal
3.3 V logic, 9 V to 18 V analog supplies
High accuracy voltage outputs
Laser trimming eliminates the need for adjustments
Flexible logic
STSQ/XFR allow parallel AD8383 operation at various resolutions
Fast settling into capacitive loads
30 ns settling time to 0.25% into 150 pF load
Slew rate 460 V/µs
Available in 48-lead 7 mm × 7 mm LFCSP package

APPLICATIONS

LCD analog column driver

FUNCTIONAL BLOCK DIAGRAM

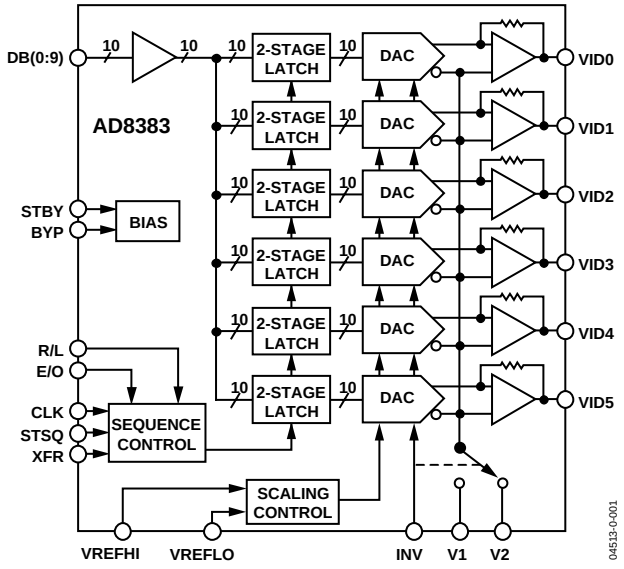

Figure 1

PRODUCT DESCRIPTION

The AD8383 provides a fast, 10-bit latched decimating digital input that drives six high voltage outputs. 10-bit input words are sequentially loaded into six separate, high speed, bipolar DACs. Flexible digital input format allows several AD8383s to be used in parallel for higher resolution displays. STSQ synchronizes sequential input loading, XFR controls synchronous output updating, and R/L controls the direction of loading as either left-to-right or right-to-left. Six channels of high voltage output drivers drive to within 1.3 V of the rail. For maximum flexibility, the output signal can be adjusted for dc reference, signal inversion.

The AD8383 is fabricated on the 26 V, fast bipolar XFHV process developed by Analog Devices, Inc. This process provides fast input logic, bipolar DACs with trimmed accuracy and fast settling, high voltage, precision drive amplifiers on the same chip.

The AD8383 dissipates 0.7 W nominal static power. The STBY pin reduces power to a minimum with fast recovery.

The AD8383 is offered in a 48-lead, 7 mm × 7 mm × 0.85 mm LFCSP package and operates over the commercial temperature range of 0°C to 85°C.

Rev. 0
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REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

Table 1. @25°C, AVCC = 15.5 V, DVCC = 3.3 V, T_{MIN} = 0°C, T_{MAX} = 75°C, VFS = 5 V, VREFLO = V1 = V2 = 7 V, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
VIDEO DC PERFORMANCE[1]	T_{MIN} to T_{MAX}, DAC Code 450 to 800				
VDE		−7.5		+7.5	mV
VCME		−3.5		+3.5	mV
REFERENCE INPUTS					
V1, V2 Range		5		AVCC – 4	V
V2 to V1 Range		−0.25			V
V1 Input Current			+0.2		µA
V2 Input Current			−7.5		µA
VREFHI Range	VREFHI ≥ VREFLO	VREFLO		AVCC	V
VREFLO Range	VREFHI ≥ VREFLO	V1 – 0.5		AVCC – 1.3	V
VREFHI Input Resistance	To VREFLO		20		kΩ
VREFLO Bias Current			−0.2		µA
VREFHI Input Current			125		µA
VFS Range[2]		0		5.5	V
RESOLUTION					
Coding	Binary	10			Bits
DIGITAL INPUT CHARACTERISTICS					
Maximum Input Data Update Rate[3]		100			Ms/s
CLK to Data Setup Time		0			ns
CLK to STSQ Setup Time		1			ns
CLK to XFR Setup Time		1			ns
CLK to Data Hold Time		3			ns
CLK to STSQ Hold Time		3			ns
CLK to XFR Hold Time		3			ns
CLK High Time		3			ns
CLK Low Time		2.5			ns
C_{IN}				3	pF
I_{IH}			0.05		µA
I_{IL}			0.6		µA
I_{IL}, CLK			1.2		µA
V_{IH}		2			V
V_{IL}				0.8	V
V_{TH}			1.5		V
VIDEO OUTPUT CHARACTERISTICS					
Output Voltage Swing	AVCC – VOH, VOL – AGND		1.1	1.3	V
CLK to VID Delay[4]	50% of VIDx	10.0	12.0	14.0	ns
INV to VID Delay	50% of VIDx	10.4	12.4	14.4	ns
Output Current			100		mA
Output Resistance			22		Ω

[1] VDE = Differential Error Voltage = Common-Mode Error Voltage. See Theory of Operation section.
[2] VFS = 2 × (VREFHI – VREFLO).
[3] Maximum input transition time (10% to 90%) = 0.8/(2f) where f is the operating CLK rate.
[4] Measured from 50% of falling CLK edge to 50% of output change. Measurement is made for both states of INV.

SPECIFICATIONS (continued)

Parameter	Conditions	Min	Typ	Max	Unit
VIDEO OUTPUT DYNAMIC PERFORMANCE	$T_{C, MIN}$ to $T_{C, MAX}$, V_O = 5 V Step, C_L = 150 pF				
Data Switching Slew Rate	20% to 80%		460		V/µs
Invert Switching Slew Rate	20% to 80%		560		V/µs
Data Switching Settling Time to 1%			19	24	ns
Data Switching Settling Time to 0.25%			30	50	ns
Invert Switching Settling Time to 1%	V_O = 10 V Step		75	120	ns
Invert Switching Settling Time to 0.25%	V_O = 10 V Step		250	500	ns
Invert Switching Overshoot	V_O = 10 V Step		100	200	mV
CLK and Data Feedthrough[5]			10		mV p-p
All-Hostile Crosstalk[6]					
Amplitude			40		mV p-p
Duration			20		ns
DAC Transition Glitch Energy	Code 511 to Code 512		0.3		nV-s
POWER SUPPLY					
DVCC, Operating Range		3	3.3	3.6	V
DVCC, Quiescent Current			20	28	mA
AVCC, Operating Range		9		18	V
Total AVCC Quiescent Current			40	48	mA
STBY AVCC Current STBY = H			0.15	0.45	mA
STBY DVCC Current STBY = H			3.5	5	mA
OPERATING TEMPERATURE RANGE, T_A	Ambient Temperature	0		75	°C
AMBIENT TEMPERATURE RANGE[7]		0		85	°C
OPERATING TEMPERATURE RANGE, T_J	100% tested	25		125	°C

[5] Measured on two outputs differentially as CLK and DB(0:9) are driven and STSQ and XFR are held low.
[6] Measured on two outputs differentially as the other four outputs make a full-scale transition for both states of INV.
[7] Operation at 85°C ambient temperature requires a thermally optimized PCB layout (see Application Notes), minimum airflow of 200 lfm, input clock rate not exceeding 100 MHz, black-to-white transition ≤4 V, C_L ≤150 pF.

ABSOLUTE MAXIMUM RATINGS

Table 2. AD8383 Stress Ratings

Parameter	Rating
Supply Voltages	
AVCCx – AGNDx	18 V
DVCC – DGND	4.5 V
Input Voltages	
Maximum Digital Input Voltages	DVCC + 0.5 V
Minimum Digital Input Voltages	DGND – 0.5 V
Maximum Analog Input Voltages	AVCC + 0.5 V
Minimum Analog Input Voltages	AGND – 0.5 V
Internal Power Dissipation[8]	
LFCSP Package @ 25°C Ambient	3.8 W
Operating Temperature Range	0°C to 85°C
Storage Temperature Range	–65°C to +125°C
Lead Temperature Range (Soldering 10 sec)	300°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings for extended periods may reduce device reliability.

[8] 48-Lead LFCSP Package:
θ_{JA} = 26°C/W (Still Air): JEDEC STD, 4-layer board with 0 CFM airflow
θ_{JC} = 20°C/W
ψ_{JB} = 11.0°C/W in Still Air

MAXIMUM POWER DISSIPATION

Junction Temperature

The maximum power that can be safely dissipated by the AD8383 is limited by its junction temperature. The maximum safe junction temperature for plastic encapsulated devices as determined by the glass transition temperature of the plastic is approximately 150°C. Exceeding this limit temporarily may cause a shift in the parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

Overload Protection

The AD8383 employs a 2-stage overload protection circuit that consists of an output current limiter and a thermal shutdown. The maximum current at any one output of the AD8383 is internally limited to 100 mA, average. In the event of a momentary short-circuit between a video output and a power supply rail (AVCC or AGND), the output current limit is sufficiently low to provide temporary protection.

The thermal shutdown debiases the output amplifier when the junction temperature reaches the internally set trip point. In the event of an extended short-circuit between a video output and a power supply rail, the output amplifier current continues to switch between 0 mA and 100 mA typical with a period determined by the thermal time constant and the hysteresis of the thermal trip point. The thermal shutdown provides long-term protection by limiting the average junction temperature to a safe level.

Operating Temperature Range

Production testing guarantees a minimum thermal shutdown junction temperature (T_J) of at least 125°C.

To ensure operation at T_J < 125°C, it is necessary to limit the maximum power dissipation as described in the Applications section.

Exposed Paddle

The die paddle must be soldered to AVCC for reliable electrical operation.

See the Applications section for details regarding use of the exposed paddles to dissipate excess heat.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

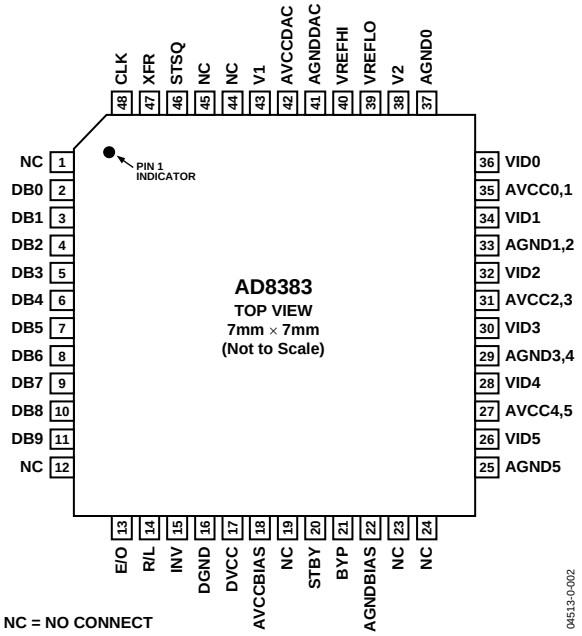


Figure 2. 48-Lead LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin Name	Function	Description
DB(0:9)	Data Input	10-Bit Data Input. MSB = DB(0:9).
CLK	Clock	Clock Input.
STSQ	Start Sequence	The state of STSQ is detected on the active edge of CLK. A new data loading sequence begins on the next active edge of CLK after STSQ is detected HIGH. The active CLK edge is the rising edge when E/O is held HIGH. It is the falling edge when E/O is held LOW.
R/L	Right/Left Select	A new data loading sequence begins on the left with Channel 0 when this input is LOW, and on the right with Channel 5 when this input is HIGH.
E/O	Even/Odd Select	The active CLK edge is the rising edge when this input is held HIGH and the falling edge when this input is held LOW. Data is loaded sequentially on the rising edges of CLK when this input is HIGH and on the falling edges when this input is LOW.
XFR	Data Transfer	XFR is detected and a data transfer is initiated on a rising CLK edge when this input is held HIGH. Data is transferred to the video outputs on the next rising CLK edge after XFR is detected.
VID0–VID5	Analog Outputs	These pins are directly connected to the analog inputs of the LCD panel.
V1, V2	Reference Voltages	The voltage applied between these pins set the reference levels of the analog outputs.
VREFHI, VREFLO	Full-Scale References	The voltage applied between these pins sets the full-scale output voltage.
INV	Invert	When this pin is HIGH, the analog output voltages are above VMID. When LOW, the analog output voltages are below VMID. VMID is a hypothetical reference level set by the voltages applied to V1 and V2. VMID is equal to (V1 + V2)/2.
DVCC	Digital Power Supply	Digital Power Supply.
DGND	Digital Supply Return	This pin is normally connected to the analog ground plane.
AVCCx	Analog Power Supplies	Analog Power Supplies.
AGNDx	Analog Supply Returns	Analog Supply Returns.
BYP	Bypass	A 0.1 µF capacitor connected between this pin and AGND ensures optimum settling time.
STBY	Standby	When HIGH, the internal circuits are debiased and the power dissipation drops to a minimum.

TIMING DIAGRAMS

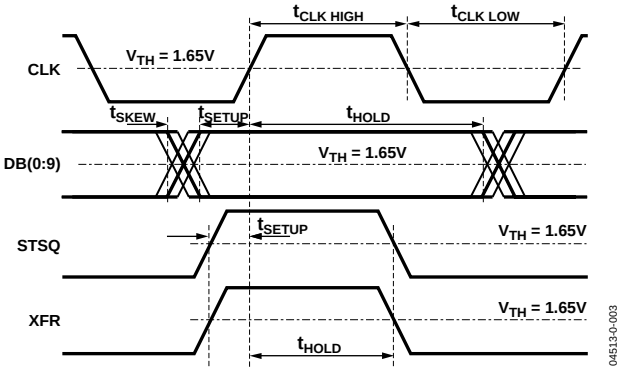


Figure 3. Timing Diagram, Even Mode (E/O = HIGH)

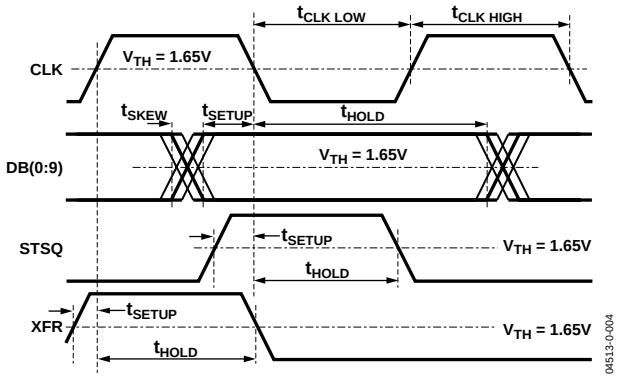


Figure 4. Timing Diagram, Odd Mode (E/O = LOW)

THEORY OF OPERATION

TRANSFER FUNCTION AND ANALOG OUTPUT VOLTAGE

The DecDriver has two regions of operation: where the video output voltages are either above or below a reference voltage VMID, and where VMID = (V1 + V2)/2. The transfer function defines the analog output voltage as the function of the digital input code as follows:

$$VIDx(n) = V1 - VFS \times \left(1 - \frac{n}{1023}\right) \text{ for INV = LOW}$$

$$VIDx(n) = V2 + VFS \times \left(1 - \frac{n}{1023}\right) \text{ for INV = HIGH}$$

where n = input code

$$VFS = 2 \times (VREFHI - VREFLO)$$

A number of internal limits define the usable range of the analog output voltages, VIDx, as shown in Figure 5.

To best correlate transfer function errors to image artifacts, the overall accuracy of the DecDriver is defined by two parameters, VDE and VCME.

VDE, the differential error voltage, measures the difference between the rms value of the output and the rms value of the ideal. The defining expression is

$$VDE(n) = \frac{[VOUTN(n) - V2] - [VOUTP(n) - V1]}{2} - \left(1 - \frac{n}{1023}\right) \times VFS$$

VCME, the common-mode error voltage, measures ½ the dc bias of the output. The defining expression is

$$VCME(n) = \frac{1}{2}\left[\frac{1}{2}\left(VOUTN(n) + VOUTP(n)\right) - \frac{V1 + V2}{2}\right]$$

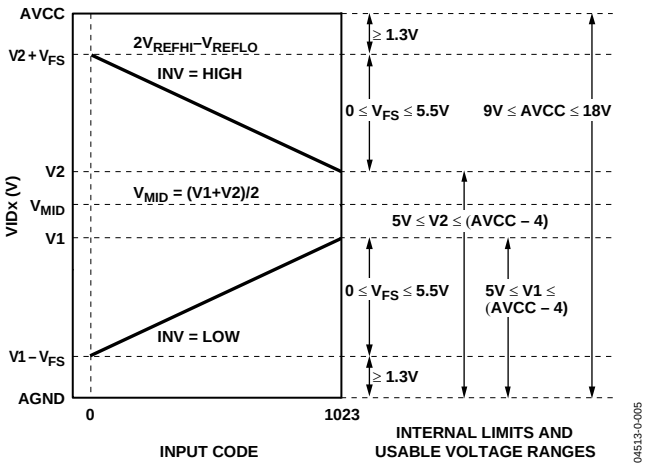


Figure 5. Transfer Function, VIDx vs. Input Code, Internal Limits and Usable Output Voltage Range

APPLICATIONS

The V1 and V2 inputs in these systems are tied together and are normally connected to VCOM, as shown in Figure 6.

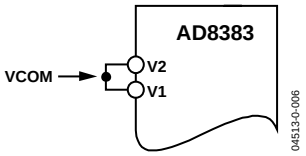


Figure 6. Standard Connection Diagram

The transfer function of the AD8383 is shown in Figure 7 for V2 = V1 = VCOM.

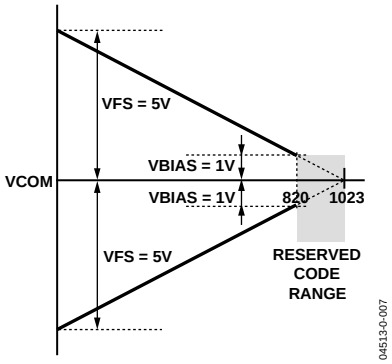


Figure 7. Output Transfer Function for Standard Connection

EXTERNAL VBIAS GENERATION

In systems that require improved brightness resolution and higher accuracy, the V1 and V2 inputs, connected to external voltage references, provide the necessary VBIAS while allowing the full code range to be used for gamma correction.

V1 sets the white drive voltage while INV = LOW and *V2* sets the white drive voltage while INV = HIGH. *V1* and *V2* are defined as

$$V1 = VCOM - VBIAS$$

$$V2 = VCOM + VBIAS$$

To ensure a symmetrical ac driving voltage, the difference between *V2* and *VCOM* must be equal to the difference between *VCOM* and *V1*.

$$(V2 - VCOM) = (VCOM - V1)$$

The circuit in Figure 8 ensures symmetry to within 1 mV with a minimum component count. Bypass capacitors are not shown for clarity.

The transfer function and the input symmetry error of the AD8383 are shown in Figure 9 when the circuit of Figure 8 is used to generate VBIAS.

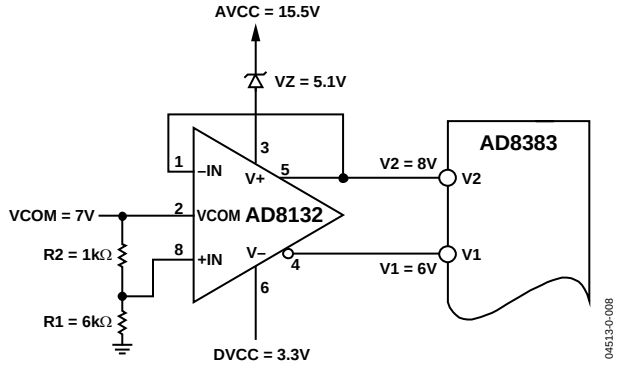
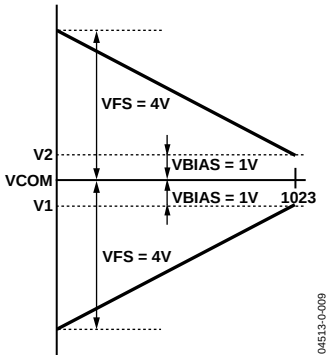


Figure 8. High Accuracy Reference Circuit



THE AD8383, IN THE APPLICATIONS CIRCUIT SHOWN, TYPICALLY PRODUCES A SYMMETRICAL OUTPUT AT 85°C WHEN ITS SUPPLY, (V+) – (V–), IS AT 7.2V.

Figure 9. Transfer Function for High Accuracy Reference Applications

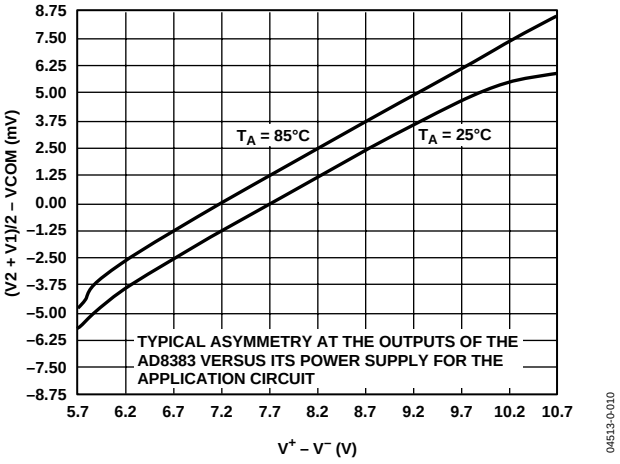


Figure 10. Accuracy for High Accuracy Reference Applications

PCB DESIGN FOR GOOD THERMAL PERFORMANCE

The total maximum power dissipation of the AD8383 is partly dependent on load. In a 6-channel 60 Hz XGA system running at a 65 MHz clock rate, the total maximum power dissipation is 1.08 W at an LCD panel input capacitance of 150 pF.

At the maximum specified clock rate of 100 Ms/s, the total maximum power dissipation can exceed 2 W for large capacitive loads, as shown in Table 4.

Although the maximum safe operating junction temperature is higher, the AD8383 is 100% tested at a junction temperature of 125°C. Consequently, the maximum guaranteed operating junction temperature is 125°C. To limit the maximum junction temperature at or below the guaranteed maximum, the package, in conjunction with the PCB, must effectively conduct heat away from the junction.

The AD8383's LFCSP package is designed to provide superior thermal characteristics, partly achieved by an exposed die paddle on the bottom surface of the package. In order to take full advantage of this feature, the exposed paddle must be in direct thermal contact with the PCB, which then serves as a heat sink.

A thermally effective PCB must incorporate a thermal pad and a thermal via structure. The thermal pad provides a solderable contact surface on the top surface of the PCB. The thermal via structure provides a thermal path to the inner and bottom layers of the PCB to remove heat.

THERMAL PAD DESIGN

Thermal performance of the AD8383 varies logarithmically with the contact area between the exposed thermal paddle and the thermal pad on the top layer of the PCB. See Figure 11.

The θ_{JA} (of the AD8383 mounted on a standard JEDEC PCB) is reduced by approximately 40% as the contact area increases from 0% (no thermal pad) to 50%. It approaches its specified value as the contact area (on the JEDEC standard PCB) approaches 100%.

In order to minimize thermal performance degradation of production PCBs, the contact area between the thermal pad and the PCB should be maximized. Therefore, the size of the thermal pad should match the exposed 5.25 mm × 5.25 mm paddle size. However, if the PCB design rules require a pad-to-pad clearance of more than 0.3 mm, the size of the thermal pad may be reduced to 5 mm × 5 mm. Additionally, a second thermal pad of the same size should be placed on the bottom side of the PCB. At least one thermal pad should be in direct thermal (and electrical) contact with the AVCC plane.

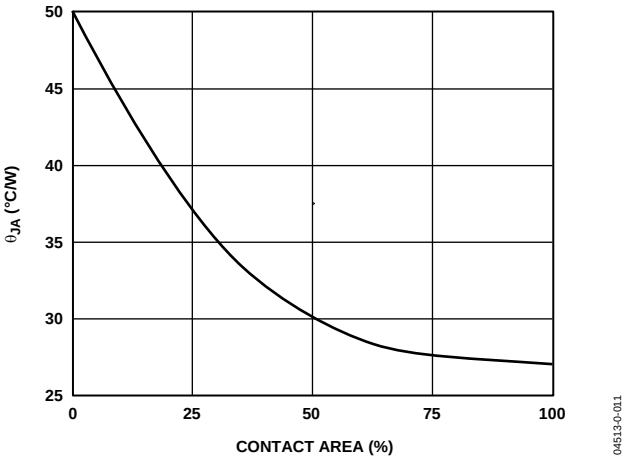


Figure 11. Thermal Performance vs. Contact Area (on a JEDEC PCB)

Table 4. Power Dissipation vs. Load Capacitance and VFS at 100 Ms/s Clock Rate

		VFS = 5 V		VFS = 4 V	
C_{LOAD} (pF)	$P_{QUIESCENT}$ (W)	$P_{DYNAMIC}$ (W)	P_{TOTAL} (W)	$P_{DYNAMIC}$ (W)	P_{TOTAL} (W)
150	0.7	0.72	1.42	0.58	1.28
200	0.7	0.96	1.66	0.77	1.47
250	0.7	1.20	1.90	0.96	1.66
300	0.7	1.44	2.14	1.15	1.85

THERMAL VIA STRUCTURE DESIGN

Effective heat transfer from the top to the inner and bottom layers of the PCB requires thermal vias incorporated into the thermal pad design. Thermal performance increases logarithmically with the number of vias, as shown in Figure 12. With the AD8383 on a standard JEDEC PCB, θ_{JA} reaches its specified value when a total of 16 vias are used. At a via count above 36, θ_{JA} approaches its optimum value as the slope of the curve approaches zero.

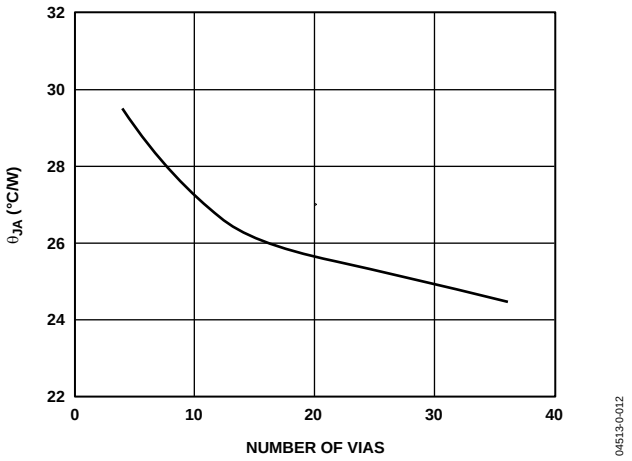


Figure 12. Thermal Performance vs. Number of Vias (on a JEDEC PCB)

Near optimum thermal performance of production PCBs is attained when the number of vias is at least 36.

SOLDER MASKING

To minimize the formation of solder voids due to solder flowing into the via holes (solder wicking), the via diameter should be small. Solder masking of the via holes on the top layer of the PCB plugs the via holes, inhibiting solder flow into the holes. To optimize the thermal pad coverage, the solder mask diameter should be no more than 0.1 mm larger than the via diameter.

REFERENCE PCB DESIGN

The top copper layer is shown in Figure 13.

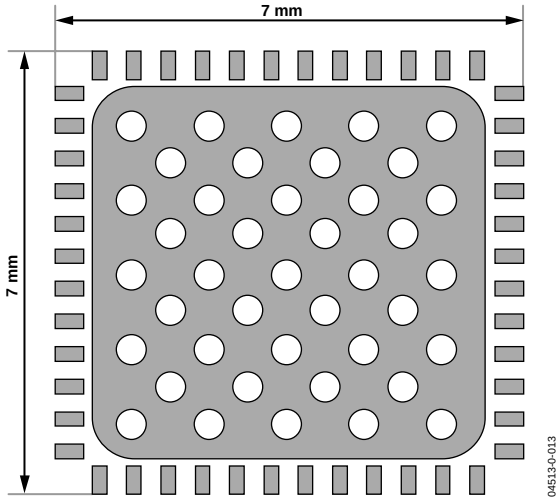


Figure 13. Recommended PCB Landing

The bottom thermal pad forms AVCC plane.

Thermal Pads

Top PCB Layer:	5.25 mm × 5.25 mm
Bottom PCB Layer:	5.25 mm × 5.25 mm

Thermal via structure

Diameter:	0.25 mm
Number of vias:	41
Via Grid Pitch:	0.5 mm

Miscellaneous

Perimeter Pads:	0.5 mm × 0.25 mm
Solder Mask Swell:	0.02 mm

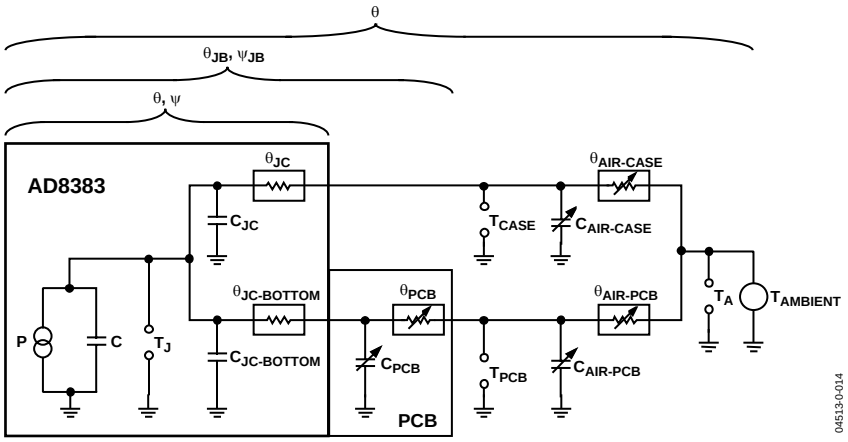


Figure 14. Thermal Equivalent Circuit

ESTIMATED JUNCTION TEMPERATURE

Assuming no heat flows through the sides of the AD8383 package, heat flow from the AD8383 is through two paths. While part of the total heat generated dissipates through the top of the case, the remainder flows into the PCB to be dissipated.

Assuming there is no other heat-generating component near the AD8383, the thermal equivalent circuit of a system that consists of one AD8383 mounted on a PCB is shown in Figure 14.

The thermal resistance of the top of the case, θ_{JC}, is constant, independent of the system variables, and well defined. θ_{JC} depends on the thermal resistance of the molding compound.

The thermal resistance of the system, θ_{JA}, is system dependent and therefore cannot be properly estimated. Although it is traditional to provide the thermal resistance of a JEDEC reference system in the data sheet, its value may not be appropriate for all systems and may result in large errors (>>25%).

The thermal resistance of production PCBs, θ_{JC}, depends largely on the particular PCB design, and, to some extent, the environmental conditions specific to the particular system. Although θ_{JB} is traditionally not provided on data sheets, a thermal characterization parameter, ψ_{JB}, of a JEDEC reference system is gaining increasing acceptance. When the PCB thermal design near the AD8383 closely approximates the PCB of the JEDEC reference system, θ_{JA} approaches ψ_{JB}.

For thermally enhanced packages, the thermal resistance of the exposed thermal paddle, $\theta_{JC\text{-}BOTTOM}$, is very low and may therefore be ignored.

Junction Temperature and Maximum Power Dissipation

In a thermal steady state represented by the simplified schematic shown in Figure 15, heat flow from the die is partly through the top of the case, causing a temperature drop ($T_J - T_{CASE}$), and partly through the PCB, causing a temperature drop ($T_J - T_{PCB}$). The junction temperature is calculated as follows:

$$P = P_{CASE} + P_{PCB} = \frac{(T_J - T_{CASE})}{\theta_{JC}} + \frac{(T_J - T_{PCB})}{\theta_{PCB}}$$

$$T_J = \frac{\theta_{JC}\theta_{PCB}P + \theta_{PCB}T_{CASE} + \theta_{JC}T_{PCB}}{\theta_{JC} + \theta_{PCB}}$$

where:

T_J is the junction temperature
T_{CASE} is the temperature of the top of the case (near the output pins for the AD8383)
T_{PCB} is the PCB temperature on the solder side (directly under the AD8383)
P is the total power dissipated by the AD8383
θ_{JC} is the thermal resistance of the top of the case
θ_{PCB} is the thermal resistance of the PCB

At a given maximum allowed junction temperature, the maximum allowed power dissipation is

$$P_{MAX} = \left[\frac{(\theta_{JC} + \theta_{PCB})}{\theta_{JC}\theta_{PCB}}T_{JMAX} - \frac{T_{CASE}}{\theta_{JC}} - \frac{T_{PCB}}{\theta_{PCB}}\right]$$

For a thermally optimized PCB, θ_{JC} can be replaced with ψ_{PCB} and the equation can be rewritten as

$$P_{MAX} = \left[\frac{(\theta_{JC} + \psi_{PCB})}{\theta_{JC}\psi_{PCB}}T_{JMAX} - \frac{T_{CASE}}{\theta_{JC}} - \frac{T_{PCB}}{\psi_{PCB}}\right]$$

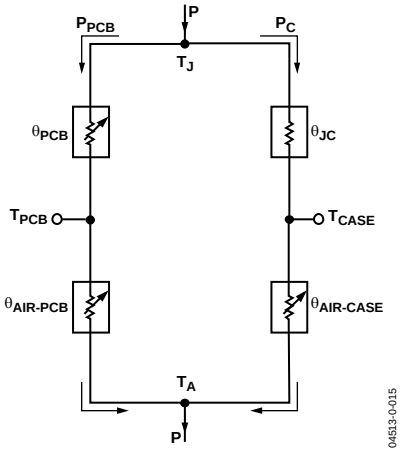


Figure 15. Simplified Thermal Equivalent Circuit

Verification of the Maximum Operating Junction Temperature

In order to verify the system thermal design for compliance with the maximum operating junction temperature specification, temperature measurements T_{CASE} and T_{PCB} are required at the maximum possible total power dissipation in a complete, fully assembled LCD projection system.

Maximum possible total power dissipation of the AD8383 occurs when the video input to the projector is a pattern with 1-pixel-wide white and black vertical lines. An alternative pattern that results in the maximum possible total power dissipation is a 1-pixel checkerboard pattern. The expected total power dissipation of the AD8383 in a 60 Hz, 6-channel XGA projector displaying the 1-pixel-wide vertical line or checkerboard pattern is 1.08 W (at AVCC = 15.5 V, VCOM = 7 V, and LCD capacitance = 150 pF).

Although the case and PCB temperatures are highly dependent on the PCB design, their measured values are expected to be similar at approximately 40°C above the ambient (on a typical PCB with a minimal airflow whose thermal design follows the recommendations described in this note). The junction temperature then calculates to approximately 10°C above the case and PCB temperatures. At a 70°C ambient temperature, the junction temperature is expected to be at approximately 120°C.

The AD8383 has a relatively small thermal mass. In order to minimize measurement errors due to the thermal mass of the measuring device, a small-gauge thermocouple or a thermal probe with a very small thermal mass is required for the measurement of T_{CASE} and T_{PCB}.

Power-Up and Power-Down Sequencing

As indicated in the Absolute Maximum Ratings, the voltage at any input pin cannot exceed its supply voltage by more than 0.5 V. To ensure compliance with the Absolute Maximum Ratings, power-up and power-down sequencing may be required.

During power-up, initial application of nonzero voltages to any of the input pins must be delayed until the supply voltage ramps up to at least the highest maximum operational input voltage.

During power-down, the voltage at any input pin must reach zero during a period not exceeding the hold-up time of the power supply.

Failure to comply with the Absolute Maximum Ratings may result in functional failure or damage to the internal ESD diodes.

Damaged ESD diodes may cause temporary parametric failures, which may result in image artifacts. Damaged ESD diodes cannot provide full ESD protection, thus reducing reliability.

The recommended sequence is

Power ON

1. Apply power to supplies.
2. Apply power to other I/Os.

Power OFF

1. Remove power from I/Os.
2. Remove power from supplies.

VBIAS Generation—V1, V2 Input Pin Functionality

In order to avoid image flicker, a bias voltage of approximately 1 V minimum must be maintained across the pixels of HTPS LCDs. The AD8383 provides two methods of maintaining this bias voltage.

Internal Bias Voltage Generation

Standard systems that internally generate the bias voltage reserve the upper-most code range for the bias voltage and use the remaining code range to encode the video for gamma correction.

OUTLINE DIMENSIONS

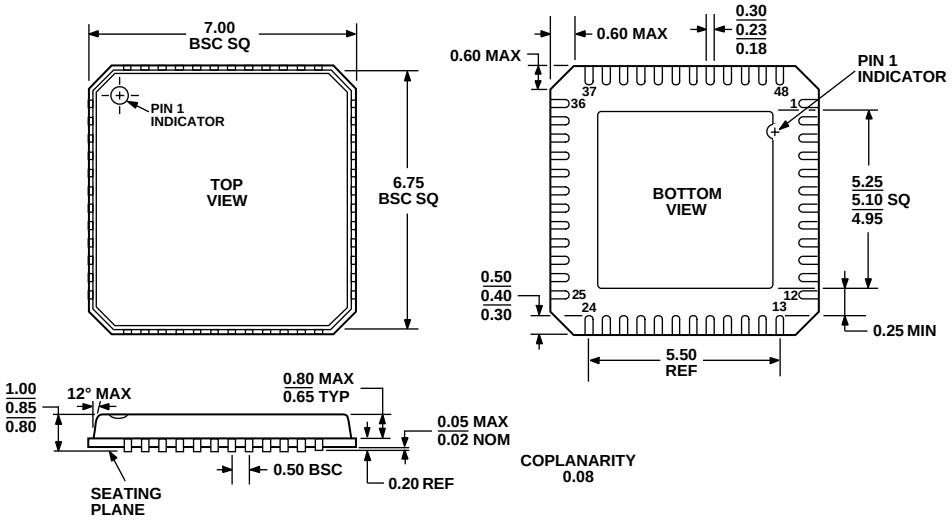


Figure 16. 48-Lead Frame Chip Scale Package [LFCSP]
(CP-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8383ACPZ[9]	0°C to 85°C	48-Lead LFCSP	CP-48

[9] Z = Pb-free part.

NOTES

NOTES

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D03191–0–1/04(0)

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