

## Current Mode Control

### Internal 1.8A MOSFET Switching Regulator IC for Buck Converter

#### ■ GENERAL DESCRIPTION

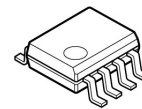
The **NJW4155** is a buck converter with **40V/1.8A** MOSFET. It corresponds to high oscillating frequency, and Low ESR Output Capacitor (MLCC) within wide input range from 4.5V to 40V.

Therefore, the **NJW4155** can realize downsizing of applications with a few external parts so that adopts current mode control.

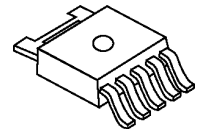
Also, it has a soft start function, external clock synchronization, over current protection and thermal shutdown circuit.

It is suitable for supplying power to a Car Accessory, Office Automation Equipment, Industrial Instrument and so on.

#### ■ PACKAGE OUTLINE



**NJW4155GM1**



**NJW4155DL3**

#### ■ FEATURES

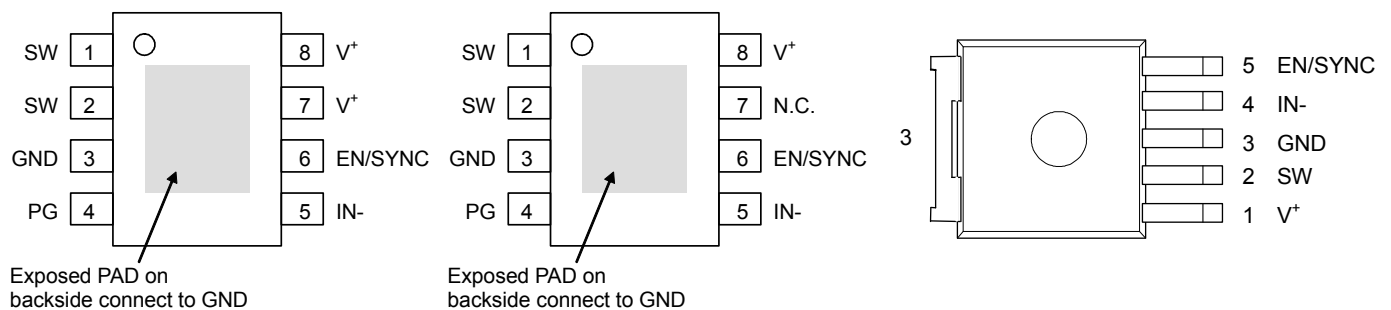
- Current Mode Control
- External Clock Synchronization
- Wide Operating Voltage Range      4.5V to 40V
- Switching Current                      2.7A min.
- PWM Control
- Built-in Compensation Circuit
- Correspond to Ceramic Capacitor (MLCC)
- Oscillating Frequency                450kHz typ. (A, C ver.)  
    300kHz typ. (B ver.)
- Soft Start Function                      4ms typ.
- UVLO (Under Voltage Lockout)
- Over Current Protection (Hiccup type)
- Thermal Shutdown Protection
- Power Good Function (NJW4155GM1 only)
- Standby Function
- Package Outline                         NJW4155GM1 : HSOP8  
    NJW4155DL3 : TO-252-5

# NJW4155

## ■ PRODUCT CLASSIFICATION

Part Number	Version	Oscillation Frequency	Power Good	Package	Operating Temperature Range
NJW4155GM1-A	A	450kHz typ.	√	HSOP8	General Spec. Ta=-40°C to +125°C
NJW4155GM1-B	B	300kHz typ.	√	HSOP8	General Spec. Ta=-40°C to +125°C
NJW4155DL3-B	B	300kHz typ.		TO-252-5	General Spec. Ta=-40°C to +125°C
NJW4155GM1-C	C	450kHz typ.	√	HSOP8 (7pin: N.C.)	General Spec. Ta=-40°C to +125°C

## ■ PIN CONFIGURATION



**NJW4155GM1-A**  
**NJW4155GM1-B**

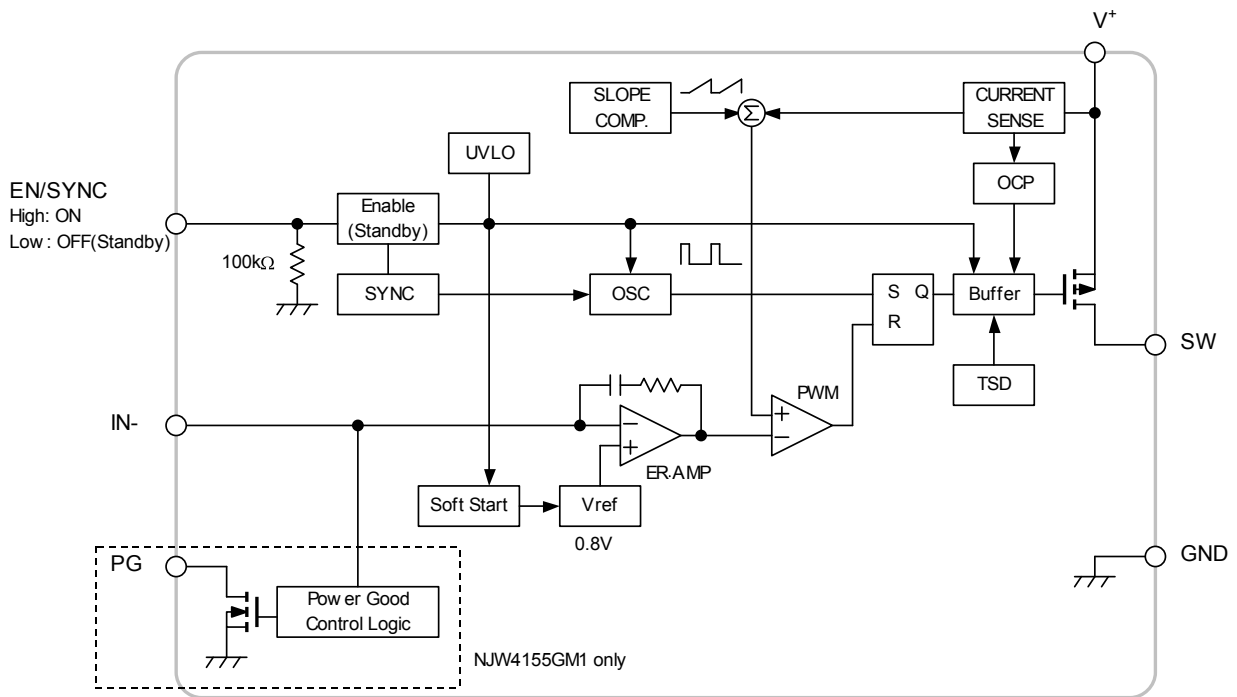
**NJW4155GM1-C**

**NJW4155DL3-B**

## ■ PIN DESCRIPTIONS

PIN NAME	PIN NUMBER			FUNCTION
	HSOP8	HSOP8	TO-252-5	
	A ver. B ver.	C ver.	B ver.	
SW	1 2	1 2	2	Switch Output pin of Power MOSFET
GND	3	3	3	GND pin
PG	4	4	—	Power Good pin. An open drain output that goes high impedance when the IN- pin voltage is stable around $\pm 10\%$ . (Only HSOP8 PKG)
IN-	5	5	4	Output Voltage Detecting pin Connects output voltage through the resistor divider tap to this pin in order to voltage of the IN- pin become 0.8V.
EN/SYNC	6	6	5	Standby Control pin The EN/SYNC pin internally pulls down with 100k $\Omega$ . Normal Operation at the time of High Level. Standby Mode at the time of Low Level or OPEN. Moreover, it operates by inputting clock signal at the oscillatory frequency that synchronized with the input signal.
N.C.	—	7	—	Non Connection
V <sup>+</sup>	7 8	8	1	Power Supply pin for Power Line
Exposed PAD	—	—	—	Connect to GND (Only HSOP8 PKG)

## ■ BLOCK DIAGRAM



# NJW4155

## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT
Supply Voltage	V <sup>+</sup>	-0.3~+45	V
V <sup>+</sup> - SW pin Voltage	V <sub>V-SW</sub>	+45	V
EN/SYNC pin Voltage	V <sub>EN/SYNC</sub>	-0.3~+45	V
IN- pin Voltage	V <sub>IN-</sub>	-0.3~+6	V
Power Good pin Voltage (*1)	V <sub>PG</sub>	-0.3~+6	V
Power Dissipation	P <sub>D</sub>	HSOP8	790 (*2) 2,500 (*3)
		TO-252-5	1,190 (*4) 3,125 (*3)
Junction Temperature Range	T <sub>J</sub>	-40 to +150	°C
Operating Temperature Range	T <sub>opr</sub>	-40 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-50 to +150	°C

(\*1): Apply only the NJW4155GM1.

(\*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(\*3): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

(\*4): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard size, 2Layers, Cu area 100mm<sup>2</sup>)

## ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V <sup>+</sup>	4.5	—	40	V
Power Good pin Voltage (*5)	V <sub>PG</sub>	0	—	5.5	V
External Clock Input Range	f <sub>SYNC</sub>	A, C version	—	600	kHz
		B version	280	500	

(\*5): Apply only the NJW4155GM1.

## ■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted,  $V^+ = V_{EN/SYNC} = 12V$ ,  $T_a = 25^\circ C$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
<b>Under Voltage Lockout Block</b>						
ON Threshold Voltage	$V_{T\_ON}$	$V^+ = L \rightarrow H$	4.2	4.4	4.5	V
OFF Threshold Voltage	$V_{T\_OFF}$	$V^+ = H \rightarrow L$	4.1	4.3	4.4	V
Hysteresis Voltage	$V_{HYS}$		70	90	–	mV
<b>Soft Start Block</b>						
Soft Start Time	$T_{SS}$	$V_B = 0.75V$	2	4	8	ms
<b>Oscillator Block</b>						
Oscillation Frequency	$f_{OSC}$	A, C version, $V_{IN} = 0.7V$	405	450	495	kHz
		B version, $V_{IN} = 0.7V$	270	300	330	kHz
Oscillation Frequency deviation (Supply voltage)	$f_{DV}$	$V^+ = 4.5V$ to $40V$	–	1	–	%
Oscillation Frequency deviation (Temperature)	$f_{DT}$	$T_a = -40^\circ C$ to $+85^\circ C$	–	5	–	%
<b>Error Amplifier Block</b>						
Reference Voltage	$V_B$		-1.0%	0.8	+1.0%	V
Input Bias Current	$I_B$		-0.1	–	+0.1	$\mu A$
<b>PWM Compare Block</b>						
Maximum Duty Cycle	$M_{AXDUTY}$	$V_{IN} = 0.7V$	92	95.5	–	%
Minimum ON Time1 (Use Built-in Oscillator)	$t_{ON-min1}$	A, C version	–	150	200	ns
		B version	–	215	290	ns
Minimum ON Time2 (Use Ext CLK)	$t_{ON-min2}$	A, C version, $f_{SYNC} = 500kHz$	–	100	140	ns
		B version, $f_{SYNC} = 400kHz$	–	145	200	ns
<b>OCP Block</b>						
COOL DOWN Time	$t_{COOL}$		–	75	–	ms
<b>Output Block</b>						
Output ON Resistance	$R_{ON}$	$I_{SW} = 1.5A$	–	0.2	0.4	$\Omega$
Switching Current Limit	$I_{LIM}$		2.7	3.4	4.0	A
SW Leak Current	$I_{LEAK}$	$V_{EN/SYNC} = 0V$ , $V^+ = 45V$ , $V_{SW} = 0V$	–	–	3	$\mu A$

# NJW4155

## ■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted,  $V^+ = V_{EN/SYNC} = 12V$ ,  $T_a = 25^\circ C$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
<b>Standby Control / Sync Block</b>						
EN/SYNC pin High Threshold Voltage	$V_{THH\_EN/SYNC}$	$V_{EN/SYNC} = L \rightarrow H$	1.6	–	$V^+$	V
EN/SYNC pin Low Threshold Voltage	$V_{THL\_EN/SYNC}$	$V_{EN/SYNC} = H \rightarrow L$	0	–	0.5	V
Input Bias Current (EN/SYNC pin)	$I_{EN}$	$V_{EN/SYNC} = 12V$	–	170	250	$\mu A$
<b>Power Good Block (*6)</b>						
High Level Detection Voltage	$V_{THH\_PG}$	Measured at IN- pin	105	110	115	%
Low Level Detection Voltage	$V_{THL\_PG}$	Measured at IN- pin	85	90	95	%
Hysteresis Region	$V_{HYS\_PG}$		–	2	–	%
Power Good ON Resistance	$R_{ON\_PG}$	$I_{PG} = 10mA$	–	37	50	$\Omega$
Leak Current at OFF State	$I_{LEAK\_PG}$	$V_{PG} = 6V$	–	–	0.1	$\mu A$
<b>General Characteristics</b>						
Quiescent Current	$I_{DD}$	A, C version, $R_L = \text{no load}, V_{IN} = 0.7V$	–	3.5	4.2	mA
		B version, $R_L = \text{no load}, V_{IN} = 0.7V$	–	3.0	3.6	mA
Standby Current	$I_{DD\_STB}$	$V_{EN/SYNC} = 0V$	–	–	3	$\mu A$

(\*6): Apply only the NJW4155GM1.

## ■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE		UNIT
Junction-to-ambient thermal resistance	$\theta_{ja}$	HSOP8	158 (*7) 50 (*8)	°C/W
		TO-252-5	105 (*9) 40 (*8)	
Junction-to-Top of package characterization parameter	$\psi_{jt}$	HSOP8	28 (*7) 12 (*8)	°C/W
		TO-252-5	17 (*9) 12 (*8)	

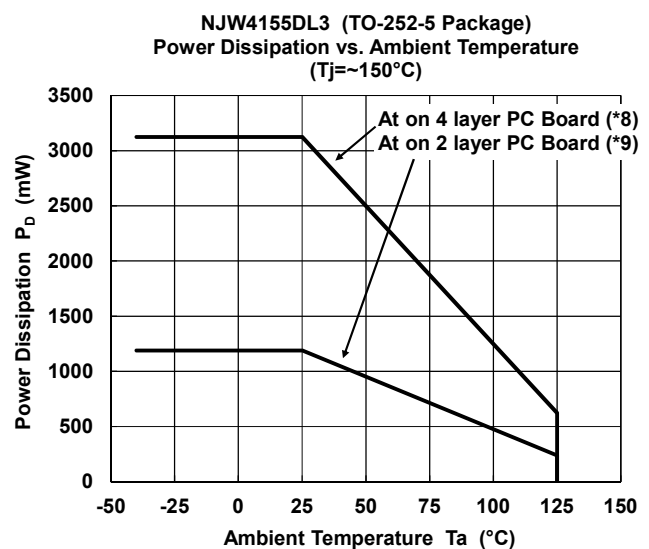
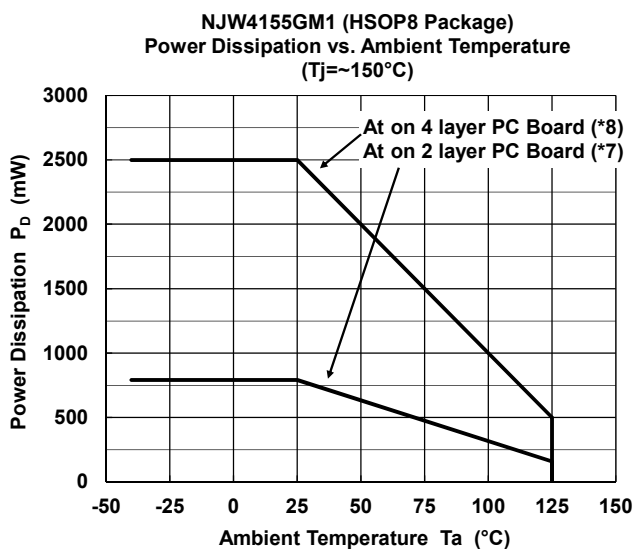
(\*7): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(\*8): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

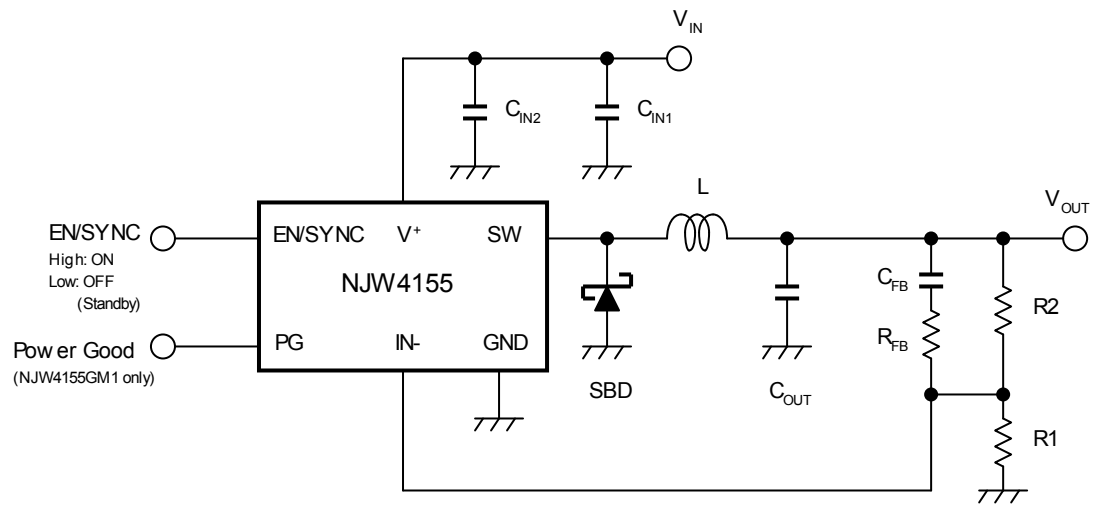
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## ■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



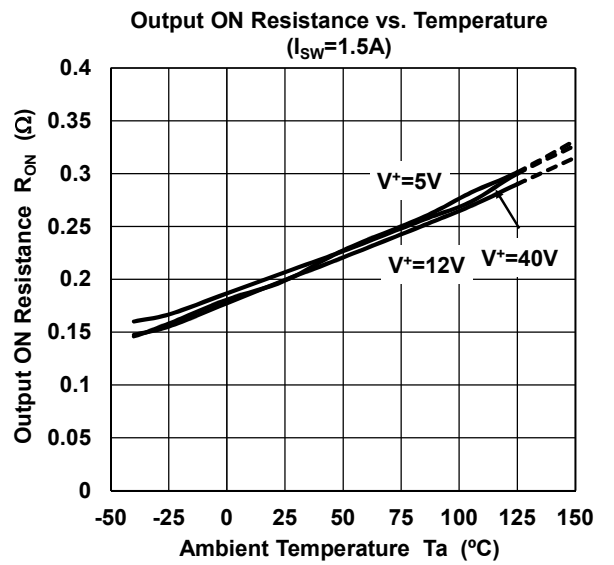
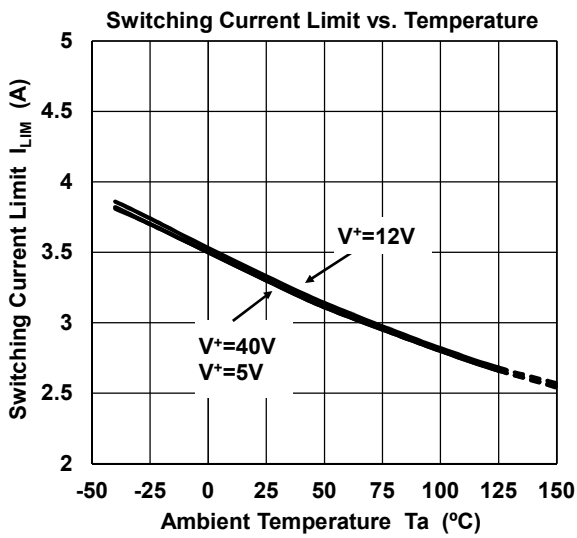
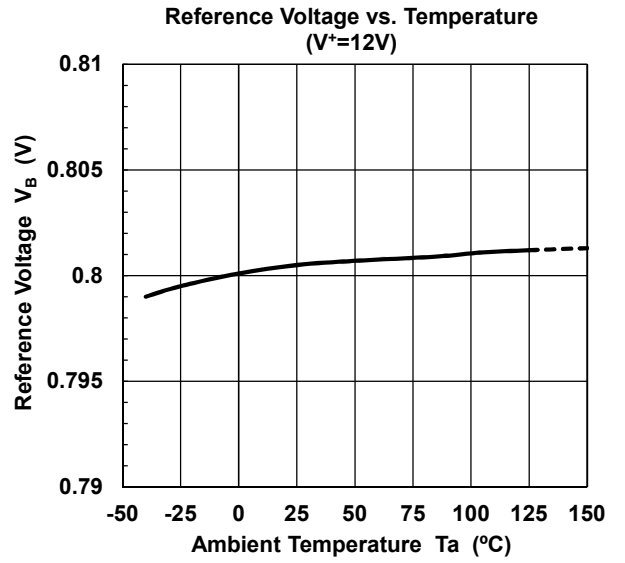
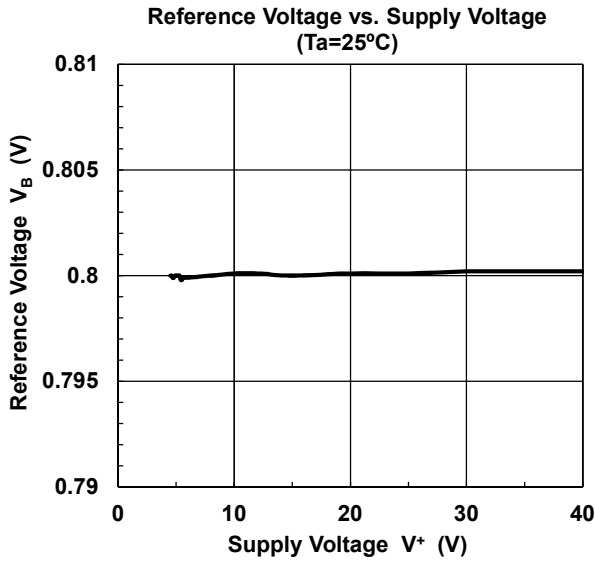
# NJW4155

## ■ TYPICAL APPLICATIONS

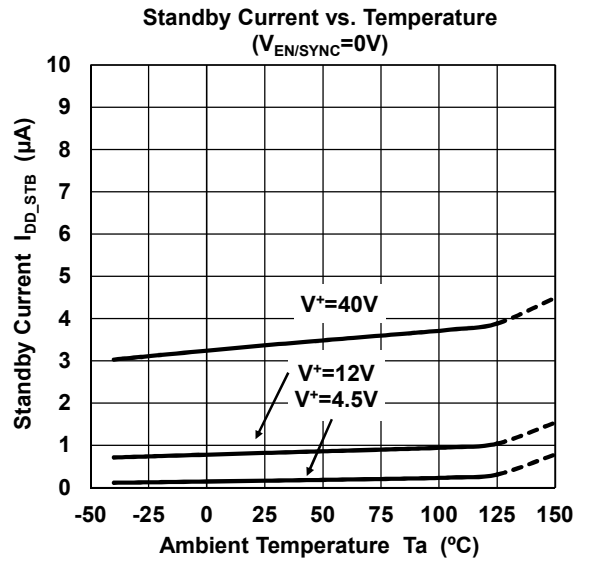
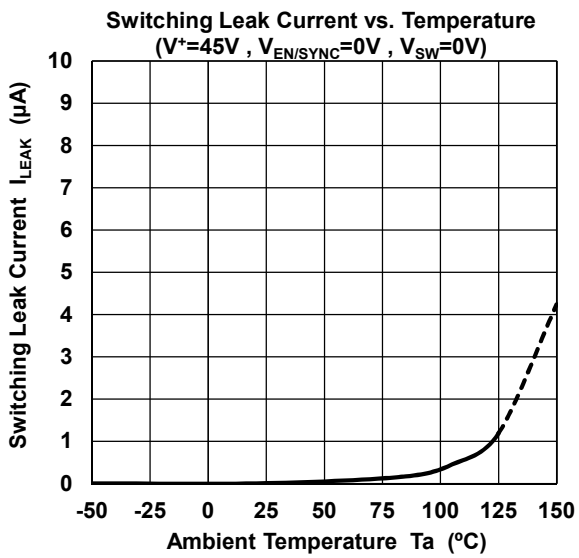
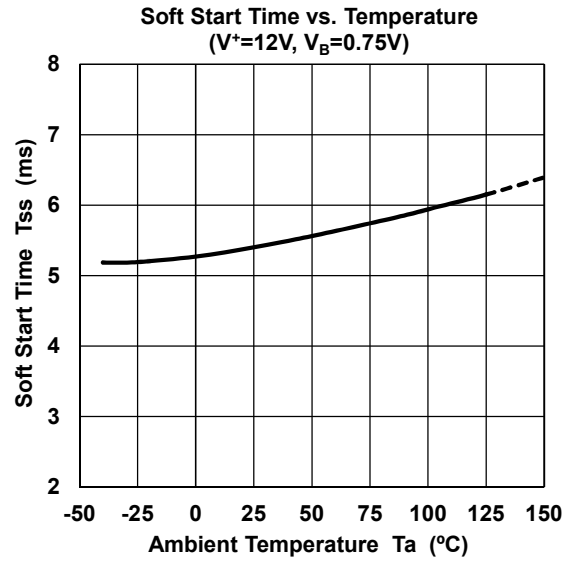
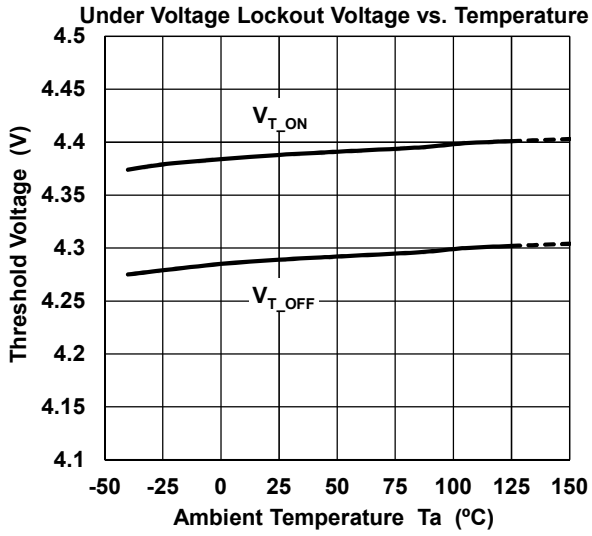




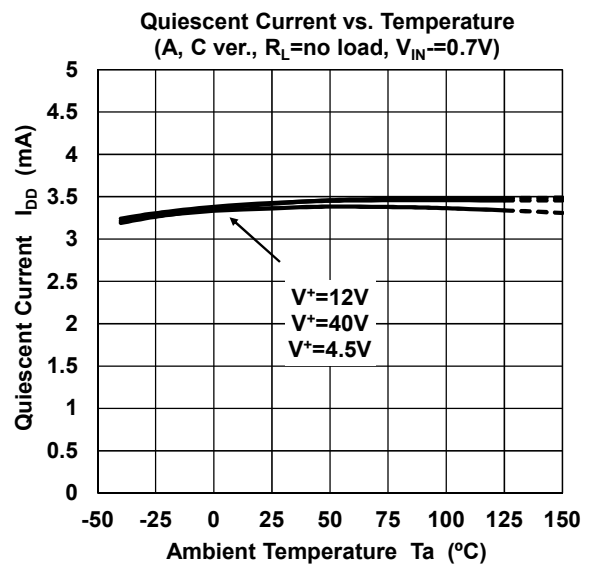
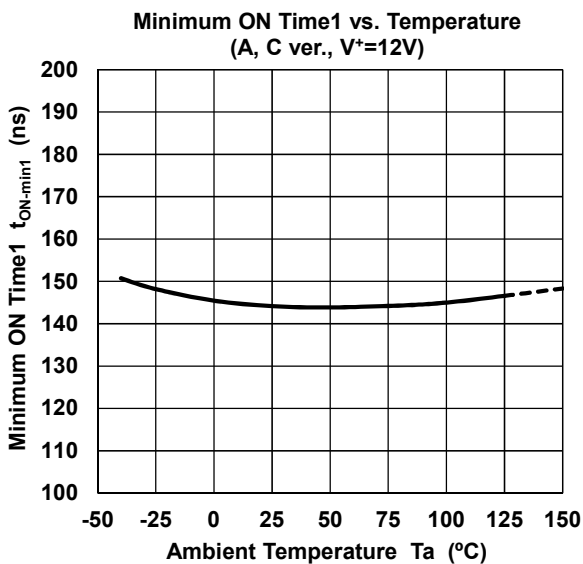
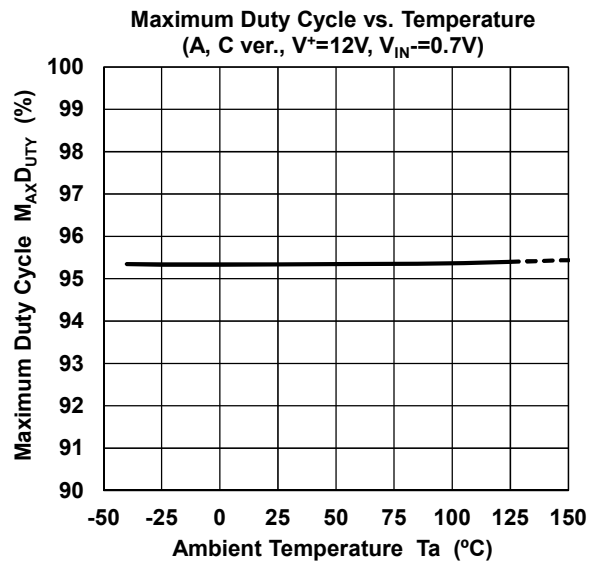
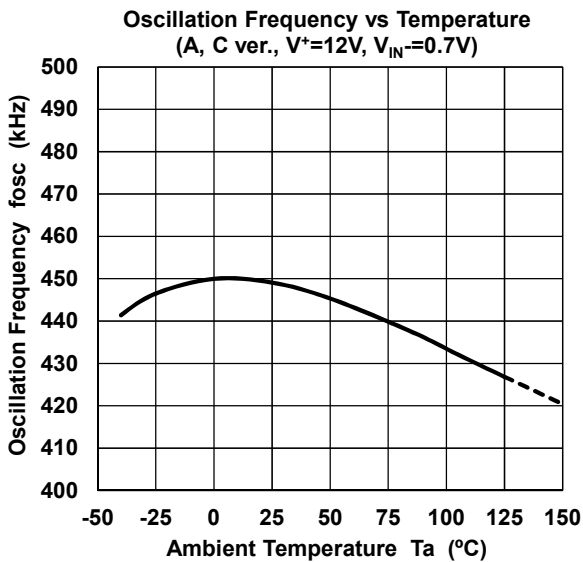
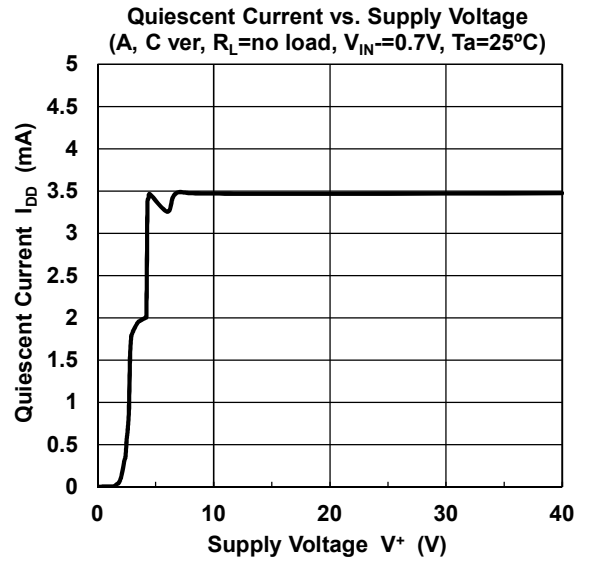
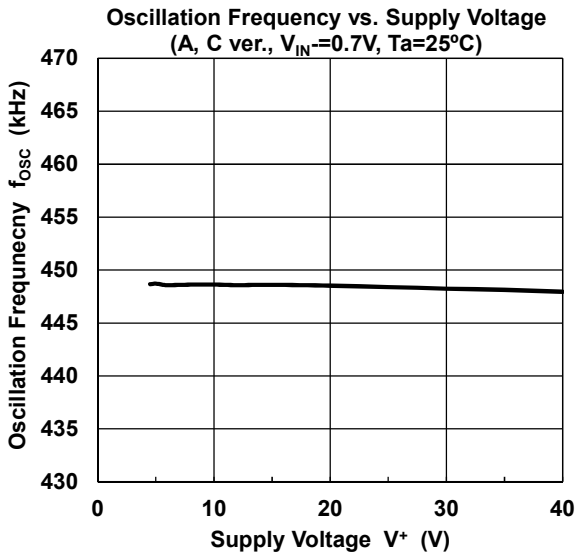
■ TYPICAL CHARACTERISTICS (A, B, C version)



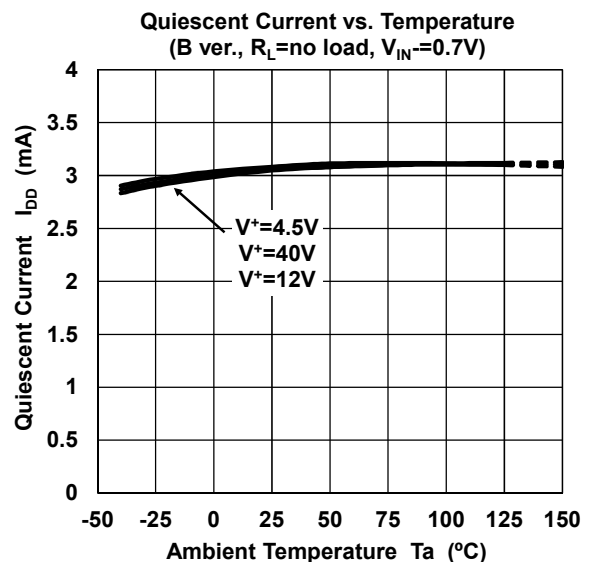
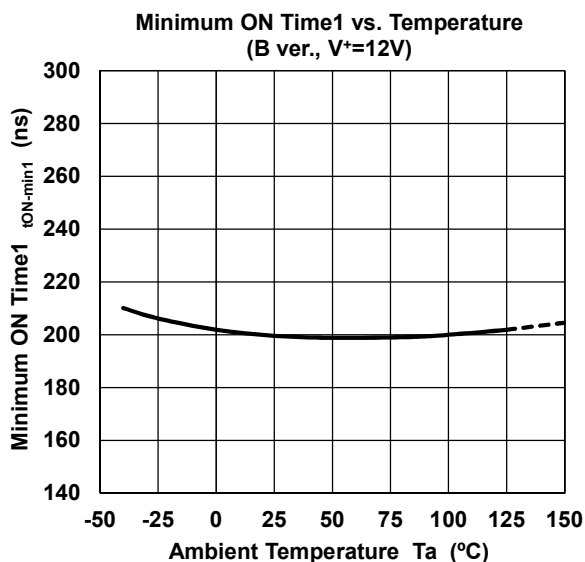
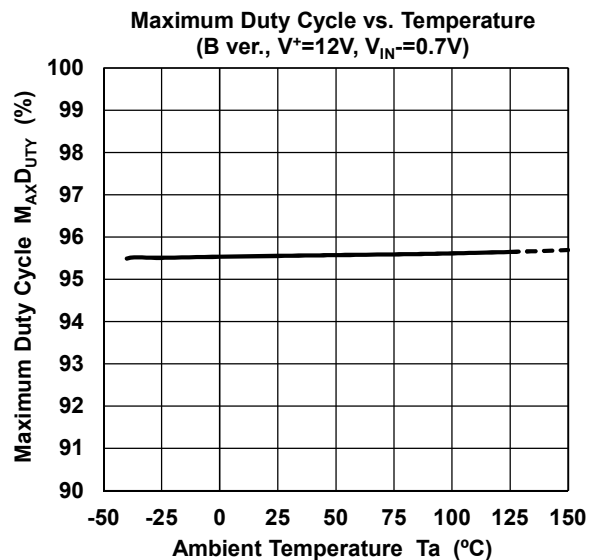
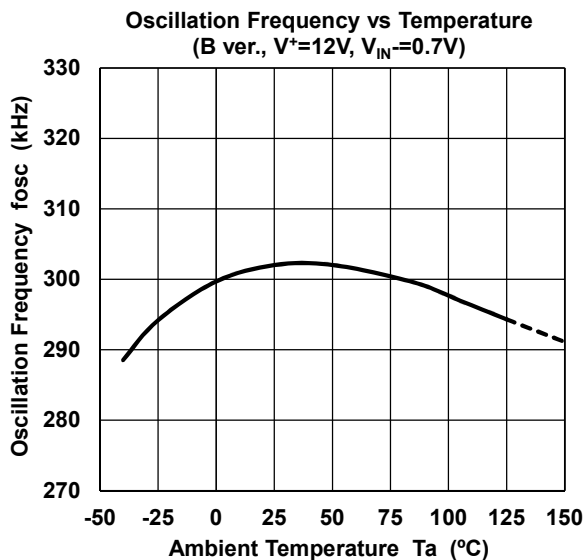
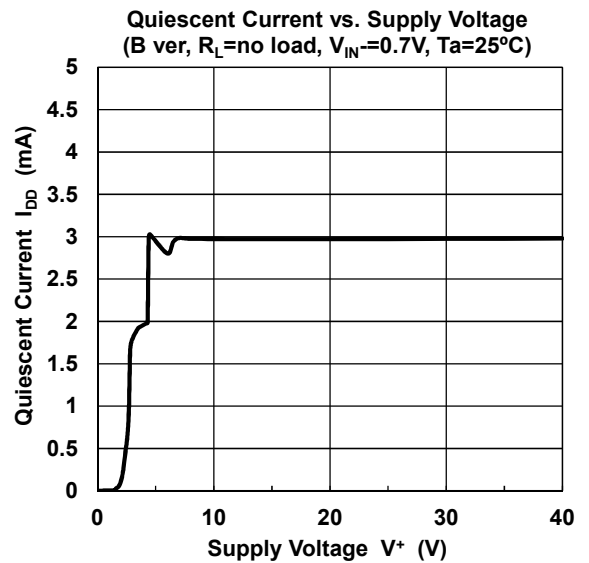
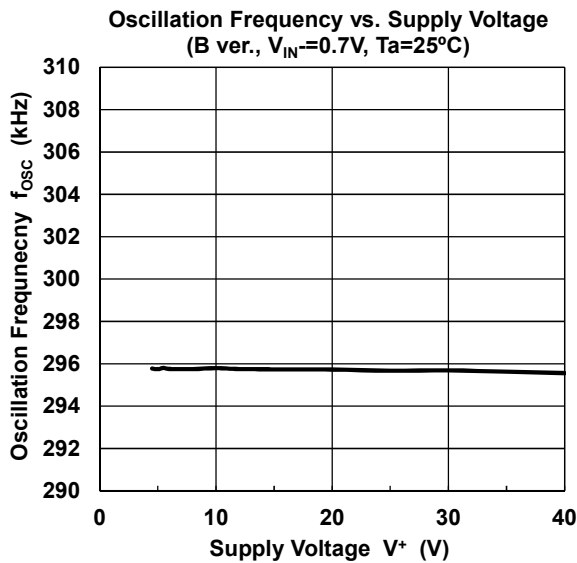
## ■ TYPICAL CHARACTERISTICS (A, B, C version)



## ■ TYPICAL CHARACTERISTICS (A, C version)



## ■ TYPICAL CHARACTERISTICS (B version)



### ■ Description of Block Features

#### 1. Basic Functions / Features

- Error Amplifier Section (ER-AMP)

0.8V±1% precise reference voltage is connected to the non-inverted input of this section.

To set the output voltage, connects converter's output to inverted input of this section (IN- pin). If requires output voltage over 0.8V, inserts resistor divider.

Because the optimized compensation circuit is built-in, the application circuit can be composed of minimum external parts.

- PWM Comparator Section (PWM), Oscillation Circuit Section (OSC)

The NJW4155 uses a constant frequency, current mode step down architecture. The oscillation frequency is 450kHz (typ.) at A, C version and 300kHz (typ.) at B version. The PWM signal is output by feedback of output voltage and slope compensation switching current at the PWM comparator block.

The maximum duty ratio is 95.5% (typ.).

Table 1. Minimum ON time of NJW4155

	A, C version ( $f_{OSC}=450\text{kHz}$ )	B version ( $f_{OSC}=300\text{kHz}$ )
Use Built-in Oscillator	150ns typ.	215ns typ.
Use External Clock	100ns typ. (@ $f_{SYNC}=500\text{kHz}$ )	145ns typ. (@ $f_{SYNC}=400\text{kHz}$ )

The buck converter of ON time is decided the following formula.

$$t_{on} = \frac{V_{OUT}}{V_{IN} \times f_{OSC}} \text{ [s]}$$

$V_{IN}$  shows input voltage and  $V_{OUT}$  shows output voltage.

When the ON time becomes below in  $t_{ON-min}$ , in order to maintain output voltage at a stable state, change of duty or pulse skip operation may be performed.

- Power MOSFET (SW Output Section)

The power is stored in the inductor by the switch operation of built-in power MOSFET. The output current is limited to 2.7A(min.) the overcurrent protection function. In case of step-down converter, the forward direction bias voltage is generated with inductance current that flows into the external regenerative diode when MOSFET is turned off.

The SW pin allows voltage between the  $V^+$  pin and the SW pin up to +45V. However, you should use an Schottky diode that has low saturation voltage.

- Power Supply, GND pin ( $V^+$  and GND)

In line with switching element drive, current flows into the IC according to frequency. If the power supply impedance provided to the power supply circuit is high, it will not be possible to take advantage of IC performance due to input voltage fluctuation. Therefore insert a bypass capacitor close to the  $V^+$  pin – the GND pin connection in order to lower high frequency impedance.

### ■ Description of Block Features (Continued)

#### 2. Additional and Protection Functions / Features

##### ● Under Voltage Lockout (UVLO)

The UVLO circuit operating is released above  $V^+ = 4.4V$  (typ.) and IC operation starts. When power supply voltage is low, IC does not operate because the UVLO circuit operates. There is 90mV (typ.) width hysteresis voltage at rise and decay of power supply voltage. Hysteresis prevents the malfunction at the time of UVLO operating and releasing.

##### ● Soft Start Function (Soft Start)

The output voltage of the converter gradually rises to a set value by the soft start function. The soft start time is 4ms (typ.). It is defined with the time of the error amplifier reference voltage becoming from 0V to 0.75V. The soft start circuit operates after the release UVLO and/or recovery from thermal shutdown.

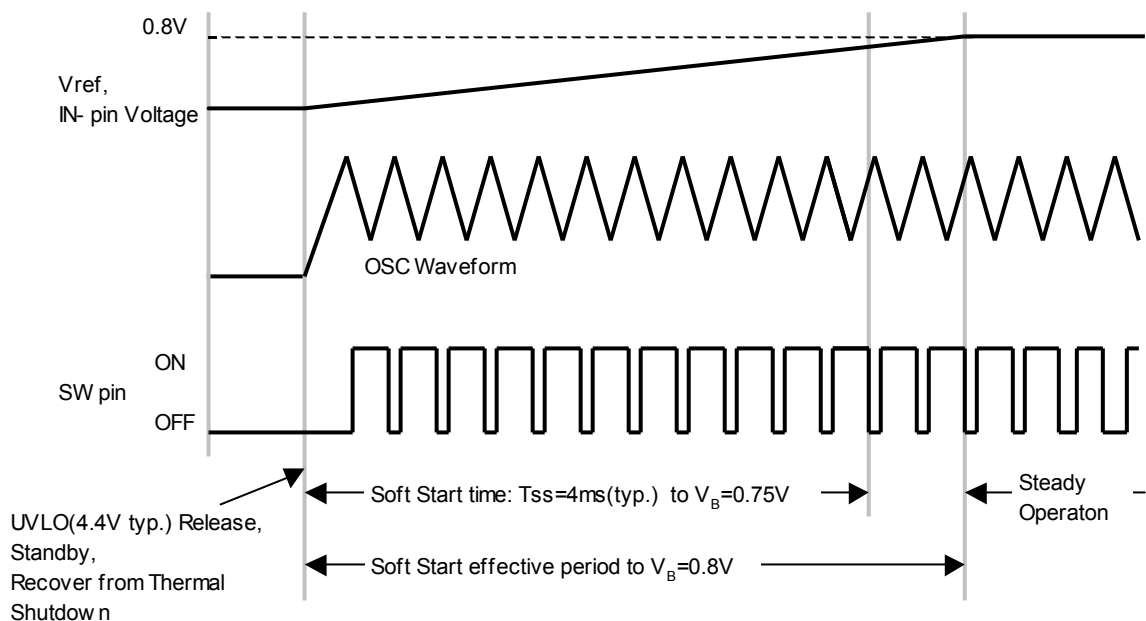


Fig. 1. Startup Timing Chart

### ■ Description of Block Features (Continued)

#### ● Over Current Protection Circuit (OCP)

NJW4155 contains overcurrent protection circuit of hiccup architecture. The overcurrent protection circuit of hiccup architecture is able to decrease heat generation at the overload.

The NJW4155 output returns automatically along with release from the over current condition.

At when the switching current becomes  $I_{LIM}$  or more, the overcurrent protection circuit is stopped the MOSFET output. The switching output holds low level down to next pulse output at OCP operating.

When the IN- pin voltage is 0.5V or lower(less), the switching operation stops after the overcurrent detection continued 128 pulses.

After NJW4155 switching operation was stopped, it restarts by soft start function after the cool down time of approx 75ms (typ.).

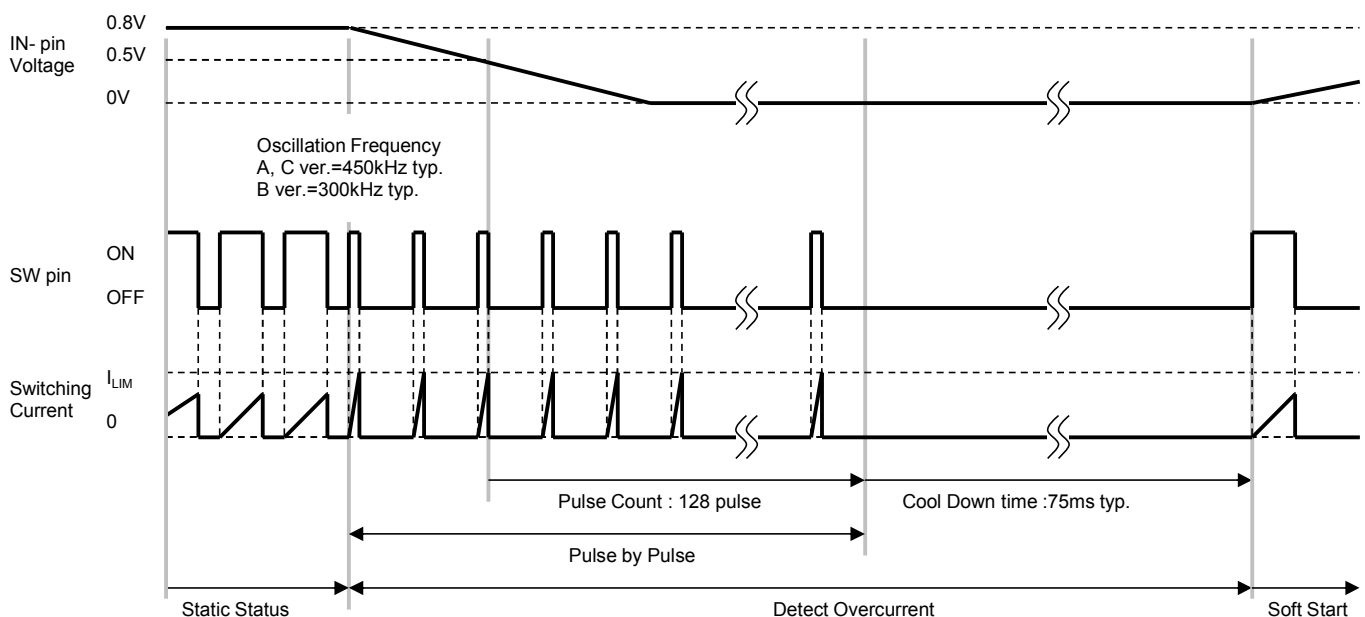


Fig. 2. Timing Chart at Over Current Detection

#### ● Thermal Shutdown Function (TSD)

When Junction temperature of the NJW4155 exceeds the  $160^{\circ}\text{C}^*$ , internal thermal shutdown circuit function stops SW function. When junction temperature decreases to  $145^{\circ}\text{C}^*$  or less, SW operation returns with soft start operation.

The purpose of this function is to prevent malfunctioning of IC at the high junction temperature. Therefore it is not something that urges positive use. You should make sure to operate within the junction temperature range rated ( $150^{\circ}\text{C}$ ). (\* Design value)

#### ● Standby Function

The NJW4155 stops the operating and becomes standby status when the EN/SYNC pin becomes less than 0.5V.

The EN/SYNC pin internally pulls down with  $100\text{k}\Omega$ , therefore the NJW4155 becomes standby mode when the EN/SYNC pin is OPEN. You should connect this pin to  $V^+$  when you do not use standby function.

### ■ Description of Block Features (Continued)

#### ● External Clock Synchronization

By inputting a square wave to EN/SYNC pin, can be synchronized to an external frequency.

You should fulfill the following specification about a square wave. (Table 2.)

Table 2. The input square wave to an EN/SYNC pin.

	A, C version ( $f_{OSC} = 450\text{kHz}$ )	B version ( $f_{OSC} = 300\text{kHz}$ )
Input Frequency	440kHz to 600kHz	280kHz to 500kHz
Duty Cycle	25% to 75%	20% to 80%
Voltage magnitude	1.6V or more at High level 0.5V or less at Low level	

The trigger of the switching operating at the external synchronized mode is detected to the rising edge of the input signal. At the time of switching operation from standby or asynchronous to synchronous operation, it has set a delay time approx  $20\mu\text{s}$  to  $30\mu\text{s}$  in order to prevent malfunctions. (Fig. 3.)

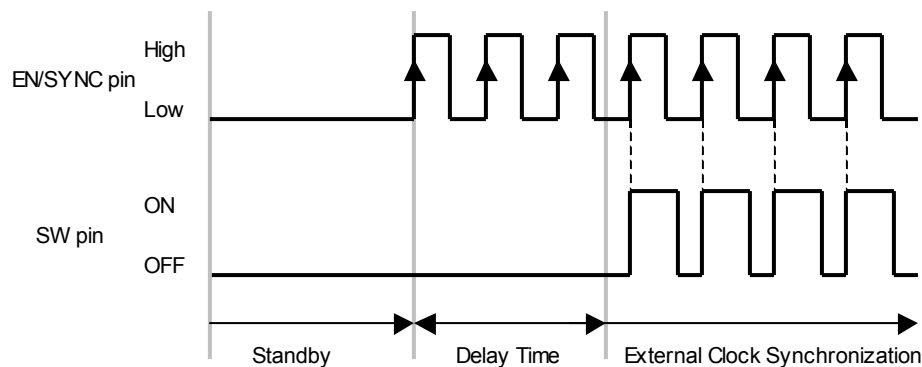


Fig. 3. Switching Operation by External Synchronized Clock

#### ● Power Good Function

It monitors the output status and outputs a signal from PG pin that internally connected to open drain MOSFET.

The Power Good pin goes high impedance when the IN- pin voltage is stable around  $\pm 10\%$ (typ.) of error amplifier reference voltage.

A low on the pin indicates that the IN- pin voltage is out of the setting voltage.

To prevent malfunction of the Power Good output, it has hysteresis  $2\%$ (typ.) and the delay time approx  $20\mu\text{s}$  to  $30\mu\text{s}$  against the IN- pin voltage changes.



### ■ Application Information

#### ● Inductors

Because a large current flows to the inductor, you should select the inductor with the large current capacity not to saturate. Optimized inductor value is determined by the input voltage and output voltage.

The Inductor setting example is shown in Table 3.

Table 3. Inductor Setting Example

Input Voltage $V_{IN}$	Output Voltage $V_{OUT}$	Inductor L	
		A, C version ( $f_{OSC} = 450\text{kHz}$ )	B version ( $f_{OSC} = 300\text{kHz}$ )
12V	3.3V	$\leq 27\mu\text{H}$	$\leq 39\mu\text{H}$
	5.0V	$\leq 33\mu\text{H}$	$\leq 47\mu\text{H}$
	8.0V	$\leq 33\mu\text{H}$	$\leq 47\mu\text{H}$
24V	3.3V	$\leq 39\mu\text{H}$	$\leq 47\mu\text{H}$
	5.0V	$\leq 47\mu\text{H}$	$\leq 56\mu\text{H}$
	8.0V	$\leq 47\mu\text{H}$	$\leq 56\mu\text{H}$

When increasing inductor value, it is necessary to increasing capacity of an output capacitor and to secure the stability of application. The minimum of inductor value is restricted from the following formula, when ON duty exceeds 50%.

$$\text{A, C version } L \geq \frac{V_{IN} \times (2 \times D_{ON} - 1)}{1.11} [\mu\text{H}]$$

$$\text{B version } L \geq \frac{V_{IN} \times (2 \times D_{ON} - 1)}{0.74} [\mu\text{H}]$$

Reducing L decreases the size of the inductor. However a peak current increases and adversely affects the efficiency. (Fig. 4.)

Moreover, you should be aware that the output current is limited because it becomes easy to operating to the overcurrent limit.

The peak current is decided the following formula.

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f_{OSC}} [\text{A}]$$

$$I_{pk} = I_{OUT} + \frac{\Delta I_L}{2} [\text{A}]$$

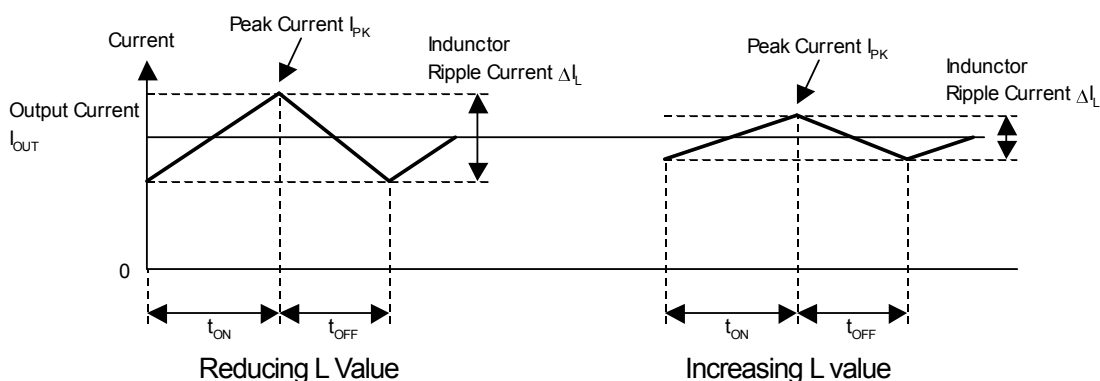


Fig. 4. Inductor Current State Transition (Continuous Conduction Mode)

### ■ Application Information (Continued)

#### ● Input Capacitor

Transient current flows into the input section of a switching regulator responsive to frequency. If the power supply impedance provided to the power supply circuit is large, it will not be possible to take advantage of the NJW4155 performance due to input voltage fluctuation. Therefore insert an input capacitor as close to the MOSFET as possible. A ceramic capacitor is the optimal for input capacitor.

The effective input current can be expressed by the following formula.

$$I_{\text{RMS}} = I_{\text{OUT}} \times \frac{\sqrt{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}}{V_{\text{IN}}} \text{ [A]}$$

In the above formula, the maximum current is obtained when  $V_{\text{IN}} = 2 \times V_{\text{OUT}}$ , and the result in this case is

$$I_{\text{RMS}} = I_{\text{OUT (MAX)}} \div 2.$$

When selecting the input capacitor, carry out an evaluation based on the application, and use a capacitor that has adequate margin.

#### ● Output Capacitor

An output capacitor stores power from the inductor, and stabilizes voltage provided to the output. Because NJW4155 corresponds to the output capacitor of low ESR, the ceramic capacitor is the optimal for compensation. The output capacitor setting example is shown in Table 4.

Table 4. Output Capacitor Setting Example

Input Voltage $V_{\text{IN}}$	Output Voltage $V_{\text{OUT}}$	Capacitor $C_{\text{OUT}}$	Part Number
A, C version			
12V, 24V	3.3V	$\geq 47\mu\text{F} / 6.3\text{V}$	GRM31CB30J476KE18: Murata
	5.0V	$\geq 22\mu\text{F} / 6.3\text{V}$	GRM31CB30J226ME18: Murata
	8.0V	$\geq 22\mu\text{F} / 10\text{V}$	GRM31CR61A226ME19: Murata
B version			
12V, 24V	3.3V	$\geq 47\mu\text{F} / 6.3\text{V} +$ $22\mu\text{F} / 6.3\text{V}$	GRM31CB30J476KE18: Murata GRM31CB30J226ME18: Murata
	5.0V	$\geq 47\mu\text{F} / 6.3\text{V}$	GRM31CB30J476KE18: Murata
	8.0V	$\geq 47\mu\text{F} / 16\text{V}$	GRM32EB31C476KE15: Murata

The output capacitor uses capacity bigger than Table 4.

In addition, you should consider varied characteristics of capacitor (a frequency characteristic, a temperature characteristic, a DC bias characteristic and so on) and unevenness peculiar to a capacitor supplier enough.

Therefore when selecting a capacitors, you should confirm the characteristics with supplier datasheets.

When selecting an output capacitor, you must consider Equivalent Series Resistance (ESR) characteristics, ripple current, and breakdown voltage.

The output ripple noise can be expressed by the following formula.

$$V_{\text{ripple(p-p)}} = \text{ESR} \times \Delta I_{\text{L}} \text{ [V]}$$

The effective ripple current that flows in a capacitor ( $I_{\text{rms}}$ ) is obtained by the following equation.

$$I_{\text{rms}} = \frac{\Delta I_{\text{L}}}{2\sqrt{3}} \text{ [Arms]}$$

### ■ Application Information (Continued)

#### ● Catch Diode

When the switch element is in OFF cycle, power stored in the inductor flows via the catch diode to the output capacitor. Therefore during each cycle current flows to the diode in response to load current. Because diode's forward saturation voltage and current accumulation cause power loss, a Schottky Barrier Diode (SBD), which has a low forward saturation voltage, is ideal.

An SBD also has a short reverse recovery time. If the reverse recovery time is long, through current flows when the switching transistor transitions from OFF cycle to ON cycle. This current may lower efficiency and affect such factors as noise generation.

#### ● Setting Output Voltage, Compensation Capacitor

The output voltage  $V_{OUT}$  is determined by the relative resistances of R1, R2. The current that flows in R1, R2 must be a value that can ignore the bias current that flows in ERAMP.

$$V_{OUT} = \left( \frac{R2}{R1} + 1 \right) \times V_B \text{ [V]}$$

The zero points are formed with R2 and  $C_{FB}$ , and it makes for the phase compensation of NJW4155. The zero point is shown the following formula.

$$f_{z1} = \frac{1}{2 \times \pi \times R2 \times C_{FB}} \text{ [Hz]}$$

You should set the zero point as a guide from 50kHz to 70kHz.

Output voltage setting resistor and compensation capacitor setting example is shown in Table 5.

Table 5. Output Voltage Setting Resistor and Compensation Capacitor Setting Example

Input Voltage $V_{IN}$	Output Voltage $V_{OUT}$	R1	R2	$C_{FB}$
12V, 24V	3.3V	4.7k $\Omega$	15k $\Omega$	180pF
	5.0V	3.0k $\Omega$	16k $\Omega$	150pF
	8.0V	2.2k $\Omega$	20k $\Omega$	120pF

(A version, B version and C version are common.)

### ■ Application Information (Continued)

#### ● Board Layout

In the switching regulator application, because the current flow corresponds to the oscillation frequency, the substrate (PCB) layout becomes an important.

You should attempt the transition voltage decrease by making a current loop area minimize as much as possible. Therefore, you should make a current flowing line thick and short as much as possible. Fig.5. shows a current loop at step-down converter. Especially, should lay out high priority the loop of  $C_{IN}$ -SW-SBD that occurs rapid current change in the switching. It is effective in reducing noise spikes caused by parasitic inductance.

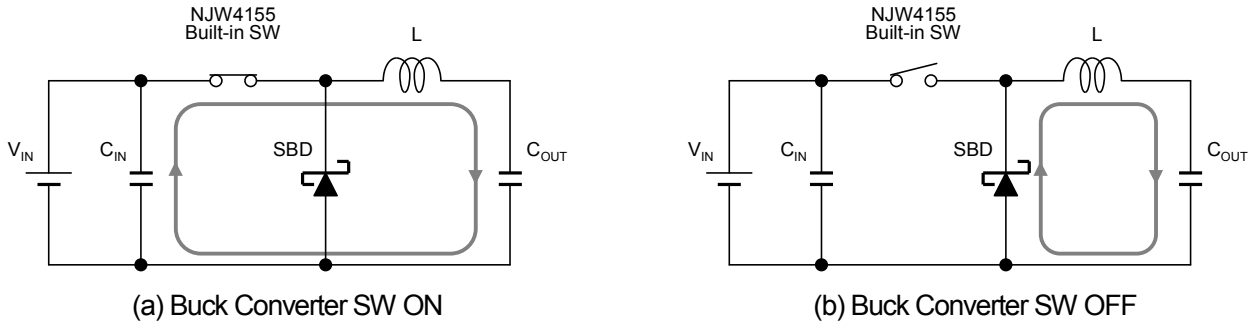


Fig. 5. Current Loop at Buck Converter

Concerning the GND line, it is preferred to separate the power system and the signal system, and use single ground point.

The voltage sensing feedback line should be as far away as possible from the inductance. Because this line has high impedance, it is laid out to avoid the influence noise caused by flux leaked from the inductance.

Fig. 6. shows example of wiring at buck converter. Fig. 7 shows the PCB layout example.

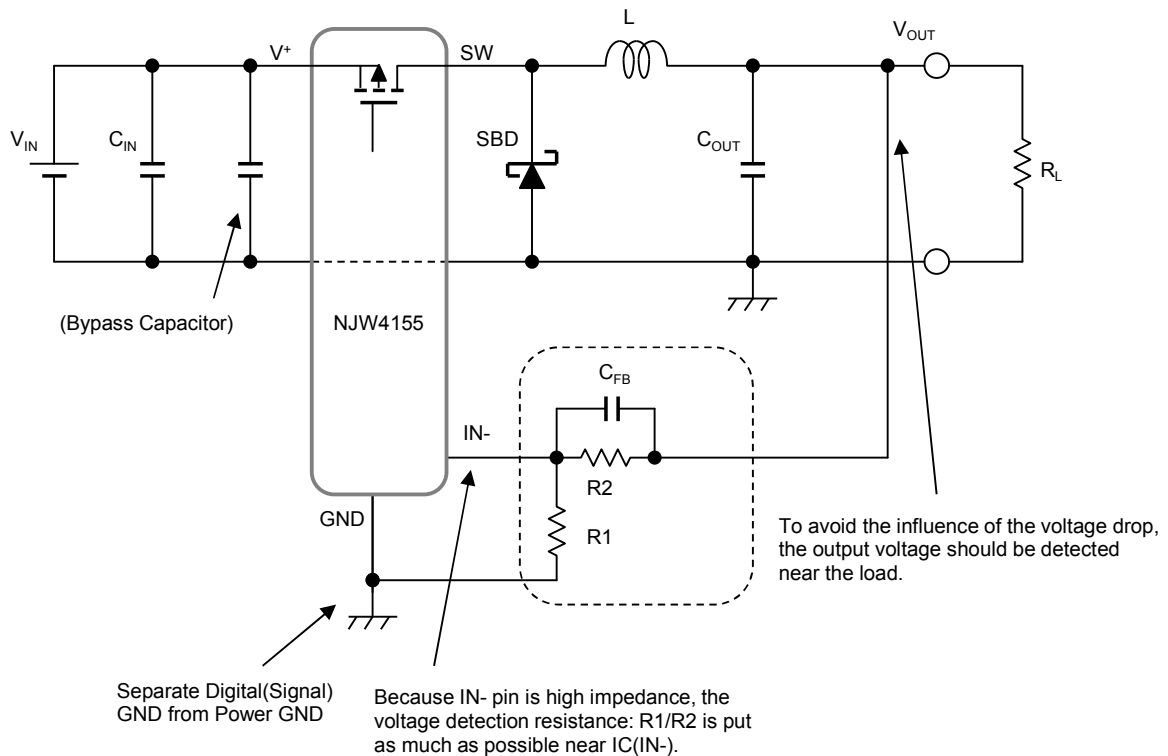
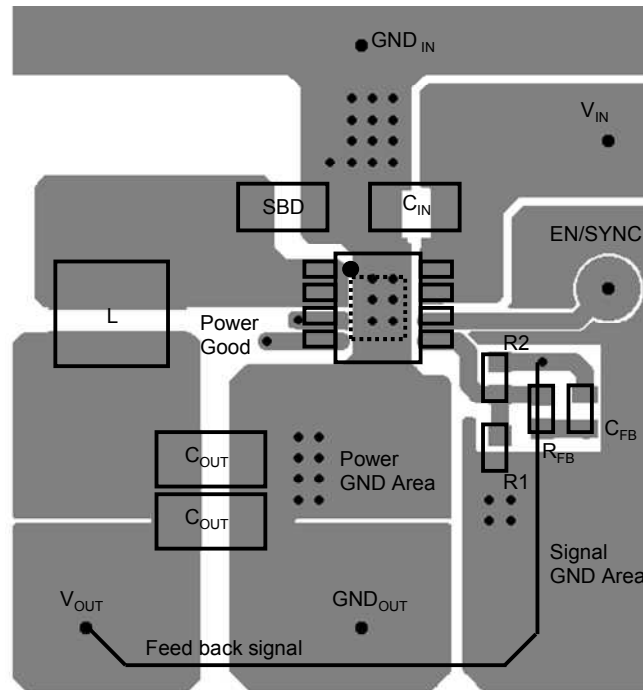


Fig. 6. Board Layout at Buck Converter

### ■ Application Information (Continued)



HSOP8 Package (A version and B version)

Connect Signal GND line and Power GND line on backside pattern

Fig. 7. Layout Example (upper view)

### ■ Calculation of Package Power

A lot of the power consumption of buck converter occurs from the internal switching element (Power MOSFET). Power consumption of NJW4155 is roughly estimated as follows.

$$\begin{aligned} \text{Input Power:} & \quad P_{\text{IN}} = V_{\text{IN}} \times I_{\text{IN}} \quad [\text{W}] \\ \text{Output Power:} & \quad P_{\text{OUT}} = V_{\text{OUT}} \times I_{\text{OUT}} \quad [\text{W}] \\ \text{Diode Loss:} & \quad P_{\text{DIODE}} = V_{\text{F}} \times I_{\text{L(avg)}} \times \text{OFF duty} \quad [\text{W}] \\ \text{NJW4155 Power Consumption:} & \quad P_{\text{LOSS}} = P_{\text{IN}} - P_{\text{OUT}} - P_{\text{DIODE}} \quad [\text{W}] \end{aligned}$$

Where:

$V_{\text{IN}}$	: Input Voltage for Converter	$I_{\text{IN}}$	: Input Current for Converter
$V_{\text{OUT}}$	: Output Voltage of Converter	$I_{\text{OUT}}$	: Output Current of Converter
$V_{\text{F}}$	: Diode's Forward Saturation Voltage	$I_{\text{L(avg)}}$	: Inductor Average Current
OFF duty	: Switch OFF Duty		

Efficiency ( $\eta$ ) is calculated as follows.

$$\eta = (P_{\text{OUT}} \div P_{\text{IN}}) \times 100 \quad [\%]$$

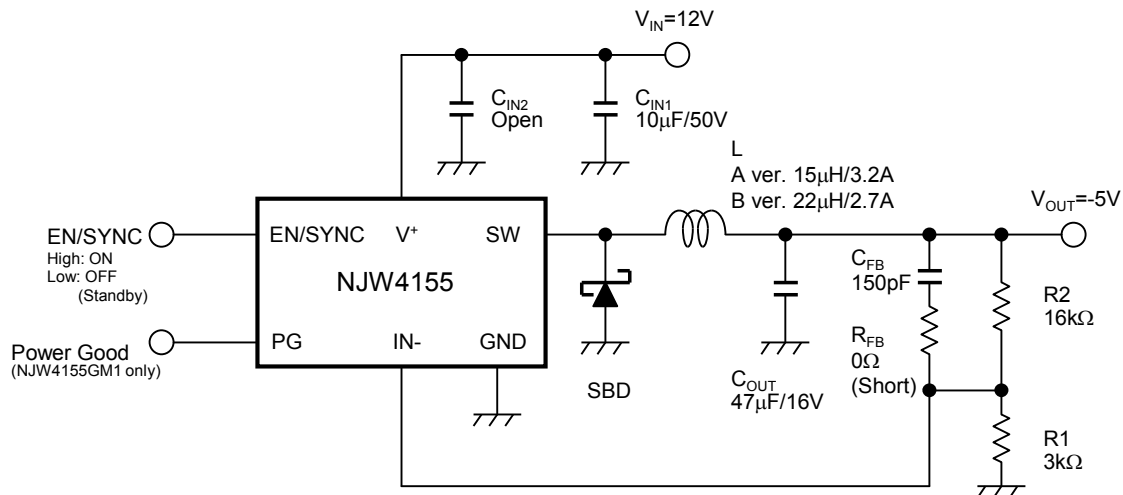
You should consider temperature derating to the calculated power consumption:  $P_{\text{D}}$ .

You should design power consumption in rated range referring to the power dissipation vs. ambient temperature characteristics.

### ■ Application Design Examples

#### ● Buck Converter Application Circuit

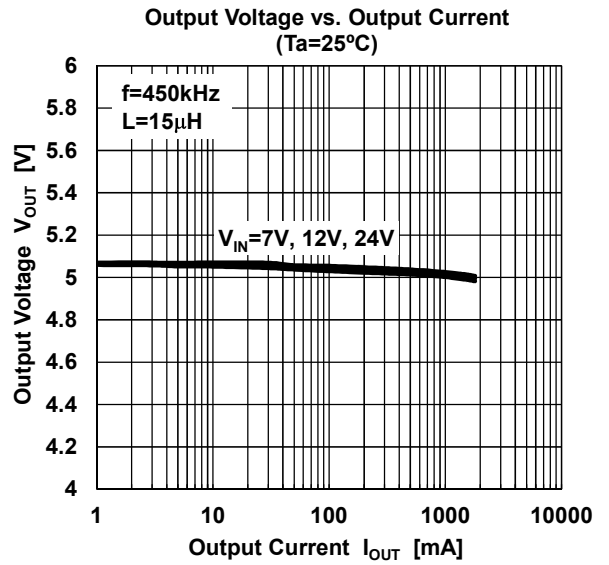
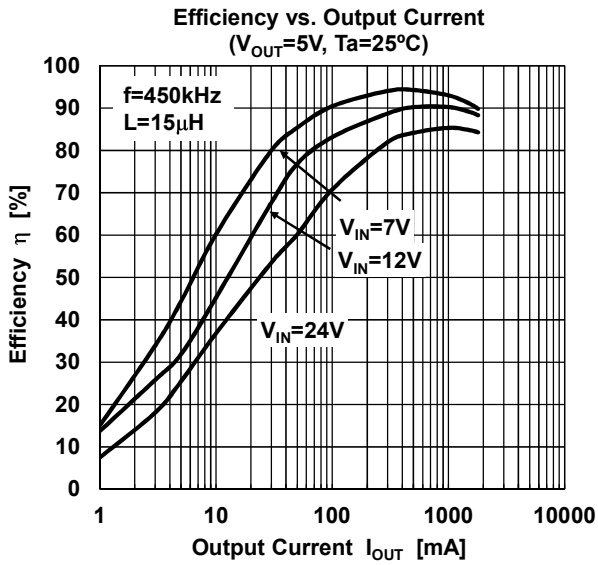
IC : NJW4155GM1  
 Input Voltage :  $V_{IN}=12V$   
 Output Voltage :  $V_{OUT}=5V$   
 Output Current :  $I_{OUT}=1.8A$   
 Oscillation frequency : A, C version  $f_{osc}=450kHz$   
                               : B version  $f_{osc}=300kHz$



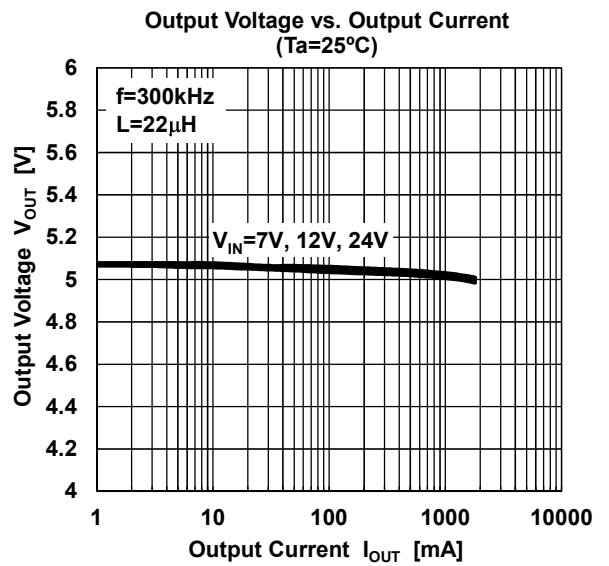
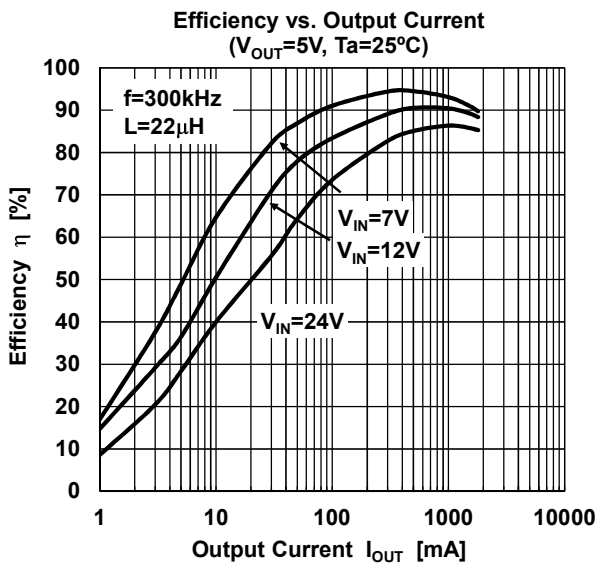
Reference	Qty.	Part Number	Description	Manufacturer
IC	1	NJW4155GM1	Internal 1.8A MOSFET SW.REG. IC	New JRC
L	1	A, C ver.: CLF10040T-150M	Inductor $15\mu H$ , 3.2A	TDK
		B ver.: CLF10040T-220M	Inductor $22\mu H$ , 2.7A	TDK
SBD	1	CMS16	Schottky Diode 40V, 3A	Toshiba
$C_{IN1}$	1	UMK325BJ106MM	Ceramic Capacitor 3225 $10\mu F$ , 50V, X5R	Taiyo Yuden
$C_{IN2}$	1	Open	Optional	—
$C_{OUT}$	1	GRM32EB31C476KE15	Ceramic Capacitor 3225 $47\mu F$ , 16V, B	Murata
$C_{FB}$	1	150pF	Ceramic Capacitor 1608 $150pF$ , 50V, CH	Std.
$R_{FB}$	1	$0\Omega$ (Short)	Optional	—
R1	1	$3k\Omega$	Resistor 1608 $3k\Omega$ , $\pm 1\%$ , 0.1W	Std.
R2	1	$16k\Omega$	Resistor 1608 $16k\Omega$ , $\pm 1\%$ , 0.1W	Std.

### Application Characteristics

#### ● A, C version



#### ● B version





# MEMO

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