DS90CR286AT-Q1 3.3 V Rising Edge Data Strobe LVDS Receiver 28-Bit Channel Link 66 MHz

1 Features

- 20 to 66 MHz Shift Clock Support
- 50% Duty Cycle on Receiver Output Clock
- Best–in–Class Setup & Hold Times on Rx Outputs
- Rx Power Consumption < 270 mW (typ) at 66 MHz Worst Case
- Rx Power-down Mode < 200 µW (max)
- ESD Rating: 4 kV (HBM), 1 kV (CDM)
- PLL Requires No External Components
- Compatible with TIA/EIA-644 LVDS Standard
- Low Profile 56-Pin DGG (TSSOP) Package
- Operating Temperature: −40°C to +105°C
- Automotive AEC-Q100 Grade 2 Qualified

2 Applications

- Video Displays
- Automotive Infotainment
- Industrial Printers and Imaging
- Digital Video Transport
- Machine Vision
- OpenLDI-to-RGB Bridge

3 Description

The DS90CR286AT-Q1 receiver converts four LVDS (Low Voltage Differential Signaling) data streams back into parallel 28 bits of LVCMOS data. The receiver data outputs strobe on the output clock's rising edge.

The receiver LVDS clock operates at rates from 20 to 66 MHz. The DS90CR286AT-Q1 phase-locks to the input LVDS clock, samples the serial bit streams at the LVDS data lines, and converts them into 28-bit parallel output data. At an incoming clock rate of 66 MHz, each LVDS input line is running at a bit rate of 462 Mbps, resulting in a maximum throughput of 1.848 Gbps.

The DS90CR286AT-Q1 device is enhanced over prior generation receivers due to a wider data valid time on the receiver output. The DS90CR286AT-Q1 is designed for PCB board chip-to-chip OpenLDI-to-RGB bridge conversion. LVDS data transmission over cable interconnect is not recommended for this device.

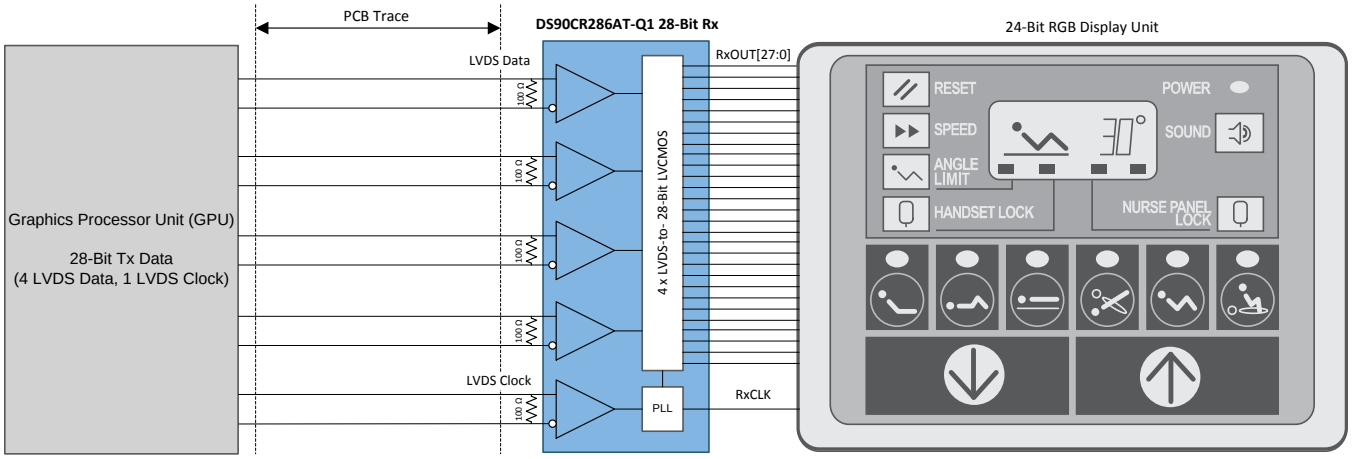
Users designing a sub-system with a compatible OpenLDI transmitter and DS90CR286AT-Q1 receiver must ensure an acceptable skew margin budget (RSKM). Details regarding RSKM can be found in the Application Information section.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90CR286AT-Q1	TSSOP (56)	14.00 mm × 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Block Diagram



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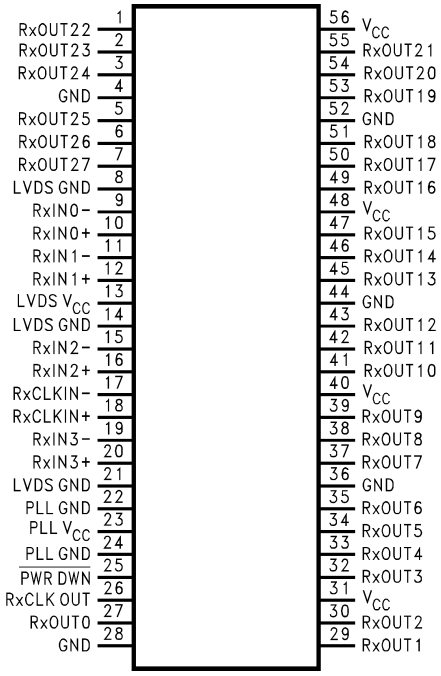
4 Revision History

Changes from Original (November 2015) to Revision A **Page**

- Changed Product Preview to full datasheet Production Data release ... 1

5 Pin Configuration and Functions

DGG Package
56-Pin TSSOP
Top View



Pin Functions

PIN		I/O , TYPE	PIN DESCRIPTION
NAME	NO.		
RxIN0+, RxIN0-, RxIN1+, RxIN1-, RxIN2+, RxIN2-, RxIN3+, RxIN3-	10, 9, 12, 11, 16, 15, 20, 19	I, LVDS	Positive and negative LVDS differential data inputs. 100 Ω termination resistors should be placed between RxIN+ and RxIN- receiver inputs as close as possible to the receiver pins for proper signaling.
RxCLKIN+, RxCLKIN-	18, 17	I, LVDS	Positive and negative LVDS differential clock input. 100 Ω termination resistor should be placed between RxCLKIN+ and RxCLKIN- receiver inputs as close as possible to the receiver pins for proper signaling.
RxOUT[27:0]	7, 6, 5, 3, 2, 1, 55, 54, 53, 51, 50, 49, 47, 46, 45, 43, 42, 41, 39, 38, 37, 35, 34, 33, 32, 30, 29, 27	O, LVCMOS	LVCMOS level data outputs.
RxCLK OUT	26	O, LVCMOS	LVCMOS level clock output. The rising edge acts as the data strobe.
$\overline{\text{PWR DWN}}$	25	I, LVCMOS	LVCMOS level input. When asserted low, the receiver outputs are low.
V_{CC}	56, 48, 40, 31	Power	Power supply pins for LVCMOS outputs.
GND	52, 44, 36, 28, 4	Power	Ground pins for LVCMOS outputs.
PLL V_{CC}	23	Power	Power supply for PLL.
PLL GND	24, 22	Power	Ground pin for PLL.
LVDS V_{CC}	13	Power	Power supply pin for LVDS inputs.
LVDS GND	21, 14, 8	Power	Ground pins for LVDS inputs.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply Voltage (V_{CC})	−0.3	4	V
LVCMOS Output Voltage	−0.3	(V_{CC} + 0.3)	V
LVDS Receiver Input Voltage	−0.3	(V_{CC} + 0.3)	V
Operating Junction Temperature		150	°C
Lead Temperature (Soldering, 4 sec)		260	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	25	105	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{Noise})			100	mVp-p

6.4 Thermal Information

THERMAL METRIC (1)		DS90CR286AT-Q1 DGG (TSSOP) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	33.3	
ψ_{JT}	Junction-to-top characterization parameter	1.0	
ψ_{JB}	Junction-to-board characterization parameter	33.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics[1][2]

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS (For $\overline{\text{PWR DWN}}$ Pin)							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4 V, 2.5 V or V_{CC}			+1.8	+10	µA
		V_{IN} = GND		−10	0		µA
LVCMOS DC SPECIFICATIONS							
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		2.7	3.3		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.06	0.3	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V			−60	−120	mA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = 1.2 V				+100	mV
V_{TL}	Differential Input Low Threshold	V_{CM} = 1.2 V		−100			mV
I_{IN}	Input Current	V_{IN} = 2.4 V, V_{CC} = 3.6 V				±10	µA
		V_{IN} = 0V , V_{CC} = 3.6 V				±10	µA
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern, DS90CR286AT-Q1 (Figure 1 Figure 2), T_A=−40°C to 105°C	f = 33 MHz		49	65	mA
			f = 40 MHz		53	70	mA
			f = 66 MHz		81	105	mA
ICCRZ	Receiver Supply Current Power Down	$\overline{\text{PWR DWN}}$ = Low; Receiver Outputs Stay Low during Power Down Mode			10	55	µA

(1) Typical values are given for V_{CC} = 3.3 V and T_A = 25ºC.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLHT	LVCMOS Low-to-High Transition Time (Figure 2)			2	5	ns
CHLT	LVCMOS High-to-Low Transition Time (Figure 2)			1.8	5	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 8)	f = 40 MHz, T = 25ºC	1.01	1.4	2.45	ns
RSPos1	Receiver Input Strobe Position for Bit 1		4.52	5.0	5.99	ns
RSPos2	Receiver Input Strobe Position for Bit 2		8.08	8.5	9.35	ns
RSPos3	Receiver Input Strobe Position for Bit 3		11.59	11.9	12.89	ns
RSPos4	Receiver Input Strobe Position for Bit 4		15.15	15.6	16.53	ns
RSPos5	Receiver Input Strobe Position for Bit 5		18.86	19.2	20.20	ns
RSPos6	Receiver Input Strobe Position for Bit 6		22.34	22.9	23.91	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 8)	f = 66 MHz, T = -40ºC	0.58	1.1	1.55	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.77	3.3	3.80	ns
RSPos2	Receiver Input Strobe Position for Bit 2		5.01	5.4	5.77	ns
RSPos3	Receiver Input Strobe Position for Bit 3		7.11	7.5	7.88	ns
RSPos4	Receiver Input Strobe Position for Bit 4		9.24	9.7	10.12	ns
RSPos5	Receiver Input Strobe Position for Bit 5		11.44	11.9	12.32	ns
RSPos6	Receiver Input Strobe Position for Bit 6		13.62	14.1	14.50	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 8)	f = 66 MHz, T = 25ºC	0.68	1.2	1.64	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.88	3.4	3.88	ns
RSPos2	Receiver Input Strobe Position for Bit 2		5.08	5.5	5.87	ns
RSPos3	Receiver Input Strobe Position for Bit 3		7.20	7.6	7.98	ns
RSPos4	Receiver Input Strobe Position for Bit 4		9.30	9.7	10.24	ns
RSPos5	Receiver Input Strobe Position for Bit 5		11.50	12.0	12.40	ns
RSPos6	Receiver Input Strobe Position for Bit 6		13.70	14.2	14.57	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 8)	f = 66 MHz, T = 105ºC	0.84	1.3	1.74	ns
RSPos1	Receiver Input Strobe Position for Bit 1		3.00	3.6	4.05	ns
RSPos2	Receiver Input Strobe Position for Bit 2		5.14	5.6	6.02	ns
RSPos3	Receiver Input Strobe Position for Bit 3		7.30	7.8	8.14	ns
RSPos4	Receiver Input Strobe Position for Bit 4		9.42	9.9	10.40	ns
RSPos5	Receiver Input Strobe Position for Bit 5		11.59	12.1	12.57	ns
RSPos6	Receiver Input Strobe Position for Bit 6		13.83	14.3	14.73	ns
RCOP	RxCLK OUT Period (Figure 3)		15		50	ns
RCOH	RxCLK OUT High Time (Figure 3)	f = 40 MHz	10.0	12.2		ns
RCOL	RxCLK OUT Low Time (Figure 3)		10.0	11.0		ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 3)		6.5	11.6		ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 3)		6.0	11.6		ns
RCOH	RxCLK OUT High Time (Figure 3)	f = 66 MHz	5.0	7.6		ns
RCOL	RxCLK OUT Low Time (Figure 3)		5.0	6.3		ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 3)		4.5	7.3		ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 3)		4.0	6.3		ns

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RCCD	RxCLK IN to RxCLK OUT Delay at 25°C, V_{CC} = 3.3V(1) (Figure 4)		3.5	5.0	7.5	ns
RPLLS	Receiver Phase Lock Loop Set (Figure 5)				10	ms
RPDD	Receiver Power Down Delay (Figure 7)				1	µs

(1) Total latency for the channel link chipset is a function of clock period and gate delays through the transmitter (TCCD) and receiver (RCCD). The total latency for the DS90CR285 transmitter and DS90CR286AT-Q1 receiver is: (T + TCCD) + (2*T + RCCD), where T = Clock period. If another transmitter is used, the alternative transmitter's TCCD must be used to calculate total latency.

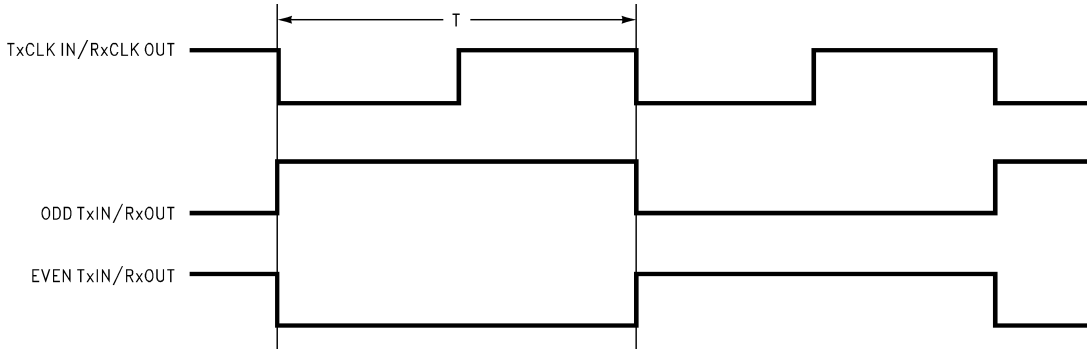


Figure 1. "Worst Case" Test Pattern

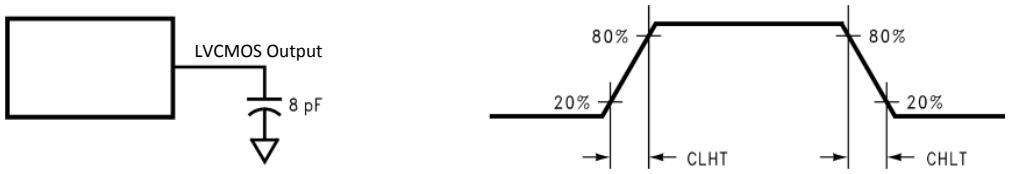


Figure 2. LVCMOS Output Load and Transition Times

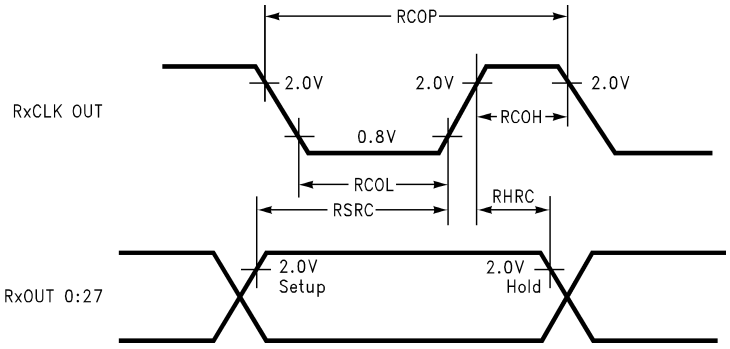


Figure 3. Setup/Hold and High/Low Times

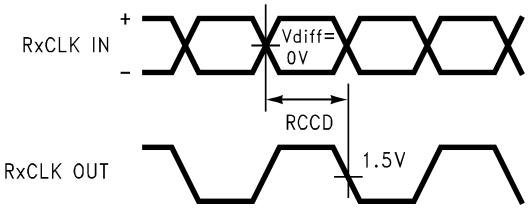


Figure 4. Clock In to Clock Out Delay

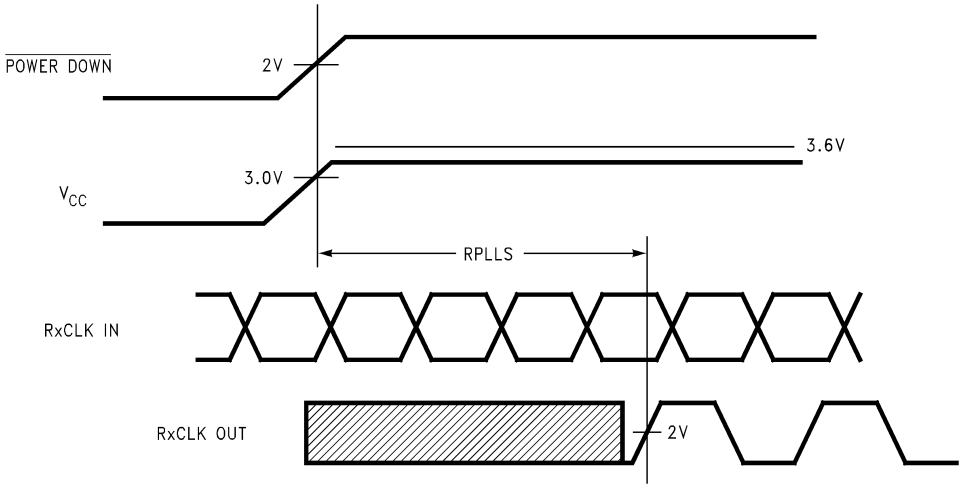


Figure 5. Phase Lock Loop Set Time

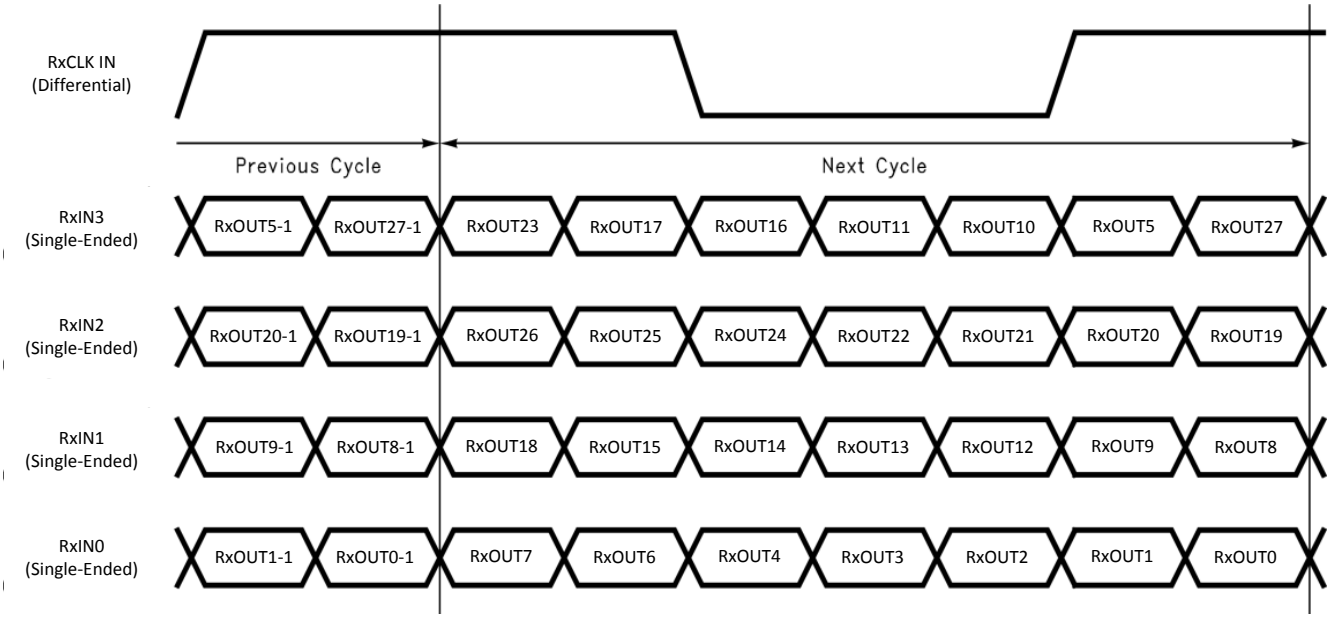


Figure 6. Mapping of 28 LVCMOS Parallel Data to 4D + C LVDS Serialized Data

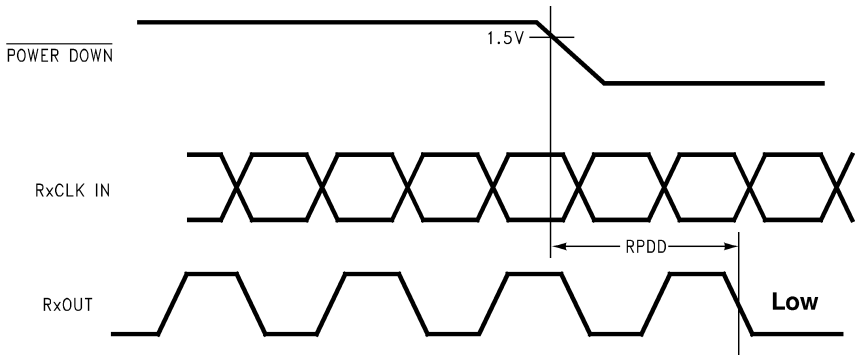


Figure 7. Power Down Delay

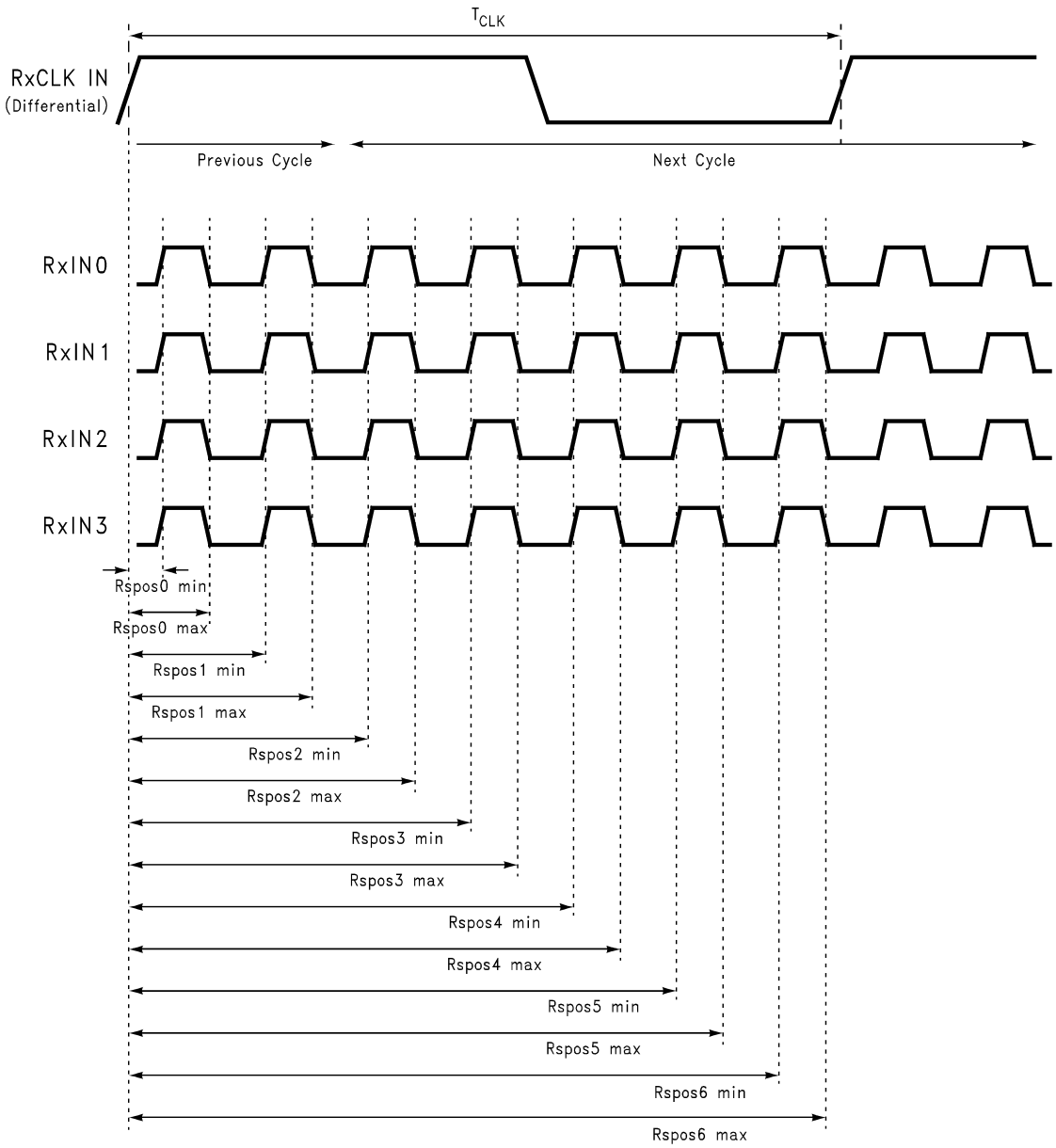


Figure 8. LVDS Input Strobe Position

6.7 Typical Characteristics

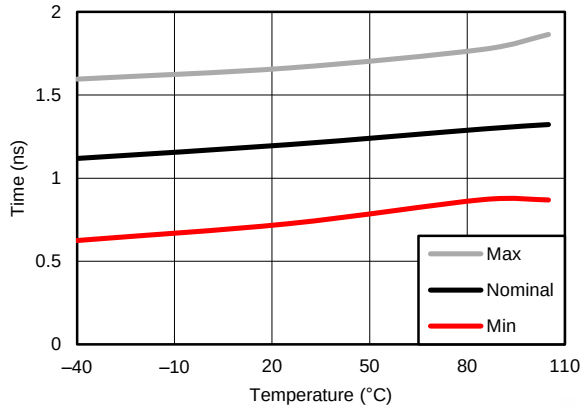


Figure 9. Rx Strobe Position 0 versus Temperature
Operating Frequency: 66 MHz

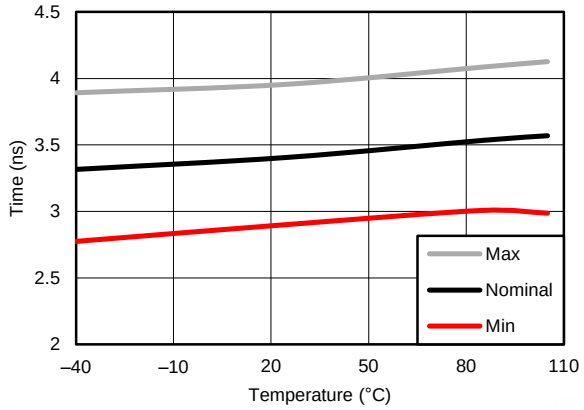


Figure 10. Rx Strobe Position 1 versus Temperature
Operating Frequency: 66 MHz

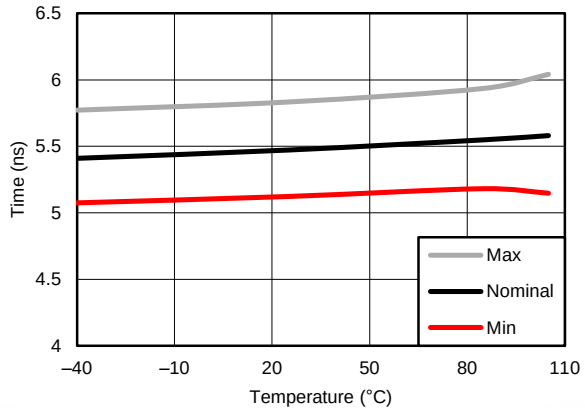


Figure 11. Rx Strobe Position 2 versus Temperature
Operating Frequency: 66 MHz

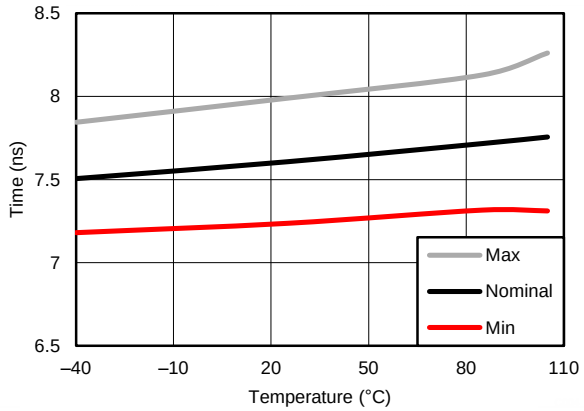


Figure 12. Rx Strobe Position 3 versus Temperature
Operating Frequency: 66 MHz

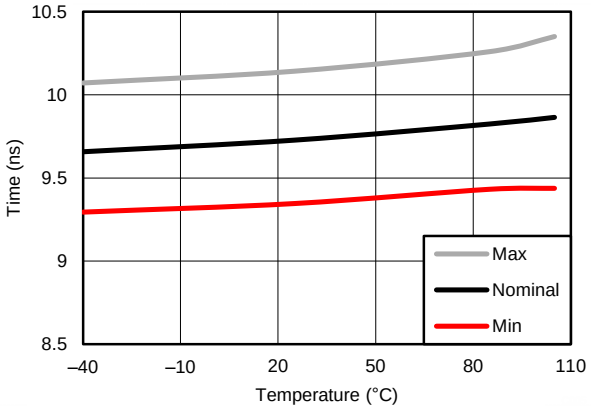


Figure 13. Rx Strobe Position 4 versus Temperature
Operating Frequency: 66 MHz

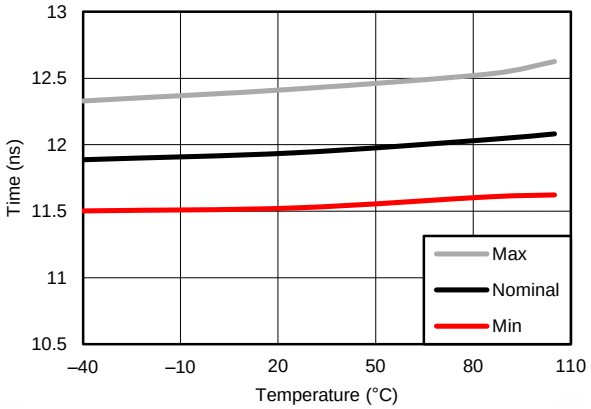


Figure 14. Rx Strobe Position 5 versus Temperature
Operating Frequency: 66 MHz

Typical Characteristics (continued)

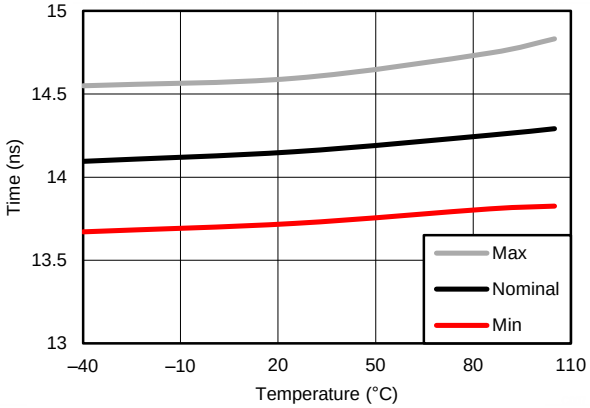


Figure 15. Rx Strobe Position 6 versus Temperature
Operating Frequency: 66 MHz

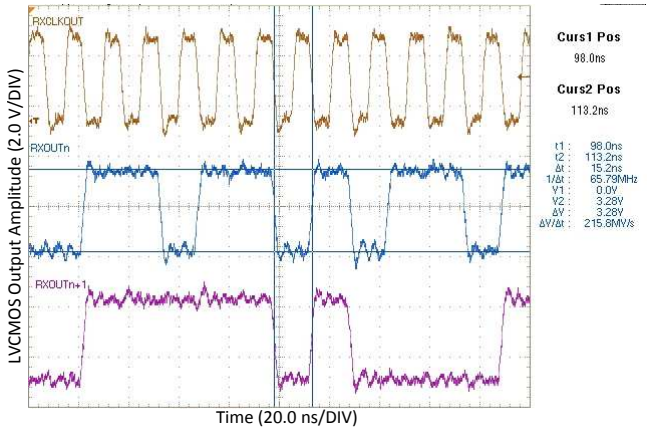


Figure 16. Parallel PRBS-7 on LVCMOS Outputs at 66 MHz

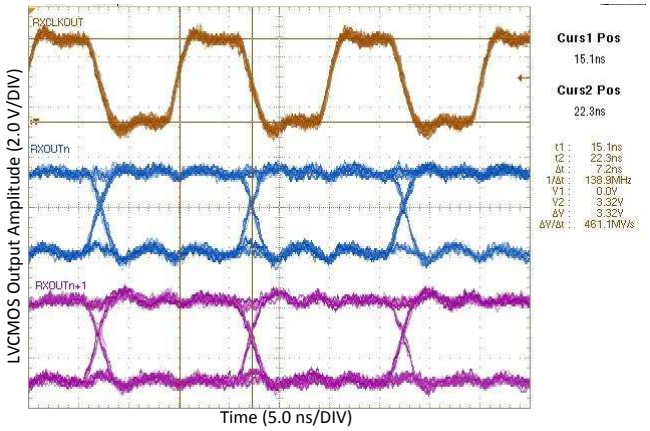


Figure 17. Typical RxOUT Timing Diagram at 66 MHz

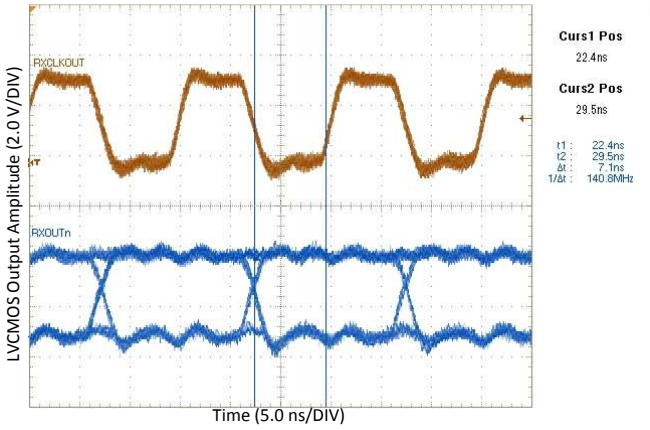


Figure 18. Typical RxOUT Setup Time at 66 MHz
(RSRC = 7.1 ns)

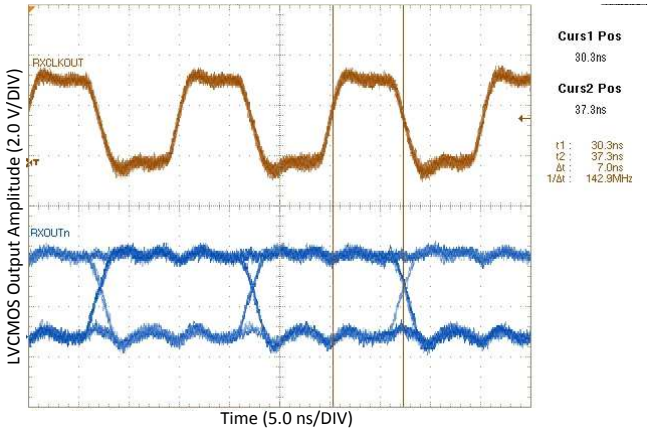


Figure 19. Typical RxOUT Hold Time at 66 MHz
(RHRC = 7.0 ns)

7 Detailed Description

7.1 Overview

The DS90CR286AT-Q1 is an AEC-Q100 Grade 2 receiver that converts four LVDS (Low Voltage Differential Signaling) data streams back into parallel 28 bits of LVCMOS data (24 bits of RGB and 4 bits of HSYNC, VSYNC, DE, and CNTL). An internal PLL locks to the incoming LVDS clock ranging from 20 to 66 MHz. The locked PLL then ensures a stable clock to sample the output LVCMOS data on the Receiver Clock Out rising edge. The DS90CR286AT-Q1 features a $\overline{\text{PWR DWN}}$ pin to put the device into low power mode when there is no active input data.

7.2 Functional Block Diagram

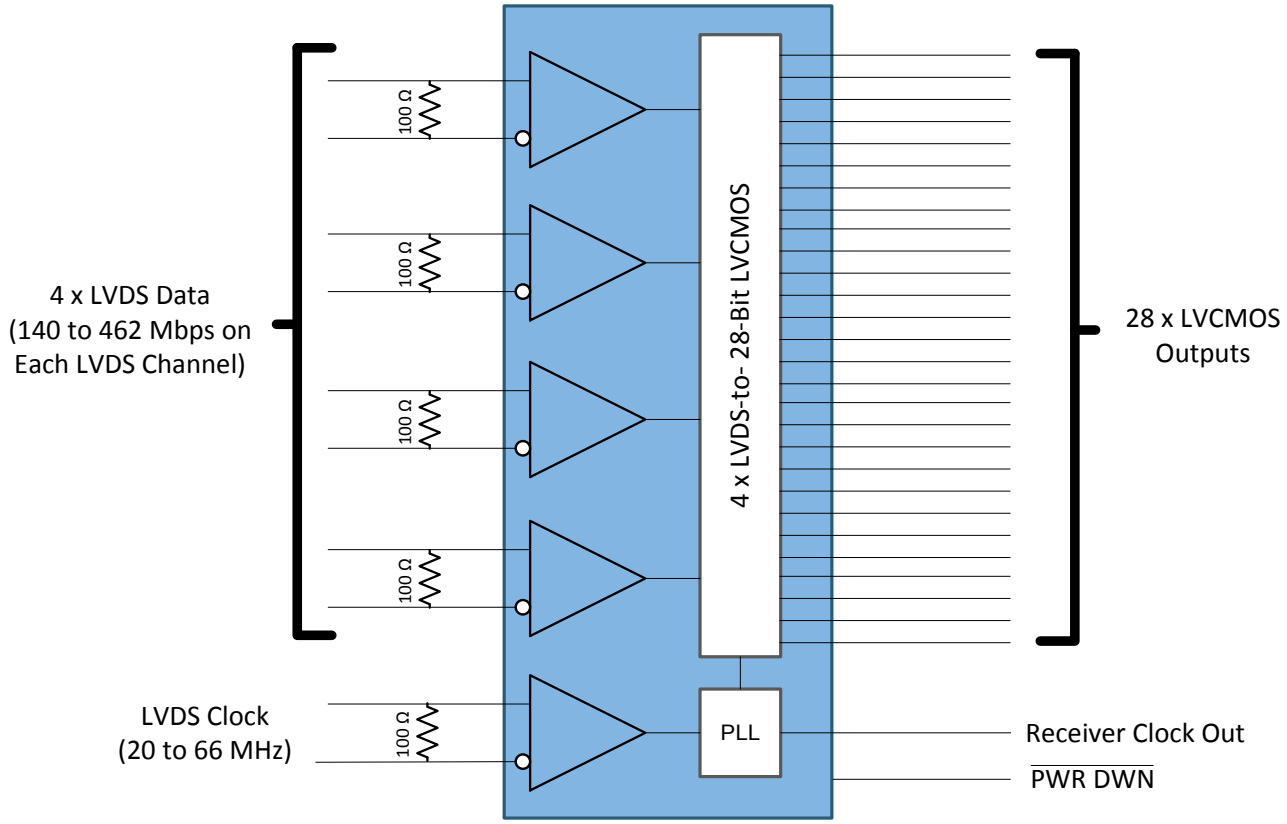


Figure 20. DS90CR286AT-Q1 Block Diagram

7.3 Feature Description

The DS90CR286AT-Q1 consists of several key blocks:

- LVDS Receivers
- Phase Locked Loop (PLL)
- Serial LVDS-to-Parallel LVCMOS Converter
- LVCMOS Drivers

7.3.1 LVDS Receivers

There are five differential LVDS inputs to the DS90CR286AT-Q1. Four of the LVDS inputs contain serialized data originating from a 28-bit source transmitter. The remaining LVDS input contains the LVDS clock associated with the data pairs.

Feature Description (continued)

7.3.1.1 Input Termination

The DS90CR286AT-Q1 requires a single 100 Ω terminating resistor across the positive and negative lines on each differential pair of the receiver input. To prevent reflections due to stubs, this resistor should be placed as close to the device input pins as possible. Figure 21 shows an example.

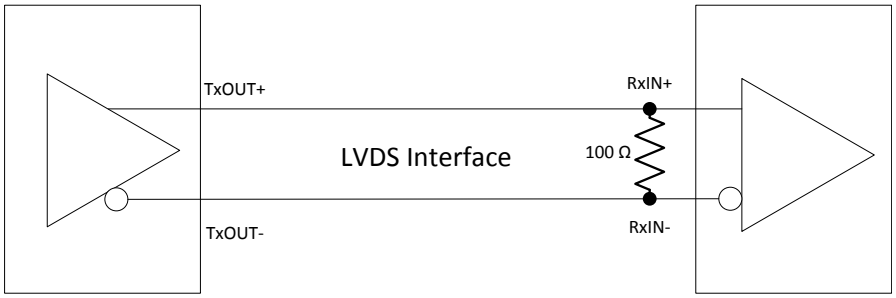


Figure 21. LVDS Serialized Link Termination

7.3.2 Phase Locked Loop (PLL)

The Channel Link I devices use an internal PLL to recover the clock transmitted across the LVDS interface. The recovered clock is then used as a reference to determine the sampling position of the seven serial bits received per clock cycle. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. Differential skew (Δt within one differential pair), interconnect skew (Δt of one differential pair to another), and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Individual bypassing of each V_{CC} to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock to improve the overall jitter budget.

7.3.3 Serial LVDS-to-Parallel LVCMOS Converter

After the PLL locks to the incoming LVDS clock, the receiver deserializes each LVDS differential data pair into seven parallel LVCMOS data outputs per clock cycle. For the DS90CR286AT-Q1, the LVDS data inputs map to LVCMOS outputs according to Figure 6.

7.3.4 LVCMOS Drivers

The LVCMOS outputs from the DS90CR286AT-Q1 are the deserialized single-ended data from the serialized LVDS data pairs. Each LVCMOS output is clocked by the PLL and should be strobed on the RxCLKOUT rising edge by the endpoint device. All unused DS90CR286AT-Q1 RxOUT outputs can be left floating.

7.4 Device Functional Modes

7.4.1 Power Down Mode

The DS90CR286AT-Q1 receiver may be placed into a power down mode at any time by asserting the $\overline{\text{PWR DWN}}$ pin (active low). The DS90CR286AT-Q1 is also designed to protect from accidental loss of power to either the transmitter or receiver. If power to the transmitter is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver loses power, the receiver inputs are shorted to V_{CC} through an internal diode. Current is limited to 5 mA per input, thus avoiding the potential for latch-up when powering the device.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS90CR286AT-Q1 is designed for a wide variety of data transmission applications. The use of serialized LVDS data lines in these applications allows for efficient signal transmission over a narrow bus width, thereby reducing cost, power, and space. The DS90CR286AT-Q1 is designed for PCB board chip-to-chip OpenLDI-to-RGB (LVDS-to-parallel) bridge conversion. LVDS data transmission over cable interconnect is not recommended for this device. Users designing a sub-system with a compatible OpenLDI transmitter and DS90CR286AT-Q1 receiver must ensure an acceptable skew margin budget (RSKM).

8.2 Typical Application

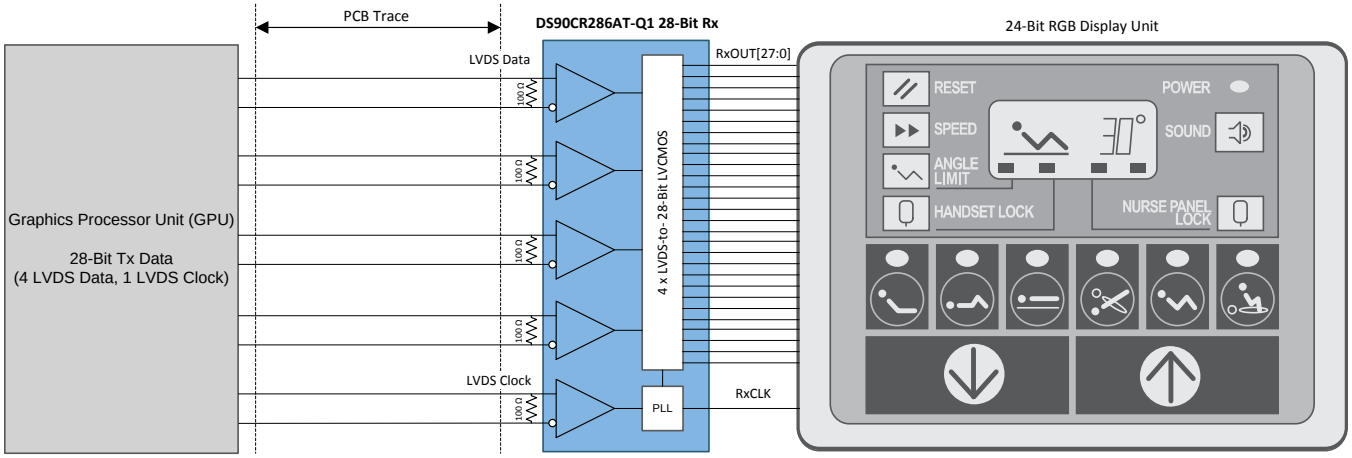


Figure 22. Typical DS90CR286AT-Q1 Application Block Diagram

8.2.1 Design Requirements

For this design example, ensure that the following requirements are observed.

Table 1. DS90CR286AT-Q1 Design Parameters

DESIGN PARAMETER	DESIGN REQUIREMENTS
Operating Frequency	LVDS clock must be within 20-66 MHz.
Bit Resolution	No higher than 24 bpp. The maximum supported resolution is 8-bit RGB.
Bit Data Mapping	Determine the appropriate mapping required by the panel display following the DS90CR286AT-Q1 outputs.
RSKM (Receiver Skew Margin)	Ensure that there is acceptable margin between Tx pulse position and Rx strobe position.
Input Termination for RxIN±	100 Ω ± 10% resistor across each LVDS differential pair. Place as close as possible to IC input pins.
RxIN± Board Trace Impedance	Design differential trace impedance with 100 Ω ± 5%.
LVCMOS Outputs	If unused, leave pins floating. Series resistance on each LVCMOS output optional to reduce reflections from long board traces. If used, 33 Ω series resistance is typical.
DC Power Supply Coupling Capacitors	Use a 0.1 µF capacitor to minimize power supply noise. Place as close as possible to Vcc pins.

8.2.2 Detailed Design Procedure

To begin the design process with the DS90CR286AT-Q1, determine the following:

- Operating Frequency
- Bit Resolution of the Panel
- Bit Mapping from Receiver to Endpoint Panel Display
- RSKM Interoperability with Transmitter Pulse Position Margin

8.2.2.1 Bit Resolution and Operating Frequency Compatibility

The bit resolution of the endpoint panel display reveals whether there are enough bits available in the DS90CR286AT-Q1 to output the required data per pixel. The DS90CR286AT-Q1 has 28 parallel LVCMOS outputs and can therefore provide a bit resolution up to 24 bpp (bits per pixel). In each clock cycle, the remaining bits are the three control signals (HSync, VSync, DE) and one spare bit.

The number of pixels per frame and the refresh rate of the endpoint panel display indicate the required operating frequency of the receiver clock. To determine the required clock frequency, refer to the following formula:

$$f\_Clk = [H\_Active + H\_Blank] \times [V\_Active + V\_Blank] \times f\_Vertical \quad (1)$$

where

- H_Active = Active Display Horizontal Lines
- H_Blank = Blanking Period Horizontal Lines
- V_Active = Active Display Vertical Lines
- V_Blank = Blanking Period Vertical Lines
- f_Vertical = Refresh Rate (in Hz)
- f_Clk = Operating Frequency of LVDS clock

In each frame, there is a blanking period associated with horizontal rows and vertical columns that are not actively displayed on the panel. These blanking period pixels must be included to determine the required clock frequency. Consider the following example to determine the required LVDS clock frequency:

- H_Active = 640
- H_Blank = 40
- V_Active = 480
- V_Blank = 41
- f_Vertical = 59.95 Hz

Thus, the required operating frequency is determined below:

$$[640 + 40] \times [480 + 41] \times 59.95 = 21239086 \text{ Hz} \approx 21.24 \text{ MHz} \quad (2)$$

Since the operating frequency for the PLL in the DS90CR286AT-Q1 ranges from 20-66 MHz, the DS90CR286AT-Q1 can support a panel display with the aforementioned requirements.

If the specific blanking interval is unknown, the number of pixels in the blanking interval can be approximated to 20% of the active pixels. The following formula can be used as a conservative approximation for the operating LVDS clock frequency:

$$f\_Clk \approx H\_Active \times V\_Active \times f\_Vertical \times 1.2 \quad (3)$$

Using this approximation, the operating frequency for the example in this section is estimated below:

$$640 \times 480 \times 59.95 \times 1.2 = 22099968 \text{ Hz} \approx 22.10 \text{ MHz} \quad (4)$$

8.2.2.2 Data Mapping between Receiver and Endpoint Panel Display

Ensure that the LVCMOS outputs are mapped to align with the endpoint display RGB mapping requirements following the deserializer. Two popular mapping topologies for 8-bit RGB data are shown below:

1. LSBs are mapped to RxIN3±.
2. MSBs are mapped to RxIN3±.

The following tables depict how these two popular topologies can be mapped to the DS90CR286AT-Q1 outputs.

Table 2. 8-Bit Color Mapping with LSBs on RxIN3±

LVDS INPUT CHANNEL	LVDS BIT STREAM POSITION	LVCMOS OUTPUT CHANNEL	COLOR MAPPING	COMMENTS
RxIN0	TxIN0	RxOUT0	R2	
	TxIN1	RxOUT1	R3	
	TxIN2	RxOUT2	R4	
	TxIN3	RxOUT3	R5	
	TxIN4	RxOUT4	R6	
	TxIN6	RxOUT6	R7	MSB
RxIN1	TxIN7	RxOUT7	G2	
	TxIN8	RxOUT8	G3	
	TxIN9	RxOUT9	G4	
	TxIN12	RxOUT12	G5	
	TxIN13	RxOUT13	G6	
	TxIN14	RxOUT14	G7	MSB
	TxIN15	RxOUT15	B2	
	TxIN18	RxOUT18	B3	
RxIN2	TxIN19	RxOUT19	B4	
	TxIN20	RxOUT20	B5	
	TxIN21	RxOUT21	B6	
	TxIN22	RxOUT22	B7	MSB
	TxIN24	RxOUT24	HSYNC	Horizontal Sync
	TxIN25	RxOUT25	VSYNC	Vertical Sync
	TxIN26	RxOUT26	DE	Data Enable
RxIN3	TxIN27	RxOUT27	R0	LSB
	TxIN5	RxOUT5	R1	
	TxIN10	RxOUT10	G0	LSB
	TxIN11	RxOUT11	G1	
	TxIN16	RxOUT16	B0	LSB
	TxIN17	RxOUT17	B1	
	TxIN23	RxOUT23	GP	General Purpose

Table 3. 8-Bit Color Mapping with MSBs on RxIN3±

LVDS INPUT CHANNEL	LVDS BIT STREAM POSITION	LVCMOS OUTPUT CHANNEL	COLOR MAPPING	COMMENTS
RxIN0	TxIN0	RxOUT0	R0	LSB
	TxIN1	RxOUT1	R1	
	TxIN2	RxOUT2	R2	
	TxIN3	RxOUT3	R3	
	TxIN4	RxOUT4	R4	
	TxIN6	RxOUT6	R5	
RxIN1	TxIN7	RxOUT7	G0	LSB
	TxIN8	RxOUT8	G1	
	TxIN9	RxOUT9	G2	
	TxIN12	RxOUT12	G3	
	TxIN13	RxOUT13	G4	
	TxIN14	RxOUT14	G5	
	TxIN15	RxOUT15	B0	LSB
	TxIN18	RxOUT18	B1	

Table 3. 8-Bit Color Mapping with MSBs on RxIN3± (continued)

LVDS INPUT CHANNEL	LVDS BIT STREAM POSITION	LVCMOS OUTPUT CHANNEL	COLOR MAPPING	COMMENTS
RxIN2	TxIN19	RxOUT19	B2	
	TxIN20	RxOUT20	B3	
	TxIN21	RxOUT21	B4	
	TxIN22	RxOUT22	B5	
	TxIN24	RxOUT24	HSYNC	Horizontal Sync
	TxIN25	RxOUT25	VSYNC	Vertical Sync
	TxIN26	RxOUT26	DE	Data Enable
RxIN3	TxIN27	RxOUT27	R6	
	TxIN5	RxOUT5	R7	MSB
	TxIN10	RxOUT10	G6	
	TxIN11	RxOUT11	G7	MSB
	TxIN16	RxOUT16	B6	
	TxIN17	RxOUT17	B7	MSB
	TxIN23	RxOUT23	GP	General Purpose

In situations where the DS90CR286AT-Q1 must support 18 bpp, Table 2 is commonly used. With this mapping, MSBs of RGB data are retained on RXIN0±, RXIN1±, and RXIN2± while the two LSBs for the original 8-bit RGB resolution are ignored from RxIN3±.

8.2.2.3 RSKM Interoperability

One of the most important factors when designing the receiver into a system application is assessing how much RSKM (Receiver Skew Margin) is available. In each LVDS clock cycle, the LVDS data stream carries seven serialized data bits. Ideally, the Transmit Pulse Position for each bit will occur every (n x T)/7 seconds, where n = Bit Position and T = LVDS Clock Period. Likewise, ideally the Receive Strobe Position for each bit will occur every ((n + 0.5) x T)/7 seconds. However, due to the effects of clock jitter and ISI, both LVDS transmitter and receiver in real systems will have a minimum and maximum pulse and strobe position, respectively, for each bit position. This concept is illustrated in Figure 23:

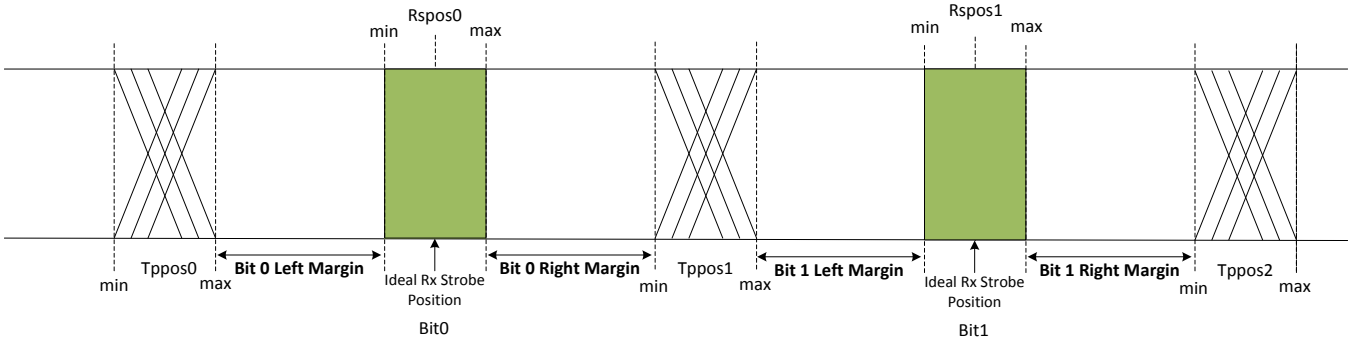


Figure 23. RSKM Measurement Example

All left and right margins for Bits 0-6 must be considered in order to determine the absolute minimum for the whole LVDS bit stream. This absolute minimum corresponds to the RSKM.

To improve RSKM performance between LVDS transmitter and receiver, designers may either advance or delay the LVDS clock compared to the LVDS data. Moving the LVDS clock compared to the LVDS data can improve the Rx strobe position compared to the Tx pulse position of the transmitter.

If there is less left bit margin than right bit margin, the LVDS clock can be delayed so that the Rx strobe position for incoming data appears to be delayed. If there is less right bit margin than left bit margin, all the LVDS data pairs can be delayed uniformly so that the LVDS clock and Rx strobe position for incoming data appear to advance. To delay an LVDS data or clock pair, designers can either add more PCB trace length or install a capacitor between the LVDS transmitter and receiver. It is important to note that when using these techniques, all serialized bit positions are shifted right or left uniformly.

When designing the DS90CR286AT-Q1 receiver with a third-party OpenLDI transmitter, users must calculate the skew margin budget (RSKM) based on the Tx pulse position and the Rx strobe position to ensure error-free transmission. For more information about calculating RSKM, refer to Application Note SNLA249.

8.2.3 Application Curves

The following application curves are examples taken with a DS90C385 serializer interfacing to a DS90CR286AT-Q1 deserializer in nominal temperature (25ºC) at an operating frequency of 66 MHz.

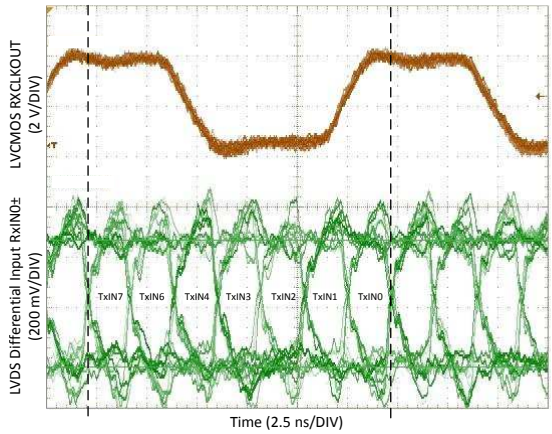


Figure 24. LVDS RxIN0± aligned with LVCMOS RxCLKOUT

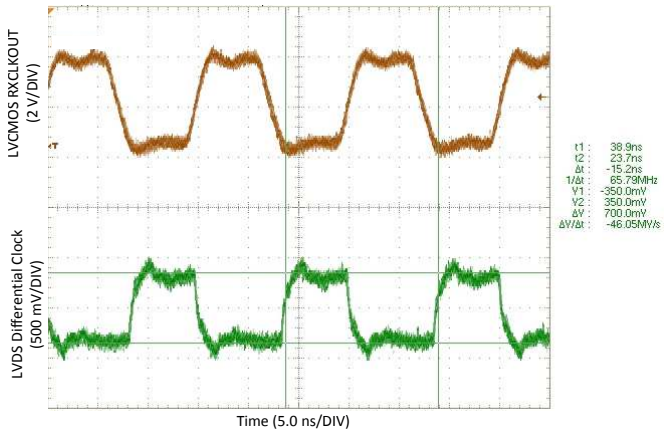


Figure 25. LVDS CLKIN aligned with LVCMOS RxCLKOUT

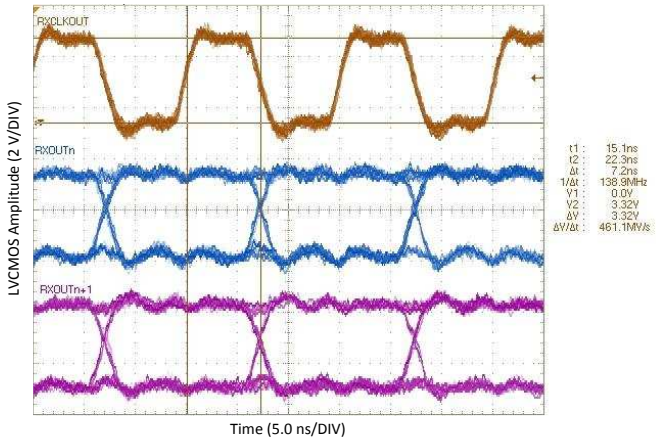


Figure 26. RxOUT and RxCLKOUT Timing Diagram

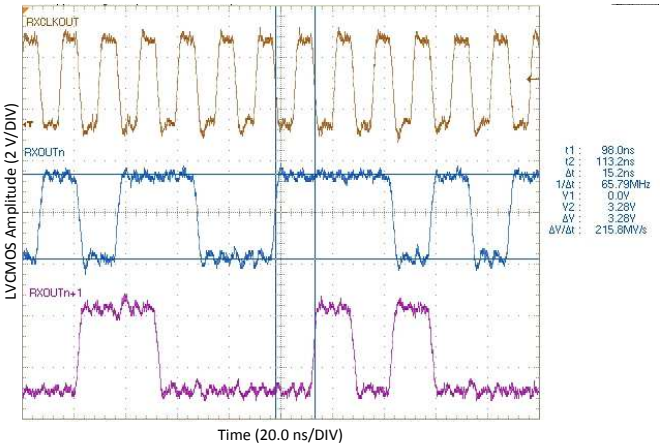


Figure 27. PRBS-7 Output on RxOUT Channels

9 Power Supply Recommendations

Proper power supply decoupling is important to ensure a stable power supply with minimal power supply noise. Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach, three parallel-connected decoupling capacitors (Multi-Layered Ceramic type in surface mount form factor) between each V_{CC} and the ground plane(s) are recommended. The three capacitor values are 0.1 µF, 0.01 µF and 0.001 µF. The preferred capacitor size is 0402. An example is shown in Figure 28. The designer should place bypass capacitors as close as possible to the V_{CC} pins and ensure each capacitor has its own via to connect the ground plane. If board space is limiting the number of bypass capacitors, the PLL V_{CC} should receive the most filtering or bypassing. Next would be the LVDS V_{CC} pins and finally the logic V_{CC} pins.

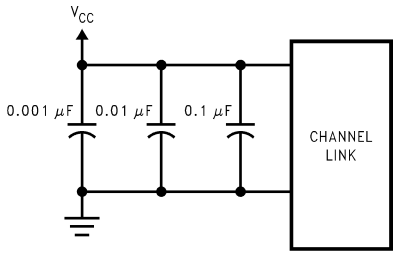


Figure 28. Recommended Bypass Capacitor Decoupling Configuration

10 Layout

10.1 Layout Guidelines

As with any high speed design, board designers must maximize signal integrity by limiting reflections and crosstalk that can adversely affect high frequency and EMI performance. The following practices are recommended layout guidelines to optimize device performance.

- Ensure that differential pair traces are always closely coupled to eliminate noise interference from other signals and take full advantage of the common mode noise canceling effect of the differential signals.
- Maintain equal length on signal traces for a given differential pair.
- Limit impedance discontinuities by reducing the number of vias on signal traces.
- Eliminate any 90º angles on traces and use 45º bends instead.
- If a via must exist on one signal polarity, mirror the via implementation on the other polarity of the differential pair.
- Match the differential impedance of the selected physical media. This impedance should also match the value of the termination resistor that is connected across the differential pair at the receiver's input.
- When possible, use short traces for LVDS inputs.

10.2 Layout Example

The following images show an example layout of the DS90CR286AT-Q1. Traces in blue correspond to the top layer and the traces in green correspond to the bottom layer. Note that differential pair inputs to the DS90CR286AT-Q1 are tightly coupled and close to the connector pins. In addition, observe that the power supply decoupling capacitors are placed as close as possible to the power supply pins with through vias in order to minimize inductance.

Layout Example (continued)

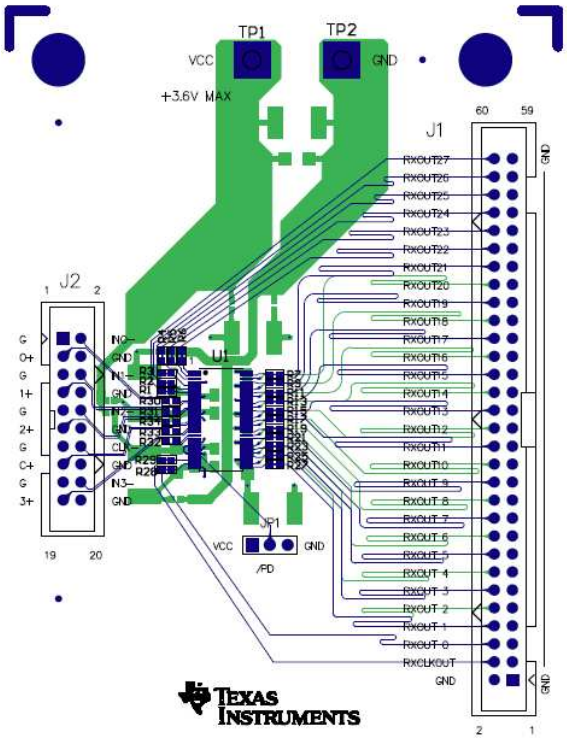


Figure 29. Example Layout with DS90CR286AT-Q1 (U1).

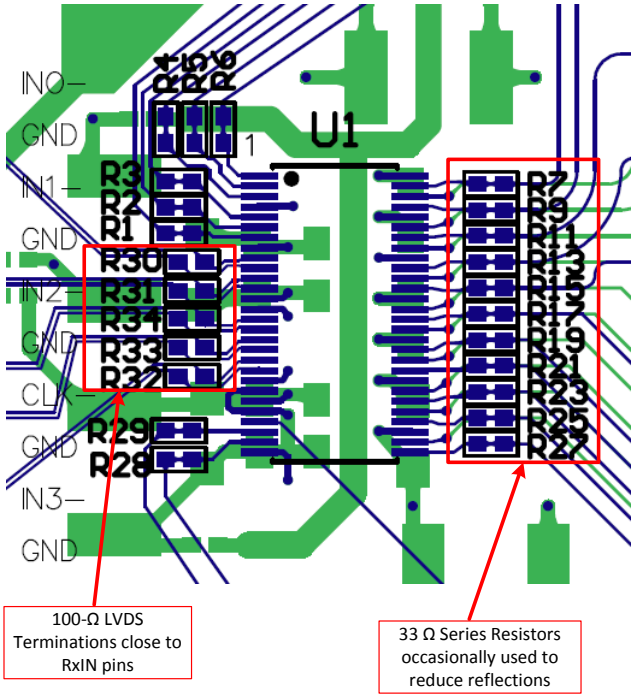


Figure 30. Example Layout Close-up.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

IC Package Thermal Metrics application report, SPRA953

How to Calculate and Improve Receiver Skew Margin for Channel Link I Devices application note, SNLA249

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90CR286ATDGGQ1	ACTIVE	TSSOP	DGG	56	34	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 105	DS90CR286ATQ DGG	Samples
DS90CR286ATDGGRQ1	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 105	DS90CR286ATQ DGG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

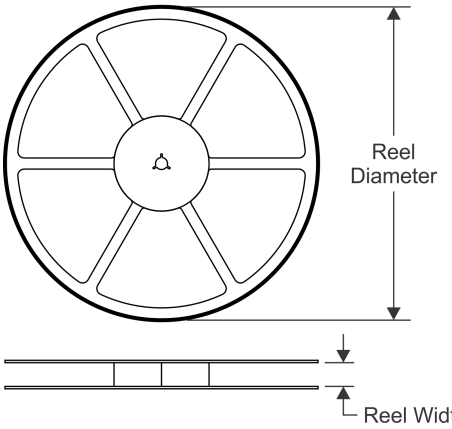
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

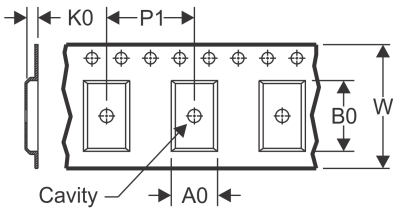
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

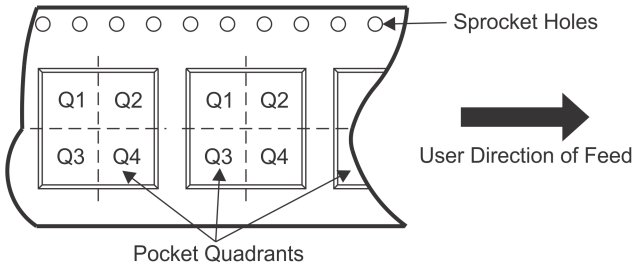


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

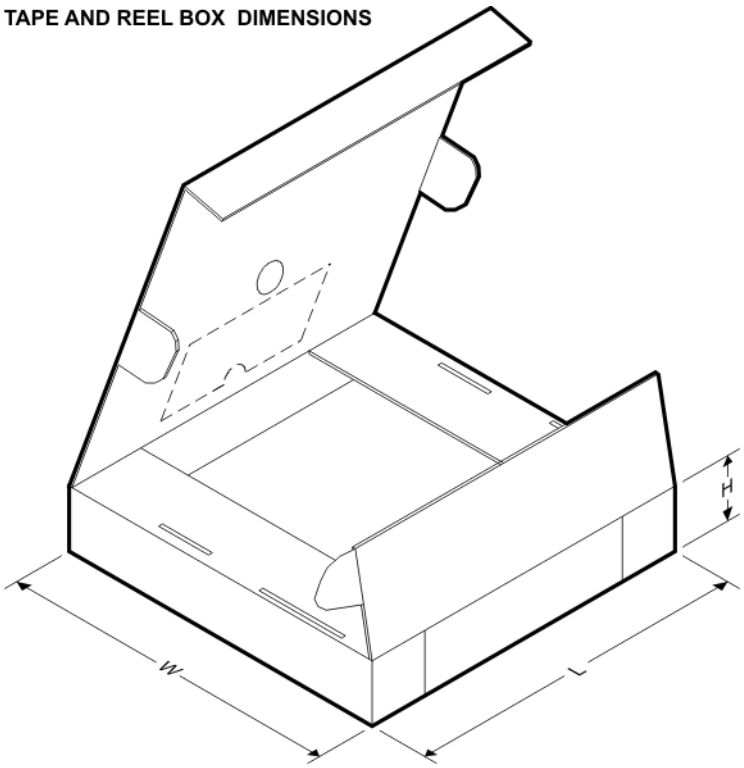
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CR286ATDGGRQ1	TSSOP	DGG	56	2000	330.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

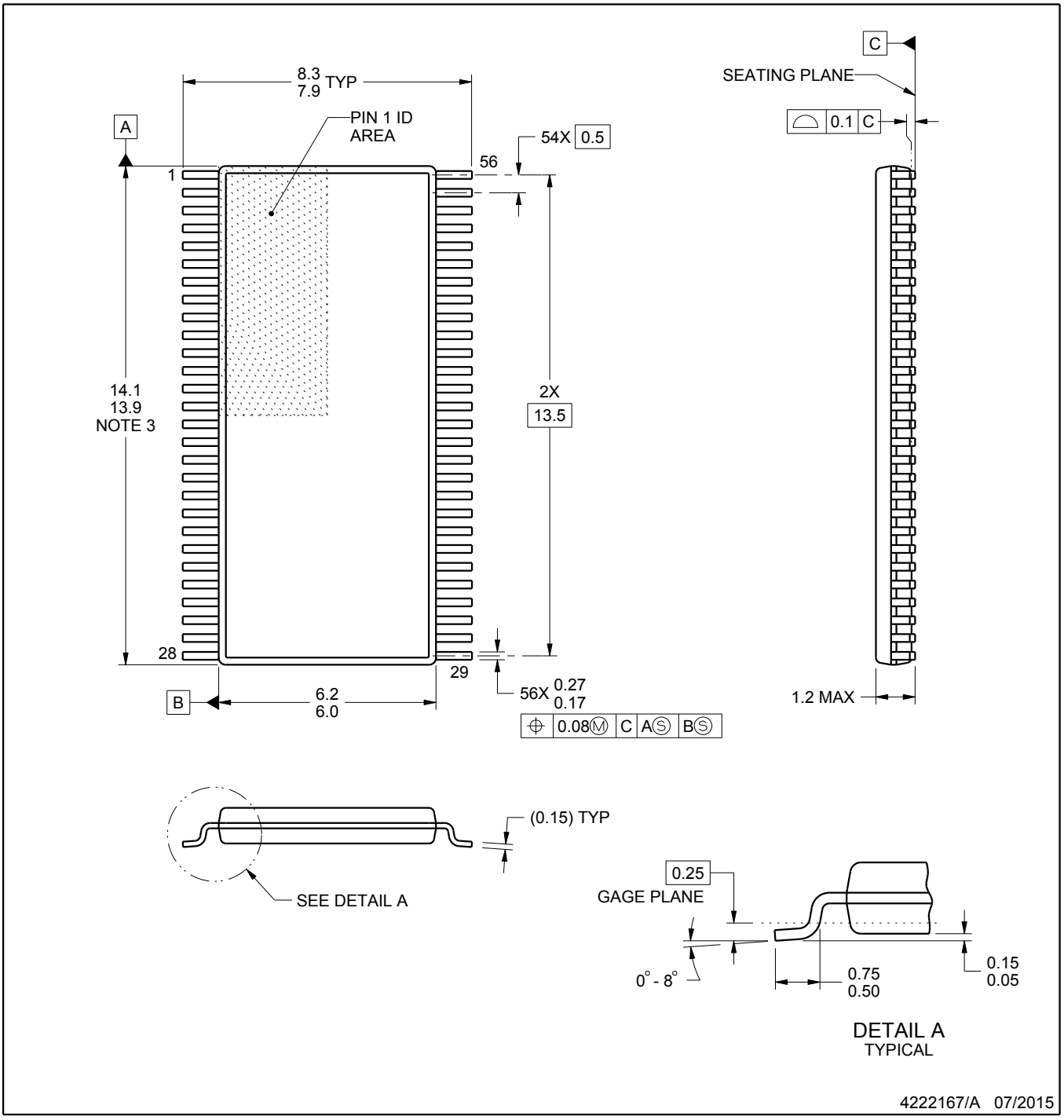
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CR286ATDGGRQ1	TSSOP	DGG	56	2000	367.0	367.0	45.0

PACKAGE OUTLINE

DGG0056A

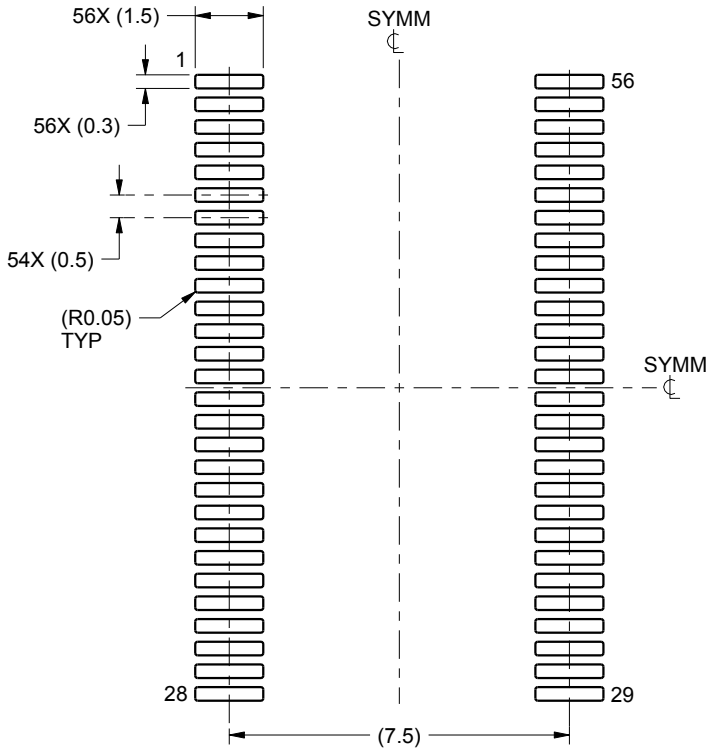
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

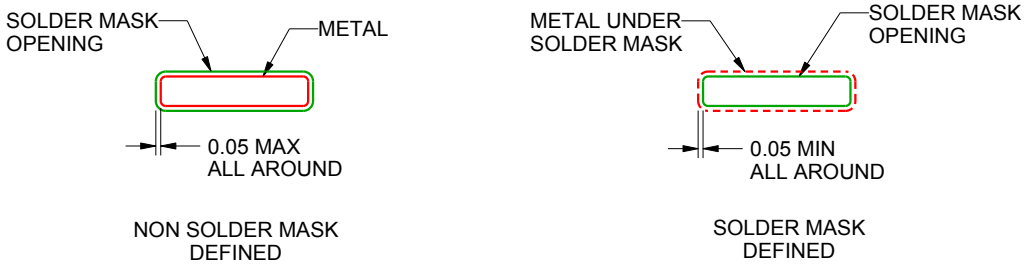


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

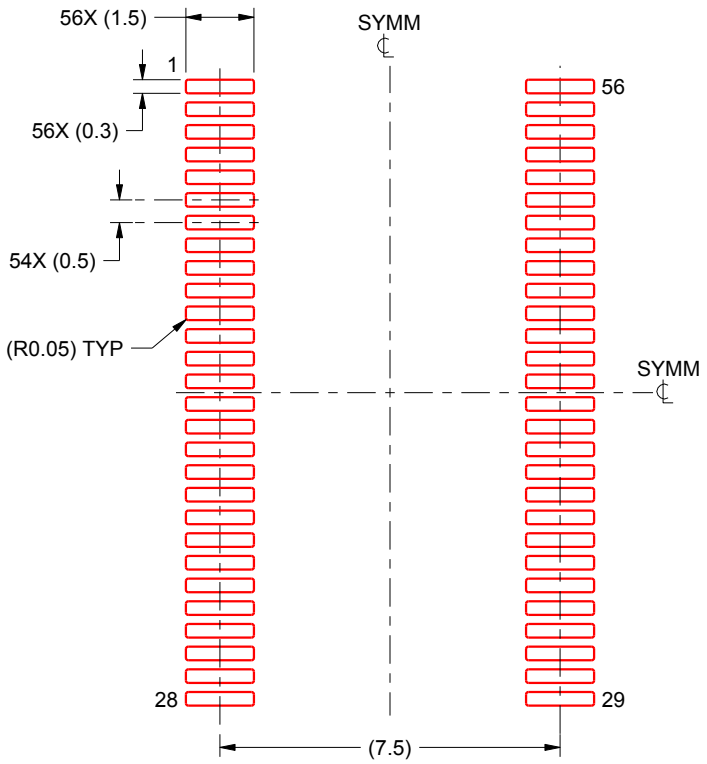


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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