Low Charge Injection 8-Channel High Voltage Analog Switch

Features

- HVCMOS® technology for high performance
- Very low quiescent power dissipation -10µA
- Output ON-resistance typically 11Ω
- Low parasitic capacitance
- DC to 10MHz analog signal frequency
- -60dB typical off-isolation at 5MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- Serial shift register logic control with latches
- Flexible operating supply voltages
- Surface mount packages

Applications

- Medical ultrasound imaging
- Non-destructive evaluation

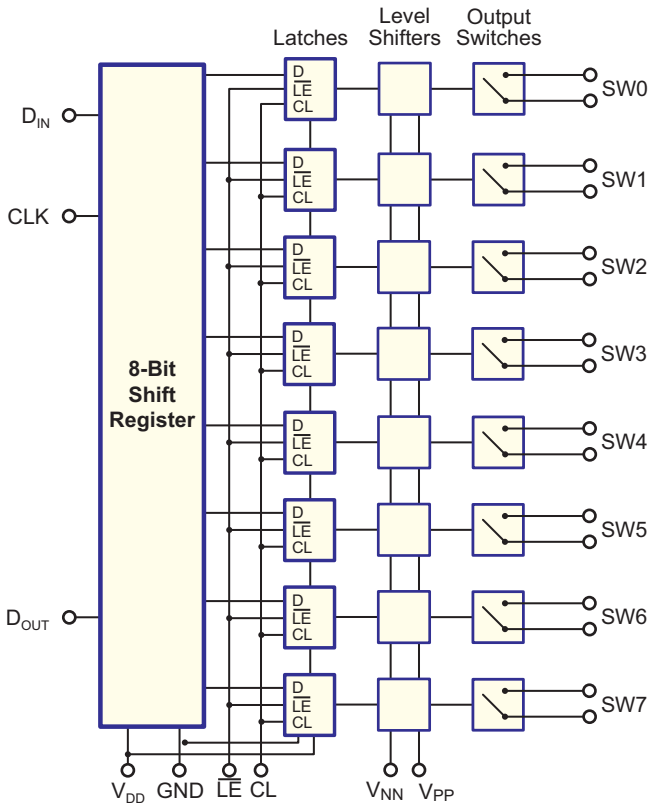
General Description

The Supertex HV219 is a low switch resistance, low charge injection 8-channel 200V analog switch integrated circuit (IC) intended primarily for medical ultrasound imaging. The device can also be used for NDE, non-destructive evaluation applications. The HV219 is a lower switch resistance, 11Ω versus 22Ω, version of the Supertex HV20220 device. The lower switch resistance will help reduce insertion loss. It has the same pin configuration as that of the Supertex HV20220PJ and the HV20220FG.

The device is manufactured using Supertex's HVCMOS® (high voltage CMOS) technology with high voltage bilateral DMOS structures for the outputs and low voltage CMOS logic for the input control. The outputs are configured as eight independent single pole single throw 11Ω analog switches. The input logic is an 8-bit serial to parallel shift register followed by an 8-bit parallel latch. The switch states are determined by the data in the latch. Logic high will correspond to a closed switch and logic low as an opened switch.

The HV219 is designed to operate on various combinations of high voltage supplies. For example the V_{PP} and V_{NN} supplies can be: +40V/-160V, +100V/-100V, or +160V/-40V. This allows the user to maximize the signal voltage for uni-polar negative, bi-polar, or uni-polar positive.

Block Diagram



Ordering Information

Package Options		
Device	**28-Lead PLCC**	**48-Lead LQFP (7x7x1.4mm)**
HV219	HV219PJ	HV219FG
	HV219PJ-G	HV219FG-G

-G indicates the part is RoHS compliant (Green)

Absolute Maximum Ratings

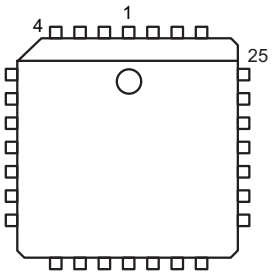
Parameter	Value
V_{DD} logic power supply voltage	-0.5V to +15V
V_{PP} - V_{NN} supply voltage	220V
V_{PP} positive high voltage supply	-0.5V to V_{NN} +200V
V_{NN} negative high voltage supply	+0.5V to -200V
Logic input voltages	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation: 28-Lead PLCC 48-Lead LQFP (7x7x1.4mm)	 1.2W 1.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

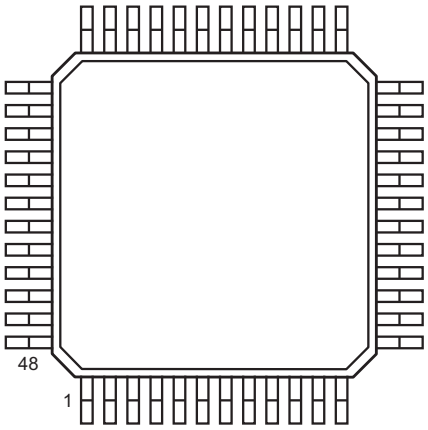
Operating Conditions

Symbol	Parameter	Value
V_{DD}	Logic power supply voltage	4.5V to 13.2V
V_{PP}	Positive high voltage supply	40V to V_{NN} +200V
V_{NN}	Negative high voltage supply	-40V to -160V
V_{IH}	High level input logic voltage	V_{DD} -1.5V to V_{DD}
V_{IL}	Low-level input logic voltage	0V to 1.5V
V_{SIG}	Analog signal voltage peak-to-peak	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air temperature	0°C to 70°C

Pin Configurations



28-Lead (J) PLCC (PJ)
(top view)

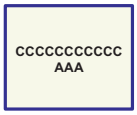


48-Lead LQFP (FG)
(7x7x1.4mm)
(top view)

Product Marking

Top Marking

Bottom Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin
A = Assembler ID*
_____ = "Green" Packaging

**May be part of top marking.*

28-Lead PLCC (PJ)

Top Marking

Bottom Marking

YY = Year Sealed
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**May be part of top marking*

48-Lead LQFP (FG)

DC Electrical Characteristics *(over recommended operating conditions unless otherwise noted)*

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R_{ONS}	Small signal switch On-resistance	-	15	-	13	19	-	24	Ω	I_{SIG} = 5mA	V_{PP} = +40V V_{NN} = -160V
		-	13	-	11	14	-	16		I_{SIG} = 200mA	
		-	13	-	11	14	-	15		I_{SIG} = 5mA	V_{PP} = +100V V_{NN} = -100V
		-	9	-	9	12	-	14		I_{SIG} = 200mA	
		-	12	-	10	13	-	15		I_{SIG} = 5mA	V_{PP} = +160V V_{NN} = -40V
		-	11	-	8	13	-	14		I_{SIG} = 200mA	
ΔR_{ONS}	Small signal switch On-resistance matching	-	20	-	5.0	20	-	20	%	I_{SIG} = 5mA, V_{PP} = +100V, V_{NN} = -100V	
R_{ONL}	Large signal switch On-resistance	-	-	-	8	-	-	-	Ω	V_{SIG} = V_{PP} - 10V, I_{SIG} = 1A	
I_{SOL}	Switch off leakage per switch	-	5.0	-	1.0	10	-	15	µA	V_{SIG}= V_{PP} -10V & V_{NN} +10V	
	DC offset switch off	-	300	-	100	300	-	300	mV	R_{LOAD} = 100KΩ	
	DC offset switch on	-	500	-	100	500	-	500	mV	R_{LOAD} = 100KΩ	
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	10	50	-	-	µA	All switches off	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-10	-50	-	-	µA	All switches off	
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	10	50	-	-	µA	All switches on, I_{SW} = 5mA	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-10	-50	-	-	µA	All switches on, I_{SW} = 5mA	
	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V_{SIG} duty cycle < 0.1%	
f_{SW}	Output switch frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I_{PP}	Average V_{PP} supply current	-	6.5	-	-	7.0	-	8.0	mA	V_{PP} = +40V V_{NN} = -160V	All output switches are turning ON and OFF at 50kHz with no load
		-	4.0	-	-	5.0	-	5.5		V_{PP} = +100V V_{NN} = -100V	
		-	4.0	-	-	5.0	-	5.5		V_{PP} = +160V V_{NN} = -40V	
I_{NN}	Average V_{NN} supply current	-	6.5	-	-	7.0	-	8.0	mA	V_{PP} = +40V V_{NN} = -160V	
		-	4.0	-	-	5.0	-	5.5		V_{PP} = +100V V_{NN} = -100V	
		-	4.0	-	-	5.0	-	5.5		V_{PP} = +160V V_{NN} = -40V	
I_{DD}	Average V_{DD} supply current	-	4.0	-	-	4.0	-	4.0	mA	f_{CLK} = 5MHz, V_{DD} = 5.0V	
I_{DDQ}	Quiescent V_{DD} supply current	-	10	-	-	10	-	10	µA	All logic inputs are static	
I_{SOR}	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = V_{DD} - 0.7V	
I_{SINK}	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = 0.7V	
C_{IN}	Large input capacitance	-	10	-	-	10	-	10	pF	---	

AC Electrical Characteristics *(over recommended operating conditions, V_{DD} = 5.0V, unless otherwise noted)*

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{SD}	Set-up time before LE rises	150	-	150	-	-	150	-	ns	---
t_{WLE}	Time width of LE	150	-	150	-	-	150	-	ns	---
t_{DO}	Clock delay time to data out	-	150	-	-	150	-	150	ns	---
tw_{CL}	Time width of CL	150	-	150	-	-	150	-	ns	---
t_{SU}	Set-up time data to clock	15	-	15	8.0	-	20	-	ns	---
t_H	Hold time data from clock	35	-	35	-	-	35	-	ns	---
f_{CLK}	Clock frequency	-	5.0	-	-	5.0	-	5.0	MHz	50% duty cycle, $f_{DATA} = f_{CLK}/2$
tr, tf	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
T_{ON}	Turn-on time	-	5.0	-	-	5.0	-	5.0	µs	$V_{SIG} = V_{PP}$ -10V, R_{LOAD} = 10KΩ
T_{OFF}	Turn-off time	-	5.0	-	-	5.0	-	5.0	µs	$V_{SIG} = V_{PP}$ -10V, R_{LOAD} = 10KΩ
dv/dt	Maximum V_{SIG} slew rate	-	20	-	-	20	-	20	V/ns	V_{PP} = +40V, V_{NN} = -160V
		-	20	-	-	20	-	20		V_{PP} = +100V, V_{NN} = -100V
		-	20	-	-	20	-	20		V_{PP} = +160V, V_{NN} = -40V
KO	Off isolation	-30	-	-30	-33	-	-	-	dB	F = 5MHz, 1KΩ//15pF load
		-58	-	-58	-	-	-	-		F = 5MHz, 50Ω load
K_{CR}	Switch crosstalk	-	-	-60	-	-	-	-	dB	F = 5MHz, 50Ω load
I_{ID}	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to GND	14	25	14	20	25	14	25	pF	0V, f = 1MHz
$C_{SG(ON)}$	On capacitance SW to GND	40	60	40	50	60	40	60	pF	0V, f = 1MHz
$+V_{SPK}$	Output voltage spike	-	-	-	-	150	-	-	mV	V_{PP} = +40V, V_{NN} = -160V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	200	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		V_{PP} = +100V, V_{NN} = -100V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	200	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	200	-	-		
Q	Charge injection	-	-	-	1450	-	-	-	pC	V_{PP} = +40V, V_{NN} = -160V, V_{SIG} = 0V
		-	-	-	1050	-	-	-		V_{PP} = +100V, V_{NN} = -100V, V_{SIG} = 0V
		-	-	-	550	-	-	-		V_{PP} = +160V, V_{NN} = -40V, V_{SIG} = 0V

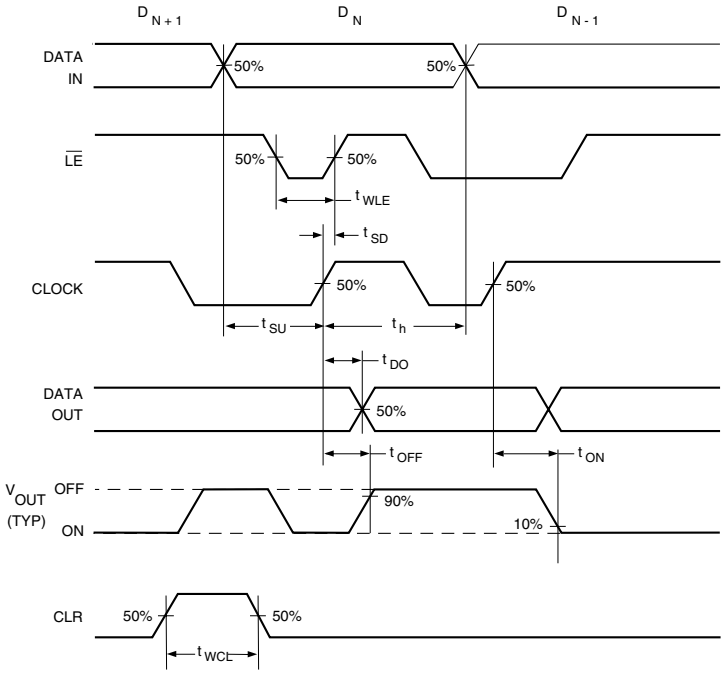
Truth Table

Data in 8-Bit Shift Register								$\overline{LE}$	CL	Output Switch State							
D0	D1	D2	D3	D4	D5	D6	D7			SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	Hold Previous State							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

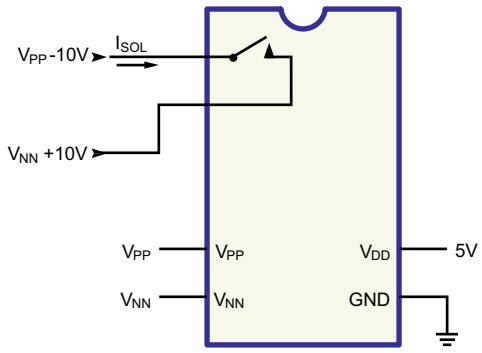
Notes:

1. *The eight switches operate independently.*
2. *Serial data is clocked in on the L to H transition clock.*
3. *The switches go to a state retaining their present condition at the rising edge of the $\overline{LE}$.*
4. *When $\overline{LE}$ is low, the shift register data flows through the latch.*
5. *Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.*
6. *The clear input overrides all other inputs.*

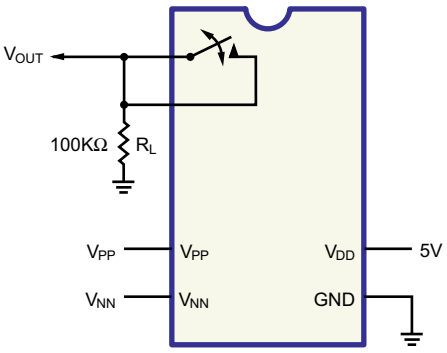
Logic Timing Waveforms



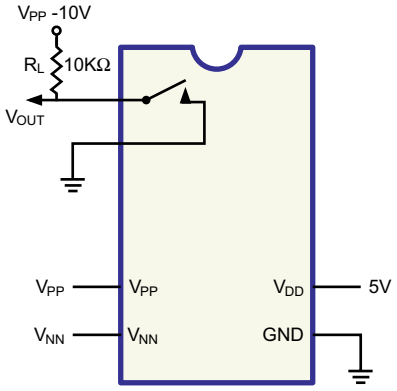
Test Circuits



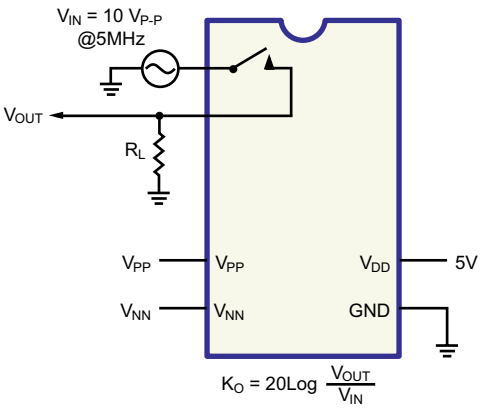
Switch OFF Leakage



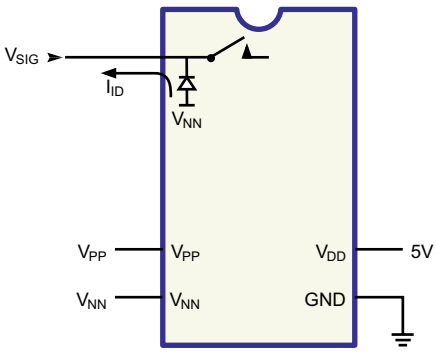
DC Offset ON/OFF



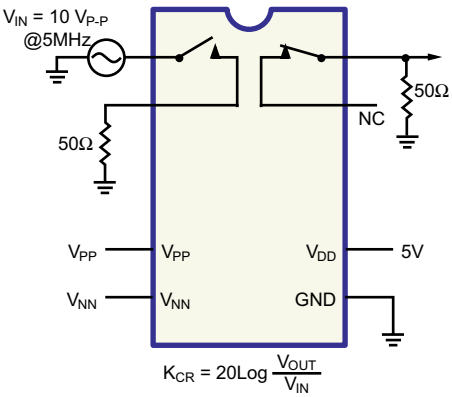
T_{ON}/T_{OFF} Test Circuit



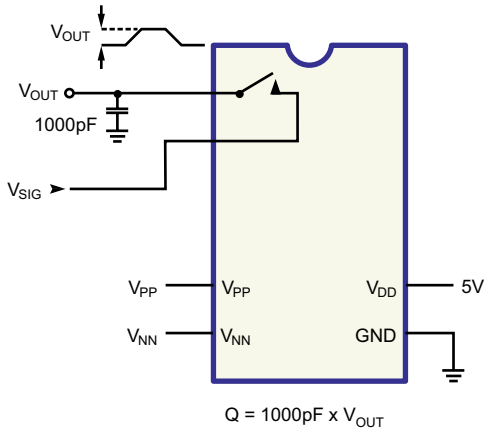
OFF Isolation



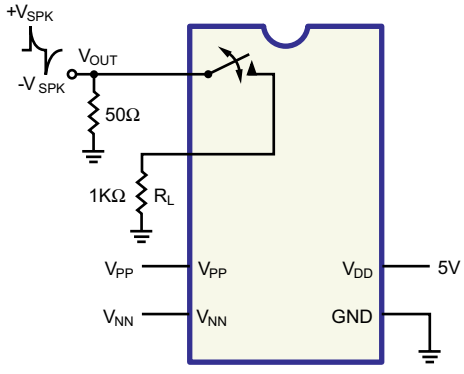
Isolation Diode Current



Crosstalk



Charge Injection



Output Voltage Spike

Pin Description
28-Lead (J-Lead) PLCC (PJ)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	SW3	8	SW0	15	NC	22	SW7
2	SW3	9	NC	16	D_{IN}	23	SW6
3	SW2	10	V_{PP}	17	CLK	24	SW6
4	SW2	11	NC	18	$\overline{LE}$	25	SW5
5	SW1	12	V_{NN}	19	CL	26	SW5
6	SW1	13	GND	20	D_{OUT}	27	SW4
7	SW0	14	V_{DD}	21	SW7	28	SW4

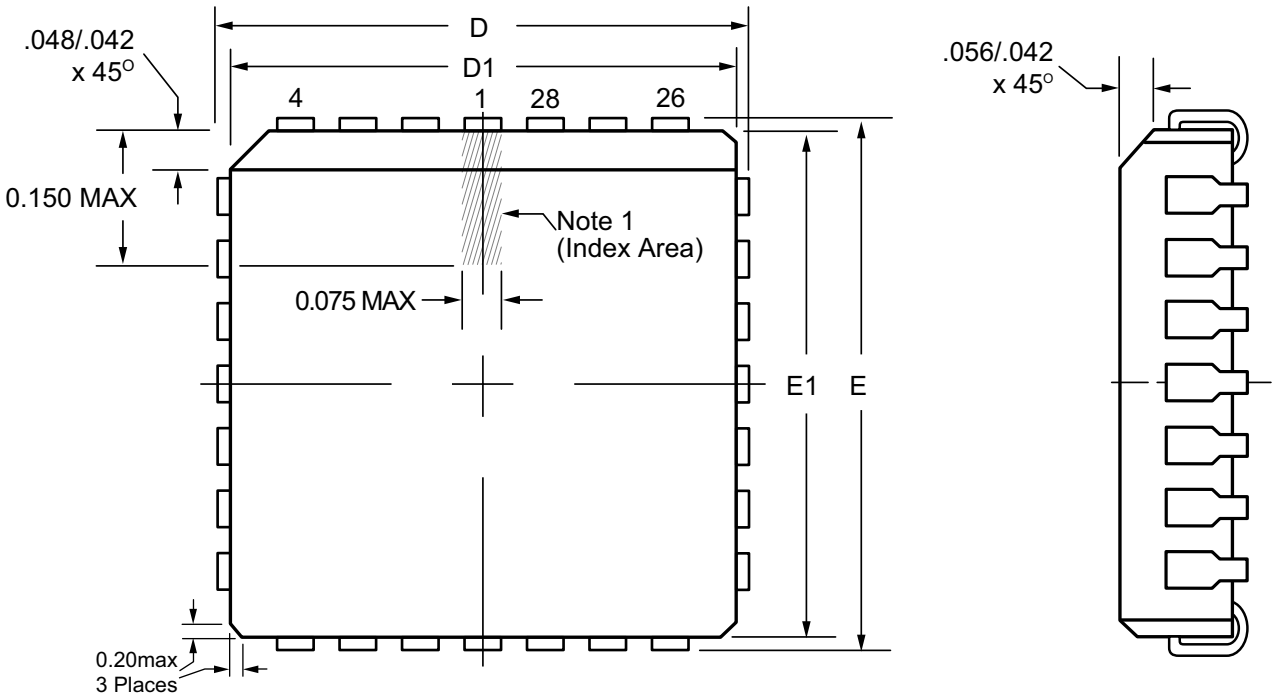
Pin Description
48-Lead LQFP (7x7x1.4mm) (FG)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	SW5	13	NC	25	V_{NN}	37	D_{OUT}
2	NC	14	SW2	26	NC	38	NC
3	SW4	15	NC	27	NC	39	SW7
4	NC	16	SW1	28	GND	40	NC
5	SW4	17	NC	29	V_{DD}	41	SW7
6	NC	18	SW1	30	NC	42	NC
7	NC	19	NC	31	NC	43	SW6
8	SW3	20	SW0	32	NC	44	NC
9	NC	21	NC	33	D_{IN}	45	SW6
10	SW3	22	SW0	34	CLK	46	NC
11	NC	23	NC	35	$\overline{LE}$	47	SW5
12	SW2	24	V_{PP}	36	CLR	48	NC

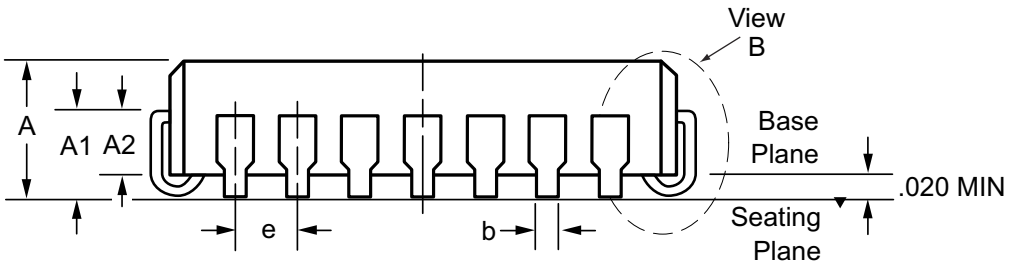
Power Up/Down Sequence

1) Power up/down sequence is arbitrary except GND must be powered up first and powered down last. This applies for applications powering GND of the IC with different voltages.
2) V_{SIG} must always be at or in between V_{PP} and V_{NN} or floating during power up/down transition.
3) Rise and fall times of the power supplies V_{DD}, V_{PP}, and V_{NN} should not be less than 1.0ms.

28-Lead PLCC Package Outline (PJ)



Top View



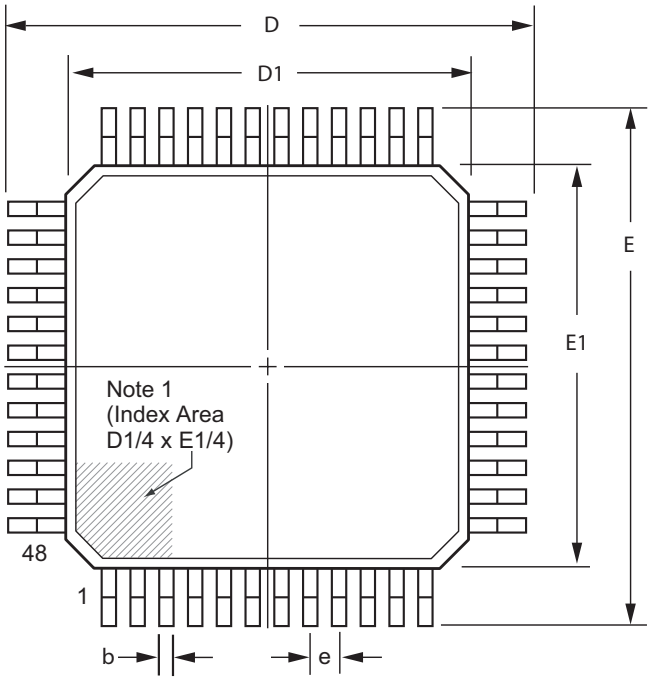
Side View

Note 1:
A Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

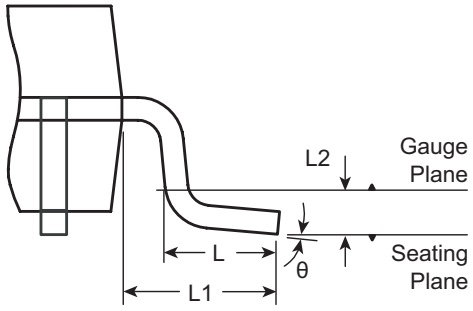
Symbol		A	A1	A2	b	D	D1	E	E1	e
Dimension (inches)	MIN	.165	.090	.062	.013	.485	.450	.485	.450	.050 BSC
	NOM	.172	.105	-	-	.490	.453	.490	.453	
	MAX	.180	.120	.083	.021	.495	.456	.495	.456	

JEDEC Registration MS-018, Variation AB, Issue A, June, 1993.
Drawings not to scale.

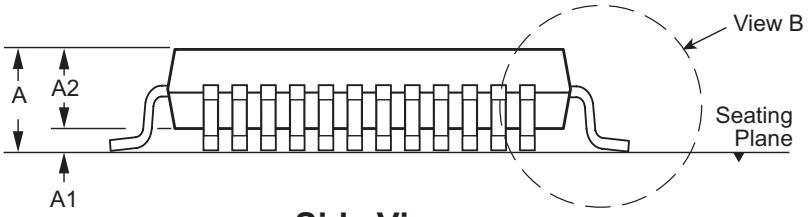
48-Lead LQFP (7x7x1.4mm) Package Outline (FG)



Top View



View B



Side View

Note 1:

A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40	0.05	1.35	0.17	8.80	6.80	8.80	6.80	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20	7.20	9.20	7.20		0.75			7°

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.
Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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