Low Capacitance, Low Charge Injection, ±15 V/+12 V *i*CMOS Quad SPST Switches

Data Sheet

ADG1211/ADG1212/ADG1213

FEATURES

1 pF off capacitance
2.6 pF on capacitance
<1 pC charge injection
33 V supply range
120 Ω on resistance
Fully specified at ±15 V, +12 V
No V_L supply required
3 V logic-compatible inputs
Rail-to-rail operation
16-lead TSSOP and 16-lead LFCSP
Typical power consumption: <0.03 µW

APPLICATIONS

Automatic test equipment
Data acquisition systems
Battery-powered systems
Sample-and-hold systems
Audio signal routing
Video signal routing
Communication systems

GENERAL DESCRIPTION

The ADG1211/ADG1212/ADG1213 are monolithic complementary metal-oxide semiconductor (CMOS) devices containing four independently selectable switches designed on an *i*CMOS® (industrial CMOS) process. *i*CMOS is a modular manufacturing process combining high voltage CMOS and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make the parts suitable for video signal switching.

FUNCTIONAL BLOCK DIAGRAM

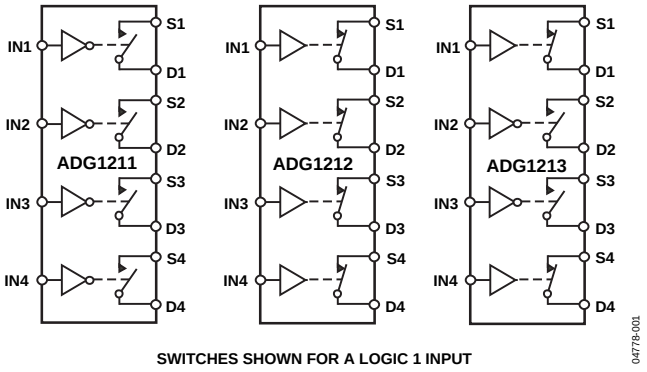

Figure 1.

*i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

The ADG1211/ADG1212/ADG1213 contain four independent single-pole/single-throw (SPST) switches. The ADG1211 and ADG1212 differ only in that the digital control logic is inverted. The ADG1211 switches are turned on with Logic 0 on the appropriate control input, while Logic 1 is required for the ADG1212. The ADG1213 has two switches with digital control logic similar to that of the ADG1211; the logic is inverted on the other two switches. The ADG1213 exhibits break-before-make switching action for use in multiplexer applications.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

PRODUCT HIGHLIGHTS

1. Ultralow capacitance.
2. <1 pC charge injection.
3. 3 V logic-compatible digital inputs: V_{IH} = 2.0 V, V_{IL} = 0.8 V.
4. No V_L logic power supply required.
5. Ultralow power dissipation: <0.03 µW.
6. 16-lead TSSOP and 3 mm × 3 mm LFCSP packages.

Rev. B

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Changes to Power Requirements, I_{DD}, Digital Inputs = 5 V Parameter, Table 2 5

7/05—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	Y Version[1] −40°C to +85°C	Y Version[1] −40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	120			Ω typ	V_S = ±10 V, I_S = −1 mA; see Figure 20
	190	230	260	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between Channels (ΔR_{ON})	2.5			Ω typ	V_S = ±10 V, I_S = −1 mA
	6	10	11	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	20			Ω typ	V_S = −5 V/0 V/+5 V; I_S = −1 mA
	57	72	79	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 21
	±0.1	±0.6	±1	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 21
	±0.1	±0.6	±1	nA max	
Channel On Leakage, I_D, I_S (On)	±0.02			nA typ	V_S = V_D = ±10 V; see Figure 22
	±0.1	±0.6	±1	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	2.5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	110			ns typ	R_L = 300 Ω, C_L = 35 pF
	130	160	195	ns max	V_S = 10 V; see Figure 23
t_{OFF}	85			ns typ	R_L = 300 Ω, C_L = 35 pF
	115	130	150	ns max	V_S = 10 V; see Figure 23
Break-Before-Make Time Delay, t_D (ADG1213 Only)	25			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 10 V; see Figure 24
Charge Injection	−0.3			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 25
Off Isolation	80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 26
Channel-to-Channel Crosstalk	90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
Total Harmonic Distortion + Noise	0.15			% typ	R_L = 10 kΩ, 5 V rms, f = 20 Hz to 20 kHz
−3 dB Bandwidth	1000			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
C_S (Off)	0.9			pF typ	V_S = 0 V, f = 1 MHz
	1.1			pF max	V_S = 0 V, f = 1 MHz
C_D (Off)	1			pF typ	V_S = 0 V, f = 1 MHz
	1.2			pF max	V_S = 0 V, f = 1 MHz
C_D, C_S (On)	2.6			pF typ	V_S = 0 V, f = 1 MHz
	3			pF max	V_S = 0 V, f = 1 MHz

Parameter	25°C	Y Version[1] –40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{DD}	220			µA typ	Digital inputs = 5 V
			380	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 5 V
			1.0	µA max	
VDD/VSS			±4.5/±16.5	V min/max	

[1] Temperature range for Y version is −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	Y Version[1] −40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	300			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA; see Figure 20
	475	567	625	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between Channels (ΔR_{ON})	4.5			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	12	26	27	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	60			Ω typ	V_S = 3 V/6 V/9 V, I_S = −1 mA
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 21
	±0.1	±0.6	±1	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 21
	±0.1	±0.6	±1	nA max	
Channel On Leakage, I_D, I_S (On)	±0.02			nA typ	V_S = V_D = 1 V or 10 V; see Figure 22
	±0.1	±0.6	±1	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	130			ns typ	R_L = 300 Ω, C_L = 35 pF
	170	210	240	ns max	V_S = 8 V; see Figure 23
t_{OFF}	95			ns typ	R_L = 300 Ω, C_L = 35 pF
	120	145	180	ns max	V_S = 8 V; see Figure 23
Break-Before-Make Time Delay, t_D	50			ns typ	R_L = 300 Ω, C_L = 35 pF
(ADG1213 Only)			10	ns min	V_{S1} = V_{S2} = 8 V; see Figure 24
Charge Injection	0			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 25
Off Isolation	80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 26
Channel-to-Channel Crosstalk	90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
−3 dB Bandwidth	900			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
C_S (Off)	1.2			pF typ	V_S = 6 V, f = 1 MHz
	1.4			pF max	V_S = 6 V, f = 1 MHz
C_D (Off)	1.3			pF typ	V_S = 6 V, f = 1 MHz
	1.5			pF max	V_S = 6 V, f = 1 MHz
C_D, C_S (On)	3.2			pF typ	V_S = 6 V, f = 1 MHz
	3.9			pF max	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{DD}	220			μA typ	Digital inputs = 5 V
			1.0	μA max	
VDD			5/165	V min/max	V_{SS} = 0 V, GND = 0 V

[1] Temperature range for Y version is −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current per Channel, S or D	25 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance (4-Layer Board)	112°C/W
16-Lead LFCSP, θ_{JA} Thermal Impedance	72.7°C/W
Reflow Soldering Peak Temperature, Pb free	260°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

Table 4. ADG1211/ADG1212 Truth Table

ADG1211 INx	ADG1212 INx	Switch Condition
0	1	On
1	0	Off

Table 5. ADG1213 Truth Table

ADG1213 INx	Switch 1, 4	Switch 2, 3
0	Off	On
1	On	Off

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

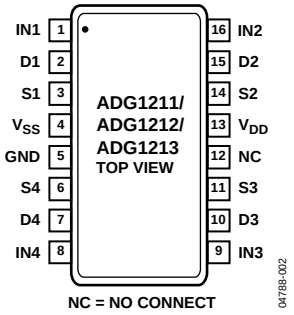

Figure 2. TSSOP Pin Configuration

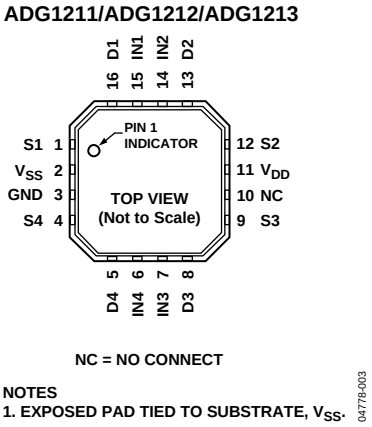

Figure 3. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	IN1	Logic Control Input.
2	16	D1	Drain Terminal. Can be an input or output.
3	1	S1	Source Terminal. Can be an input or output.
4	2	V_{SS}	Most Negative Power Supply Potential.
5	3	GND	Ground (0 V) Reference.
6	4	S4	Source Terminal. Can be an input or output.
7	5	D4	Drain Terminal. Can be an input or output.
8	6	IN4	Logic Control Input.
9	7	IN3	Logic Control Input.
10	8	D3	Drain Terminal. Can be an input or output.
11	9	S3	Source Terminal. Can be an input or output.
12	10	NC	No Internal Connection.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	S2	Source Terminal. Can be an input or output.
15	13	D2	Drain Terminal. Can be an input or output.
16	14	IN2	Logic Control Input.

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D (V_S)
The analog voltage on Terminals D and S.

R_{ON}
The ohmic resistance between D and S.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL} (I_{INH})
The input current of the digital input.

C_S (Off)
The off switch source capacitance, measured with reference to ground.

C_D (Off)
The off switch drain capacitance, measured with reference to ground.

C_D, C_S (On)
The on switch capacitance, measured with reference to ground.

C_{IN}
The digital input capacitance.

t_{ON}
The delay between applying the digital control input and the output switching on. See Figure 23.

t_{OFF}
The delay between applying the digital control input and the output switching off. See Figure 23.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

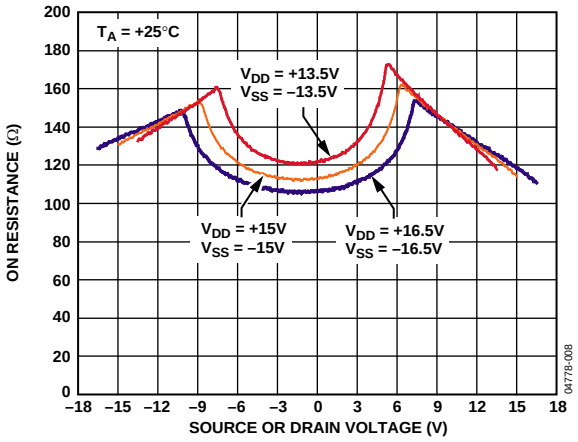

Figure 4. On Resistance as a Function of V_D (V_S) for Dual Supply

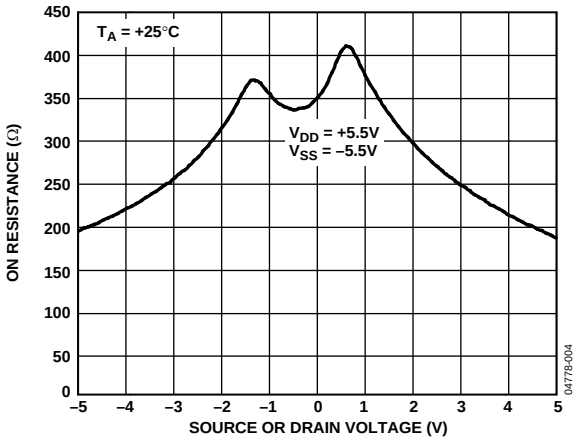

Figure 5. On Resistance as a Function of V_D (V_S) for Dual Supply

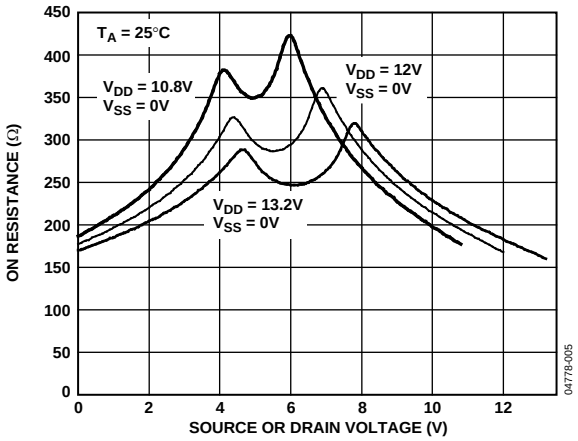

Figure 6. On Resistance as a Function of V_D (V_S) for Single Supply

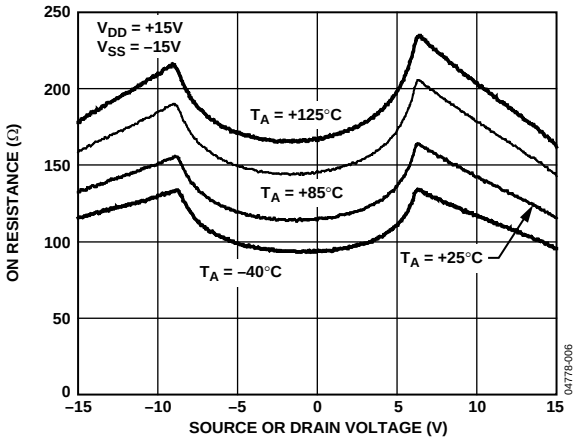

Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

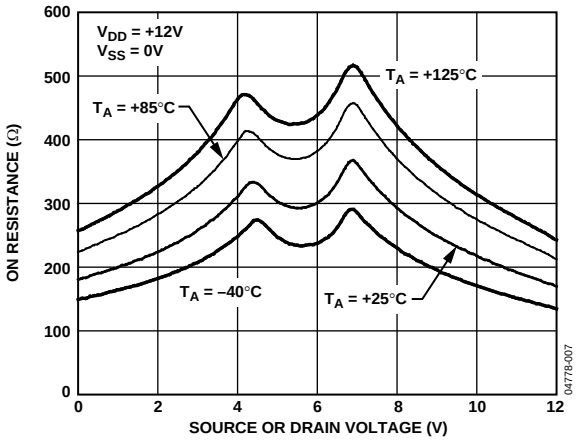

Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

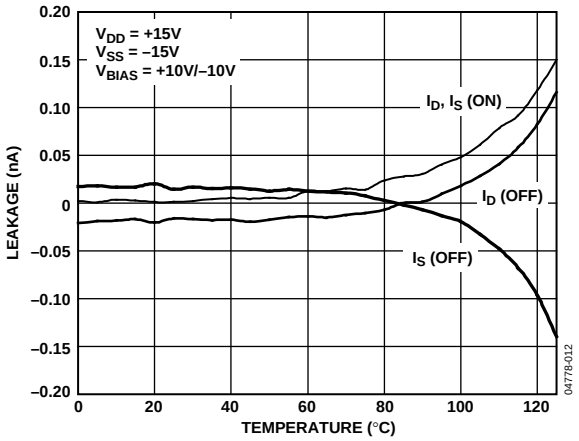

Figure 9. Leakage Currents as a Function of Temperature, Dual Supply

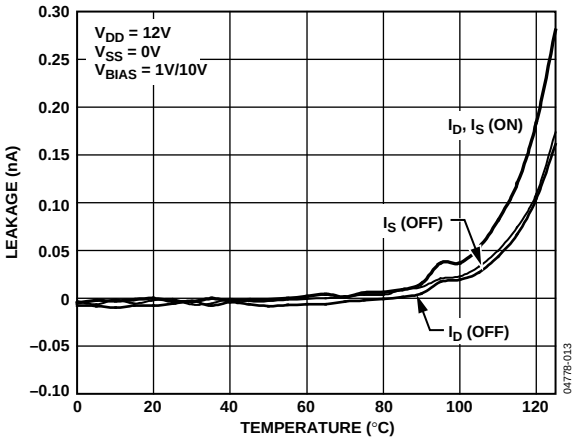

Figure 10. Leakage Currents as a Function of Temperature, Single Supply

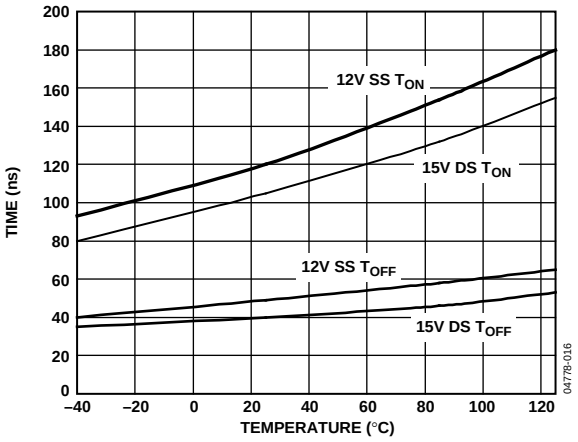

Figure 13. T_{ON}/T_{OFF} Times vs. Temperature

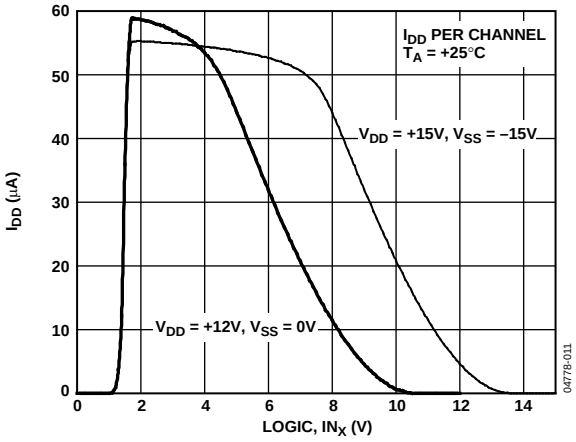

Figure 11. I_{DD} vs. Logic Level

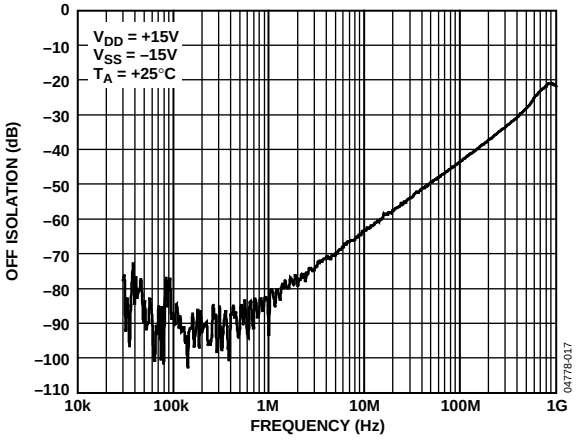

Figure 14. Off Isolation vs. Frequency

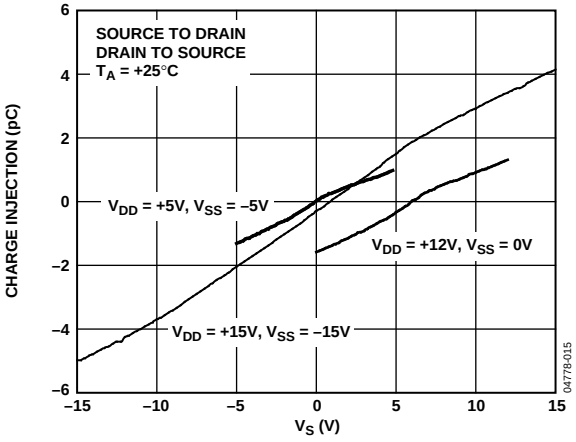

Figure 12. Charge Injection vs. Source Voltage

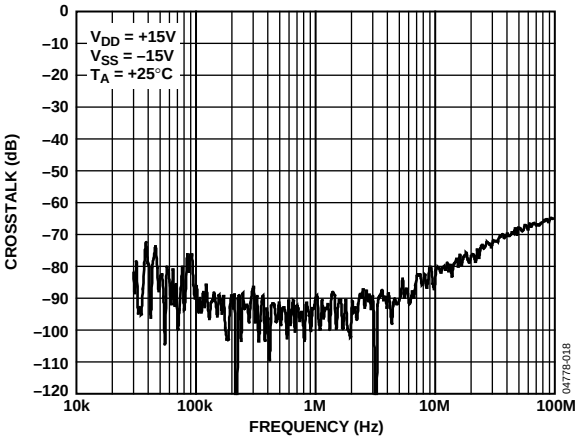

Figure 15. Crosstalk vs. Frequency

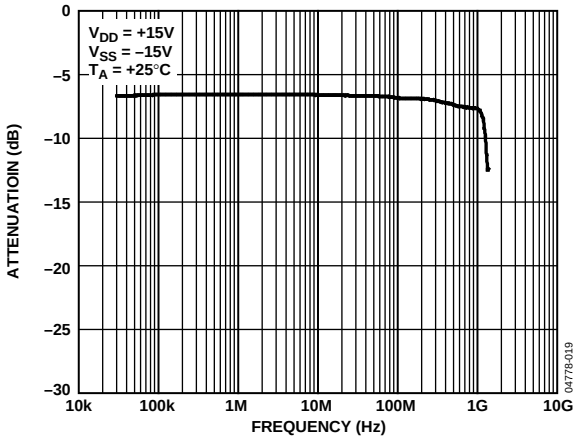

Figure 16. On Response vs. Frequency

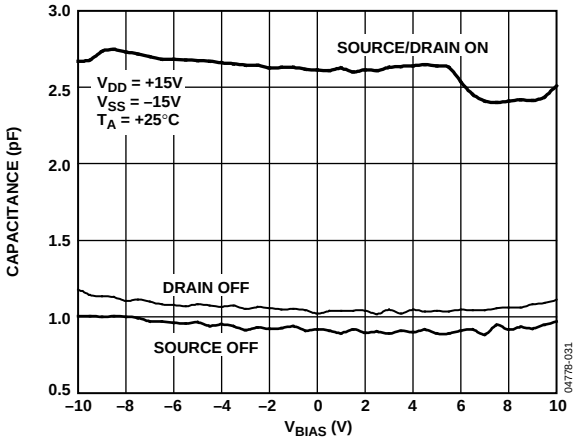

Figure 18. Capacitance vs. Source Voltage, Dual Supply

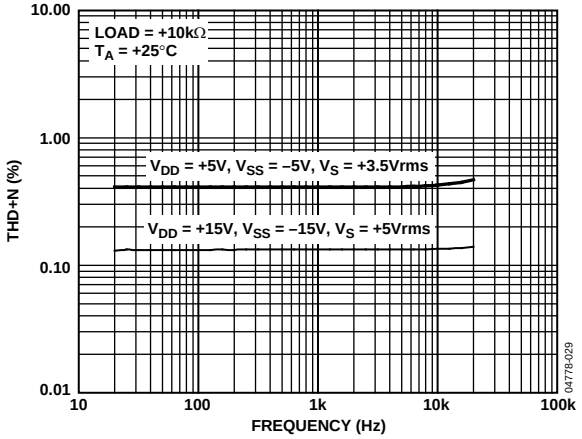

Figure 17. THD + N vs. Frequency

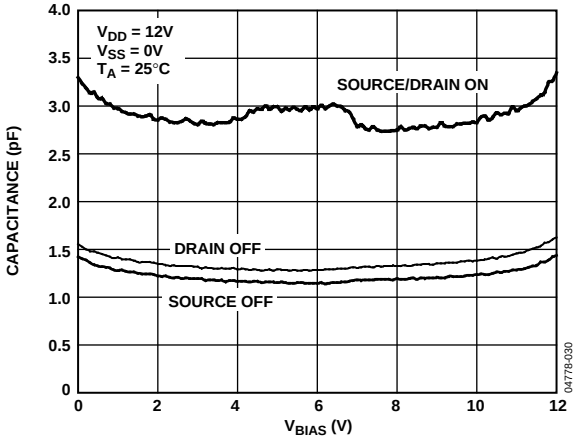

Figure 19. Capacitance vs. Source Voltage, Single Supply

TEST CIRCUITS

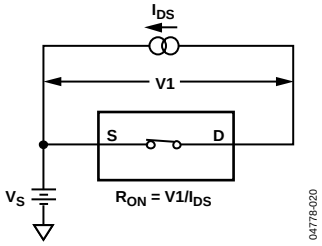

Figure 20. On Resistance

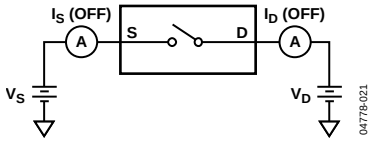

Figure 21. Off Leakage

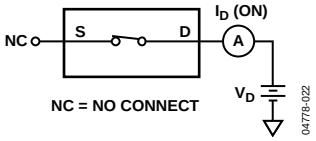

Figure 22. On Leakage

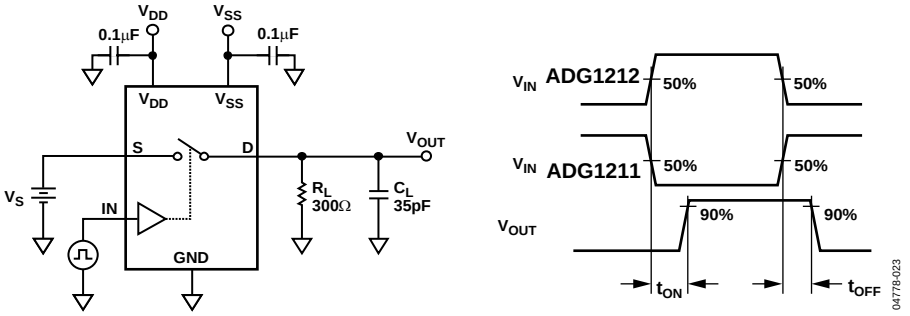

Figure 23. Switching Times

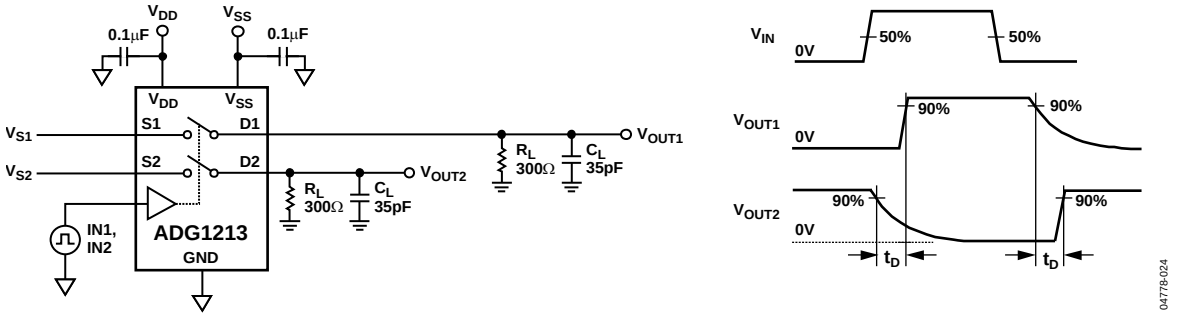

Figure 24. Break-Before-Make Time Delay

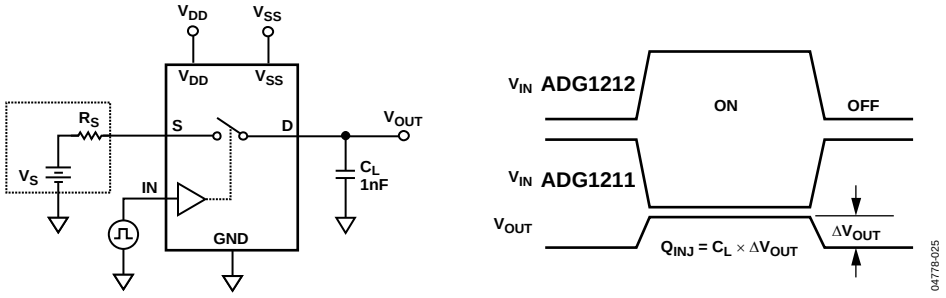

Figure 25. Charge Injection

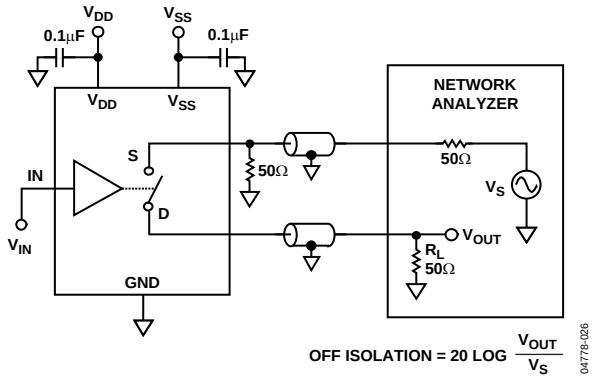

Figure 26. Off Isolation

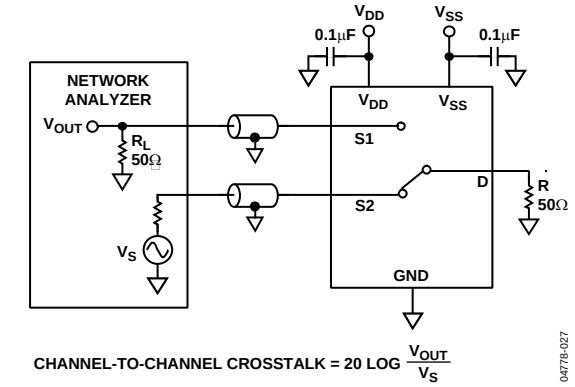

Figure 27. Channel-to-Channel Crosstalk

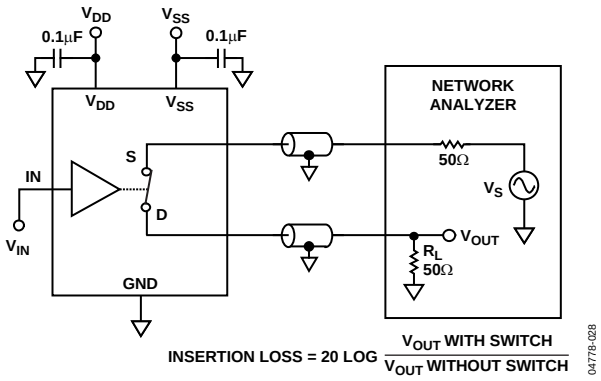

Figure 28. Bandwidth

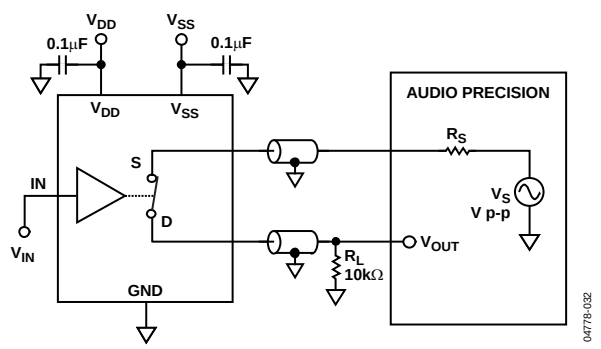

Figure 29. THD + Noise

OUTLINE DIMENSIONS

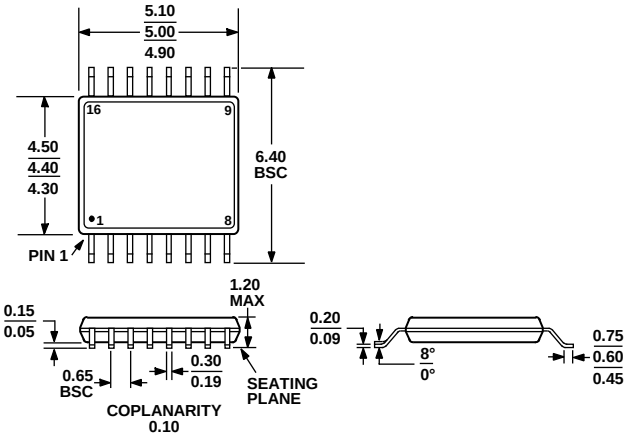

Figure 30. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

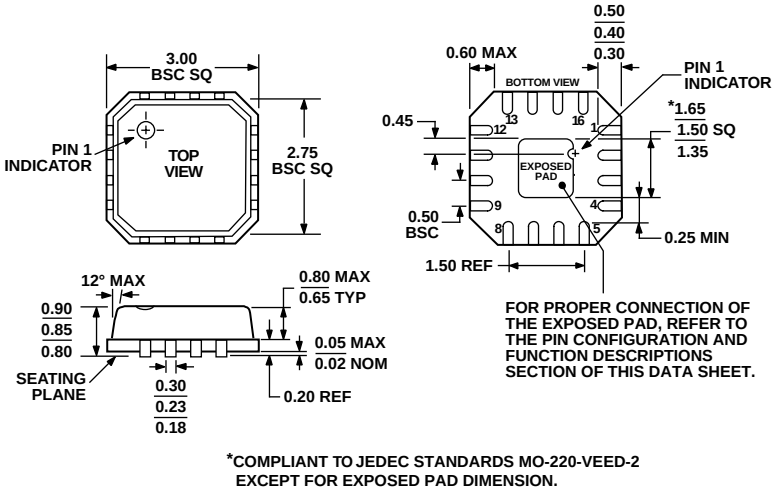

Figure 31. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADG1211YRUZ	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16	
ADG1211YRUZ-REEL	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16	
ADG1211YRUZ-REEL7	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16	
ADG1211YCPZ-500RL7	−40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-3	S07
ADG1211YCPZ-REEL7	−40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-3	S07
ADG1212YRUZ	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16	
ADG1212YRUZ-REEL	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16	
ADG1212YRUZ-REEL7	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16	
ADG1212YCPZ-500RL7	−40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-3	S08
ADG1212YCPZ-REEL7	−40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-3	S08
ADG1213YRUZ	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16	
ADG1213YRUZ-REEL	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16	
ADG1213YRUZ-REEL7	−40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16	
ADG1213YCPZ-500RL7	−40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-3	S09
ADG1213YCPZ-REEL7	−40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-3	S09

[1] Z = RoHS Compliant Part.

NOTES

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