ATP Electronics, Inc.
2590 North First Street, San Jose, CA 95131, U.S.A.
Tel: 408-732-5000
Fax: 408-732-5055
http://www.atpinc.com

Rev. Date: Apr. 26, 2017

ATP A4B32QB4BNTDSE

32GB DDR4-2666 REGISTERED ECC DIMM

DESCRIPTION

The ATP A4B32QB4BNTDSE is a high performance 32GB DDR4-2666 Registered ECC SDRAM memory module. It is organized as 4096M x 72 in a 288-pin Dual-In-Line Memory Module (DIMM) package. The module utilizes thirty-six 2048Mx4 DDR4 SDRAMs in FBGA package. The module consists of a 512-byte serial EEPROM, which contains the module configuration information.

KEY FEATURES

- High Density: 32GB (4096M x 72)
- DIMM Rank: 2 Rank
- Cycle Time: 0.75ns (1333MHz)
- CAS Latency: 19(DDR4-2666),17(DDR4-2400),15(DDR4-2133)
- Power supply: V_{DD}=1.2V ± 0.06V
  V_{PP}=2.5V± 0.125V
  V_{DDSPD}=2.2V~3.6V
- Support ECC error detection and correction
- Nominal and dynamic on-die termination(ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion(DBI) for data bus
- 16 internal banks(x4); 4 groups of 4 banks each
- Internal self calibration through ZQ
- Temperature controlled refresh (TCR)
- Asynchronous Reset
- 7.8 μs refresh interval at lower than T_{CASE}85°C, 3.9μs refresh interval at 85°C < T_{CASE} < 95 °C
- Support address and command signals parity function
- Selectable BC4 or BL8 on-the fly(OTF)
- Dynamic On Die Termination
- Fly-by topology
- PCB Height: 1.23 inches(31.25mm)
- Minimum Thickness of Golden Finger: 30 Micro-inch
- RoHS compliant

Part No.	Max Freq	Interface
A4B32QB4BNTDSE	1333MHz (0.75ns@CL=19) x2	POD12

Your Ultimate Memory Solution!

PIN DESCRIPTION

Pin Name	Description
A0~A17	Address Inputs
A10/AP	Address Input/Auto precharge
A12/BC_n	Address Input/Burst chop
BA0,BA1	SDRAM Bank Address
BG0,BG1	Bank group address inputs
RAS_n	Row address strobe input
CAS_n	Column address strobe input
WE_n	Write enable input
CS0_n	Chip Selects
CK0_t	Clock Inputs, positive line
CK0_c	Clock Inputs, negative line
C0~C2	Chip ID
CKE0	Clock Enables
ODT0	On-die termination control lines input
ACT_n	Command input: ACT_n indicates an ACTIVATE command.
DQ0~DQ63	Data Input /Output
CB0~CB7	Data check bits Input/Output
DQS0_t~DQS8_t	Data strobes
DQS0_c~DQS8_c	Data strobes, negative line
SCL	Serial clock for temperature sensor/SPD EEPROM
SDA	SPD Data Input /Output
SA0~SA2	Serial address inputs
PARITY	Parity for command and address
VDD	Power supply
VPP	DRAM activating power supply
VREFCA	Reference voltage for control, command, and address pins.
VSS	Ground
VDDSPD	SPD Power
ALERT_n	Alert output
RESET_n	Active LOW asynchronous reset
EVENT_n	Temperature sensor Event Output
VTT	SDRAM I/O termination supply
VDDQ	DRAM DQ power supply
ZQ	Reference ball for ZQ calibration
NC	No Connect
NF	No function
RFU	Reserved for future use

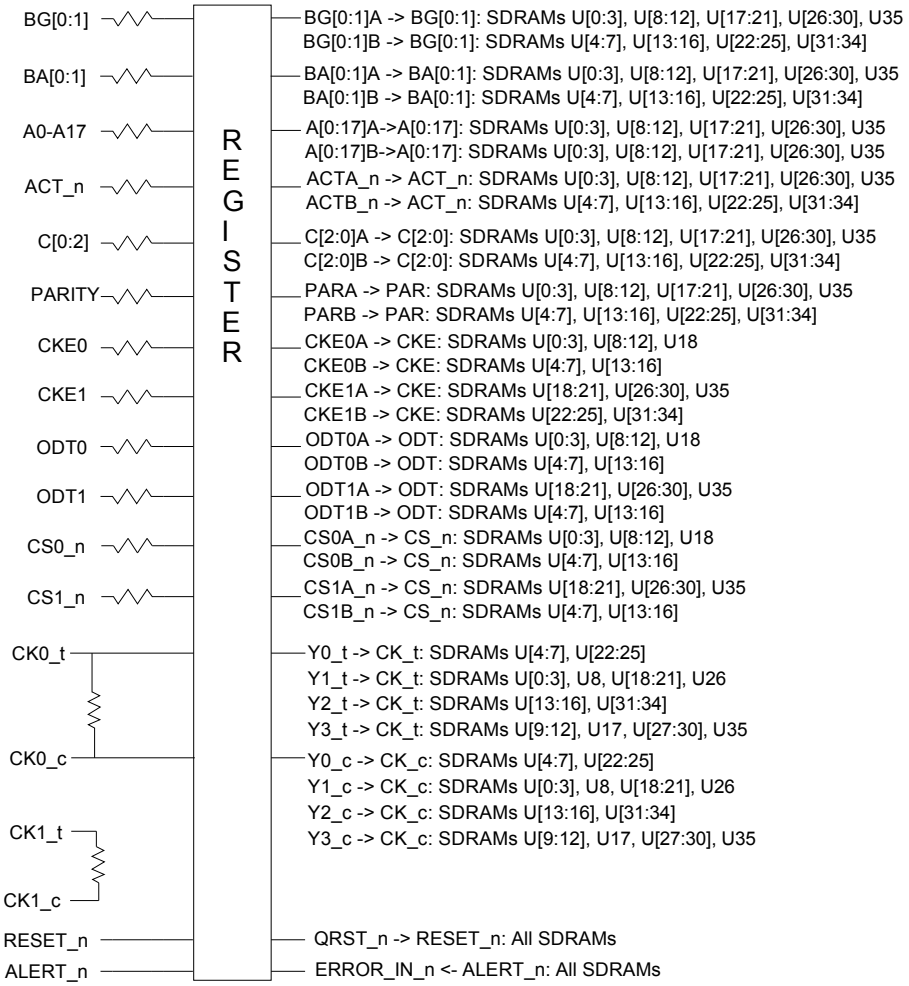
PIN ASSIGNMENT

No.	Designation	No.	Designation	No.	Designation	No.	Designation
1	NC	145	NC	74	CK0_t	218	CK1_t
2	VSS	146	VREFCA	75	CK0_c	219	CK1_c
3	DQ4	147	VSS	76	VDD	220	VDD
4	VSS	148	DQ5	77	VTT	221	VTT
5	DQ0	149	VSS	KEY			
6	VSS	150	DQ1	78	EVENT_n	222	PARITY
7	TDQS9_t, DQS9_t	151	VSS	79	A0	223	VDD
8	TDQS9_c, DQS9_c	152	DQS0_c	80	VDD	224	BA1
9	VSS	153	DQS0_t	81	BA0	225	A10/AP
10	DQ6	154	VSS	82	RAS_n/A16	226	VDD
11	VSS	155	DQ7	83	VDD	227	RFU
12	DQ2	156	VSS	84	S0_n	228	WE_n /A14
13	VSS	157	DQ3	85	VDD	229	VDD
14	DQ12	158	VSS	86	CAS_n/A15	230	NC
15	VSS	159	DQ13	87	ODT0	231	VDD
16	DQ8	160	VSS	88	VDD	232	A13
17	VSS	161	DQ9	89	S1_n	233	VDD
18	TDQS10_t, DQS10_t	162	VSS	90	VDD	234	A17
19	TDQS10_c, DQS10_c	163	DQS1_c	91	ODT1	235	NC,C2
20	VSS	164	DQS1_t	92	VDD	236	VDD
21	DQ14	165	VSS	93	C0,CS2_n,NC	237	NC,CS3_c,C1
22	VSS	166	DQ15	94	VSS	238	SA2
23	DQ10	167	VSS	95	DQ36	239	VSS
24	VSS	168	DQ11	96	VSS	240	DQ37
25	DQ20	169	VSS	97	DQ32	241	VSS
26	VSS	170	DQ21	98	VSS	242	DQ33
27	DQ16	171	VSS	99	TDQS13_t, DQS13_t	243	VSS
28	VSS	172	DQ17	100	TDQS13_c, DQS13_c	244	DQS4_c
29	TDQS11_t, DQS11_t	173	VSS	101	VSS	245	DQS4_t
30	TDQS11_c, DQS11_c	174	DQS2_c	102	DQ38	246	VSS
31	VSS	175	DQS2_t	103	VSS	247	DQ39
32	DQ22	176	VSS	104	DQ34	248	VSS
33	VSS	177	DQ23	105	VSS	249	DQ35
34	DQ18	178	VSS	106	DQ44	250	VSS
35	VSS	179	DQ19	107	VSS	251	DQ45
36	DQ28	180	VSS	108	DQ40	252	VSS
37	VSS	181	DQ29	109	VSS	253	DQ41
38	DQ24	182	VSS	110	TDQS14_t, DQS14_t	254	VSS
39	VSS	183	DQ25	111	TDQS14_c, DQS14_c	255	DQS5_c
40	TDQS12_t, DQS12_t	184	VSS	112	VSS	256	DQS5_t
41	TDQS12_c, DQS12_c	185	DQS3_c	113	DQ46	257	VSS

No.	Designation	No.	Designation	No.	Designation	No.	Designation
42	VSS	186	DQS3_t	114	VSS	258	DQ47
43	DQ30	187	VSS	115	DQ42	259	VSS
44	VSS	188	DQ31	116	VSS	260	DQ43
45	DQ26	189	VSS	117	DQ52	261	VSS
46	VSS	190	DQ27	118	VSS	262	DQ53
47	CB4	191	VSS	119	DQ48	263	VSS
48	VSS	192	VB5	120	VSS	264	DQ49
49	CB0	193	VSS	121	TDQS15_t, DQS15_t	265	VSS
50	VSS	194	CB1	122	TDQS15_c, DQS15_c	266	DQS6_c
51	TDQS17_t, DQS17_t	195	VSS	123	VSS	267	DQS6_t
52	TDQS17_c, DQS17_c	196	DQS8_c	124	DQ54	268	VSS
53	VSS	197	DQS8_t	125	VSS	269	DQ55
54	CB6	198	VSS	126	DQ50	270	VSS
55	VSS	199	VB7	127	VSS	271	DQ51
56	CB2	200	VSS	128	DQ60	272	VSS
57	VSS	201	CB3	129	VSS	273	DQ61
58	RESET_n	202	VSS	130	DQ56	274	VSS
59	VDD	203	CKE1	131	VSS	275	DQ57
60	CKE0	204	VDD	132	TDQS16_t, DQS16_t	276	VSS
61	VDD	205	RFU	133	TDQS16_c, DQS16_c	277	DQS7_c
62	ACT_n	206	VDD	134	VSS	278	DQS7_t
63	BG0	207	BG1	135	DQ62	279	VSS
64	VDD	208	ALERT_n	136	VSS	280	DQ63
65	A12/BC_n	209	VDD	137	DQ58	281	VSS
66	A9	210	A11	138	VSS	282	DQ59
67	VDD	211	A7	139	SA0	283	VSS
68	A8	212	VDD	140	SA1	284	VDDSPD
69	A6	213	A5	141	SCL	285	SDA
70	VDD	214	A4	142	VPP	286	VPP
71	A3	215	VDD	143	VPP	287	VPP
72	A1	216	A2	144	RFU	288	VPP
73	VDD	217	VDD				

Note:
1. VPP is 2.5V DC

FUNCTIONAL BLOCK DIAGRAM (PART1 OF 3)

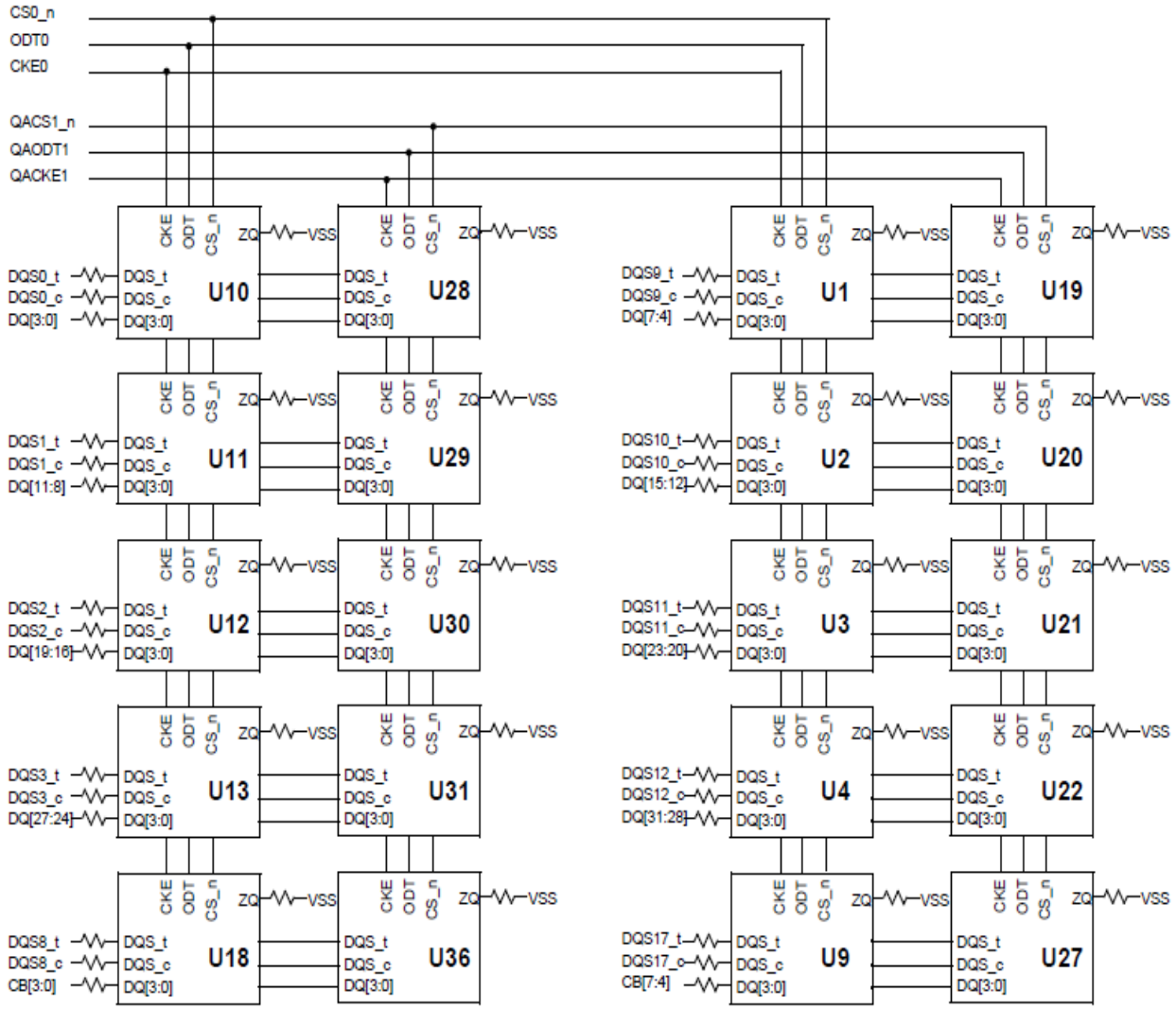


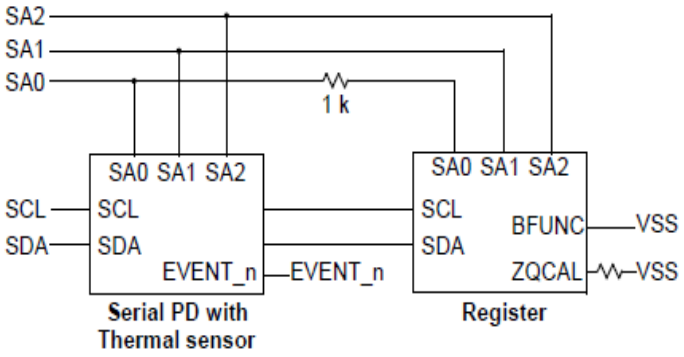
Note 1 CK0_t, CK0_c terminated with 120± 5% resistor.

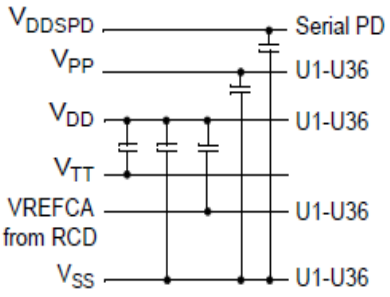
Note 2 CK1_t, CK1_c terminated with 120± 5% resistor but not used.

Note 3 Unless otherwise noted resistors are 22± 5%.

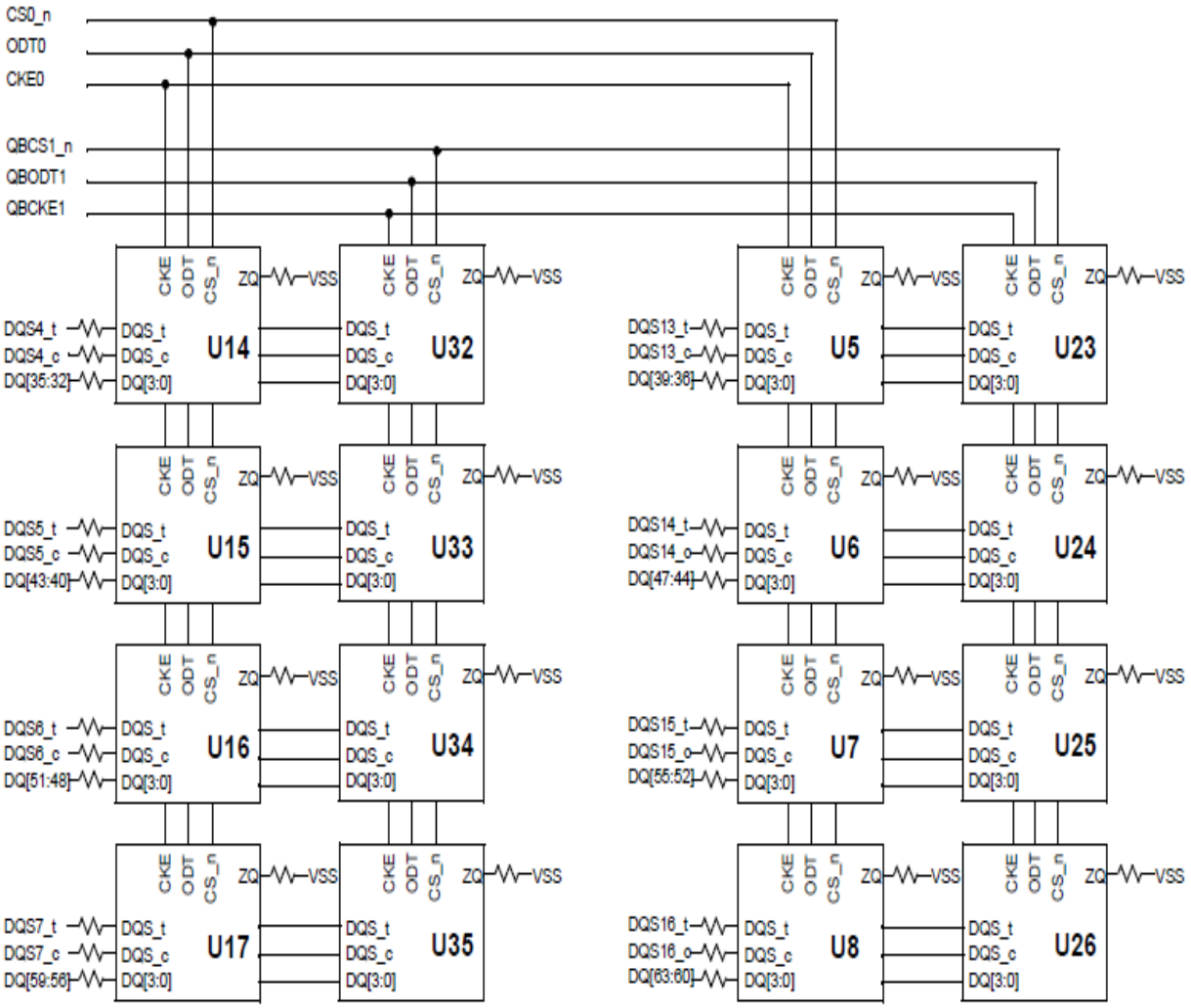
FUNCTIONAL BLOCK DIAGRAM (PART2 OF 3)







FUNCTIONAL BLOCK DIAGRAM (PART3 OF 3)



Note 1 Unless otherwise noted, resistor values are 15± 5%.
Note 2 See the Net Structure diagrams for all resistors associated with the command, address and control bus.
Note 3 ZQ resistors are 240 ± 1%. For all other resistor values refer to the appropriate wiring diagram.
Note 4 DRAM TEN pin need to be tied to Vss.
Note 5 VDDSPD also connects to the register (RCD).
Note 6 VREFCA from the edge connector only connects with the register (RCD). The RCD sources a separate VREFCA to all the SDRAMs.

ABSOLUTE MAXIMUM DC RATINGS

Item	Symbol	Rating	Units	Notes
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-0.4V ~ 1.5V	V	1,3
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.5V	V	1,3
Voltage on V_{PP} pin relative to V_{SS}	V_{PP}	-0.4V ~ 3.0V	V	4
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4V ~ 1.975V	V	1
Storage Temperature	T_{STG}	-55 to +100	°C	1,2
Operating Temperature	T_{CASE}	0 to +95	°C	1,2

Note:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.

AC & DC OPERATING CONDITIONS

Recommended operating conditions

Item	Symbol	Min.	Typical	Max.	Units
Supply Voltage [1,2,3]	V_{DD}	1.14	1.2	1.26	V
Supply Voltage for Output [1,2,3]	V_{DDQ}	1.14	1.2	1.26	V
DRAM Activating Power Supply[3]	V_{PP}	2.375	2.5	2.75	V
Input reference voltage command/ address bus	V_{REFCA}(DC)	TBD	TBD	TBD	V
Termination reference voltage (DC) – command/address bus[4]	V_{TT}	0.49 * V_{DD}- 20mA	0.50 * V_{DD}	0.51 * V_{DD}+ 20mA	V
Input High Voltage (DC)	V_{IH} (DC)	TBD	-	TBD	V
Input Low Voltage (DC)	V_{IL} (DC)	TBD	-	TBD	V
Input High Voltage (AC)	V_{IH} (AC)	TBD	-	-	V
Input Low Voltage (AC)	V_{IL} (AC)	-	-	TBD	V

Note:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.
4. VTT termination voltages in excess of specification limit will adversely affect command and address signals' voltage margins, and reduce timing margins.

RELIABILITY

MTBF @25 °C (Hours) [1]	FIT @ 25 °C [2]	MTBF @40 °C (Hours) [1]	FIT @ 40 °C [2]
1,783,000	391	987,100	758

Note:
1. The Mean Time between Failures (MTBF) is calculated using a prediction methodology, Bellcore Prediction, which based on reliability data of the individual components in the module. It assumes nominal voltage, with all other parameters within specified range.
2. Failures per Billion Device-Hours

IDD SPECIFICATION PARAMETER & POWER CONSUMPTION (PART1 OF 2)

(Values are for the DDR4 SDRAM only and are computed from values specified in the vendor' s component data sheet)

Symbol	Proposed Conditions	Value	Units
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1,510	mA
IPP0	**Operating One Bank Active-Precharge IPP Current** Same condition with IDD0	126	mA
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: sta-ble at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1,903	mA
IDD2N	**Precharge Standby Current (AL=0)** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1,300	mA
IDD2NT	**Precharge Standby ODT Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern	1,400	mA
IDD2P	**Precharge Power-Down Current** CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	730	mA
IDD2Q	**Precharge Quiet Standby Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	1,230	mA
IDD3N	**Active Standby Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern	1,760	mA
IPP3N	**Active Standby IPP Current** Same condition with IDD3N	108	mA
IDD3P	**Active Power-Down Current** CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	880	mA
IDD4R	**Operating Burst Read Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	2,830	mA

IDD SPECIFICATION PARAMETER & POWER CONSUMPTION (PART2 OF 2)

(Values are for the DDR4 SDRAM only and are computed from values specified in the vendor' s component data sheet)

Symbol	Proposed Conditions	Value	Units
IDD4W	**Operating Burst Write Current** CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	2,710	mA
IDD5B	**Burst Refresh Current (1X REF)** CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	4,730	mA
IPP5B	**Burst Refresh Write IPP Current (1X REF)** Same condition with IDD5B	378	mA
IDD6N	**Self Refresh Current: Normal Temperature Range** TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	890	mA
IDD6E	**Self-Refresh Current: Extended Temperature Range)** TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	1,250	mA
IDD6R	**Self-Refresh Current: Reduced Temperature Range** TCASE: 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	640	mA
IDD6A	**Auto Self-Refresh Current** TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	840	mA
IDD7	**Operating Bank Interleave Read Current** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	4,790	mA
IPP7	**Operating Bank Interleave Read IPP Current** Same condition with IDD7	216	mA
IDD8	**Maximum Power Down Current**	405	mA
PDIMM	**Power Consumption per DIMM** System is operating at 1067MHz clock with VDD = 1.2V. This parameter is calculated at a common loading.	5,748	mW

TIMING PARAMETER

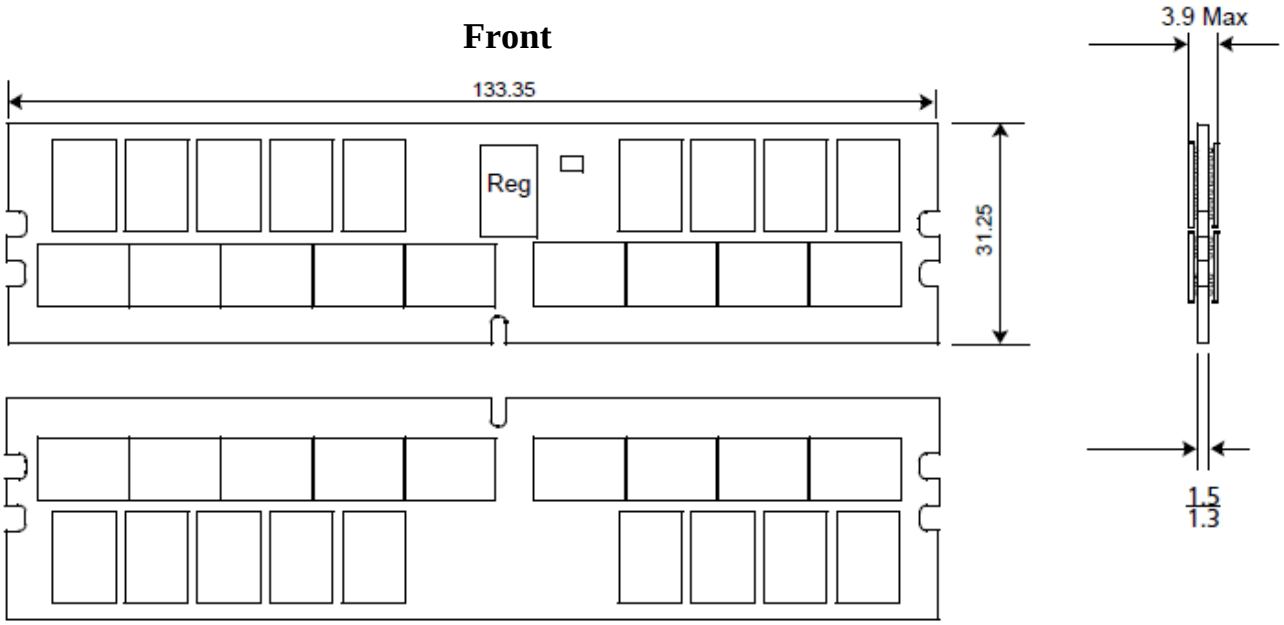
Parameter	Symbol	DDR4-2666		Units
		Min	Max	
Clock cycle time at CL=17, CWL=12	tCK	0.75	<0.833	ns
Internal read command to first data	tAA	14.25	18	ns
ACT to internal read or write delay time	tRCD	14.25		ns
PRE command period	tRP	14.25		ns
ACT to ACT or REF command period	tRC	46.25		ns
ACTIVE to PRECHARGE command period	tRAS	32	9*tREFI	ns
Average clock high pulse width	tCH(avg)	0.48	0.52	tCK
Average clock low pulse width	tCL(avg)	0.48	0.52	tCK
DQS, $\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	-	0.18	ps
DQ output hold time from DQS, $\overline{DQS}$	tQH	0.74	-	tCK
DQ low-impedance time from CK, $\overline{CK}$	tLZ(DQ)	-310	170	ps
DQ high-impedance time from CK, $\overline{CK}$	tHZ(DQ)	-	170	ps
DQS, $\overline{DQS}$ READ Preamble	tRPRE	0.9	TBD	tCK
DQS, $\overline{DQS}$ differential READ Postamble	tRPST	0.33	TBD	tCK
DQS, $\overline{DQS}$ output high time	tQSH	0.4	-	tCK
DQS, $\overline{DQS}$ output low time	tQSL	0.4	-	tCK
DQS, $\overline{DQS}$ WRITE Preamble	tWPRE	0.9	-	tCK
DQS, $\overline{DQS}$ WRITE Postamble	tWPST	0.33	TBD	tCK
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	tLZ(DQS)	-310	170	ps
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	170	ps
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL	0.46	0.54	tCK
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH	0.46	0.54	tCK
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	tDQSS	-0.27	0.27	tCK
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	tDSS	0.18	-	tCK
DQS, $\overline{DQS}$ falling edge hold time to CK, $\overline{CK}$ rising edge	tDSH	0.18	-	tCK
DLL locking time	tDLLK	854	-	nCK[1]
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	
Delay from start of internal write trans-action to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	
Delay from start of internal write trans-action to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Mode Register Set command cycle time	tMRD	8	-	nCK[1]
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	
$\overline{CAS}$ to $\overline{CAS}$ command delay for same bank group	tCCD_L	max(5 nCK, 5 ns)	-	nCK[1]
$\overline{CAS}$ to $\overline{CAS}$ command delay for different bank group	tCCD_S	4		
Auto precharge write recovery + precharge time	tDAL	tWR + roundup (tRP / tCK)		nCK[1]
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK[1]
ACTIVE to ACTIVE command delay to same bank group for 1KB page size	tRRD	max(4nCK,4.9ns)	-	
Four activate window for 1KB page size	tFAW	max(20nCK,21ns)	-	
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIS(base)	TBD	-	ps
Command and Address hold time from CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	tIH(base)	TBD	-	ps
Power-up and RESET calibration time	tZQinit	1024	-	nCK[1]
Normal operation Full calibration time	tZQoper	512	-	nCK[1]
Normal operation short calibration time	tZQCS	128	-	nCK[1]
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)	-	nCK[1]
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK,6ns)	-	nCK[1]
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1	9	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1	9	ns
RTT dynamic change skew	tADC	0.3	0.7	tCK
8Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	350	-	ns
Average periodic refresh interval (0°C ≤ TCASE ≤ 85 °C)	tREFI	7.8	7.8	us
Average periodic refresh interval (85°C ≤ TCASE ≤ 95 °C)	tREFI	3.9	3.9	us
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	nCK[1]
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCK
Write leveling output delay	tWLO	0	9.5	ns
Write leveling output error	tWLOE	0	2	ns

Note:
1. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

PHYSICAL DIMENSIONS (UNITS IN INCHES)

(Drawing not to scale)

Front



Back

Note: Tolerance on all dimensions ±0.15mm unless otherwise noted

Disclaimer:

No part of this document may be copied or reproduced in any form or by any means, or transferred to any third party, without the prior written consent of an authorized representative of ATP Electronics ("ATP"). The information in this document is subject to change without notice. ATP assumes no responsibility for any errors or omissions that may appear in this document, and disclaims responsibility for any consequences resulting from the use of the information set forth herein. ATP makes no commitments to update or to keep current information contained in this document. The information set forth in this document is considered to be "Proprietary" and "Confidential" property owned by ATP.