MP6920

Fast Turn-Off Intelligent Rectifier

The Future of Analog IC Technology

DESCRIPTION

The MP6920 is a fast turn-off intelligent rectifier for Flyback converters that combines a 60V power switch that replaces diode rectifiers for high efficiency. The chip regulates the forward voltage drop of the internal power switch to about 70mV and turns it off before the voltage goes negative.

FEATURES

- Supports DCM and Quasi-Resonant Flyback converters
- Integrated 10mΩ 60V Power Switch
- Compatible with Energy Star, 1W Standby Requirements
- V_{DD} Range From 8V to 24V
- 70mV V_{DS} Regulation Function (1)
- Max 300kHz Switching Frequency
- Light Load Mode Function (1) with <300uA Quiescent Current
- Supports High-Side and Low-Side Rectification
- Power Savings of Up to 1.5W in a Typical Notebook Adapter

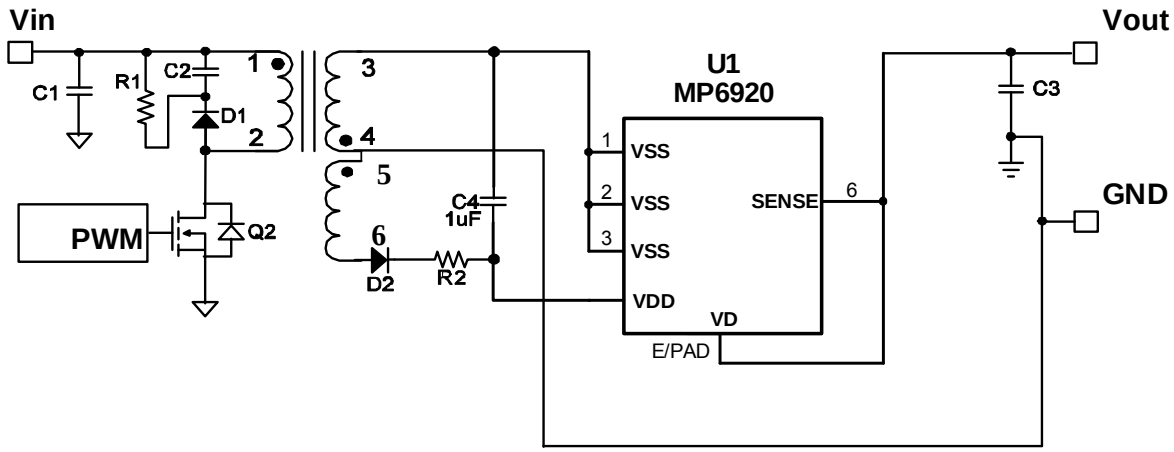
APPLICATIONS

- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems
- Flyback Converters

Notes:

1) Related issued patent: US Patent US8,067,973; US8,400,790. CN Patent ZL201010504140.4; ZL200910059751.X. Other patents pending.

TYPICAL APPLICATION

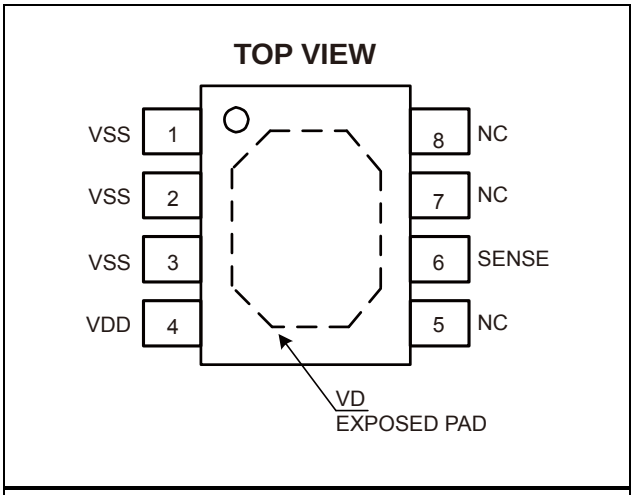


ORDERING INFORMATION

Part Number	Package	Top Marking
MP6920DN*	SOIC8E	MP6920

* For Tape & Reel, add suffix –Z (e.g. MP6920DN–Z);
For RoHS Compliant Packaging, add suffix –LF; (e.g. MP6920DN–LF–Z)

PACKAGE REFERENCE



SOIC8E

ABSOLUTE MAXIMUM RATINGS (2)

V_{DD} to V_{SS} .....-0.3V to +26V
V_D to V_{SS} .....-0.7V to +60V
Maximum Operating Frequency..... 300kHz
Continuous Power Dissipation (T_A = 25°C) (3)
SOIC8E.....2.5W
Junction Temperature.....150°C
Lead Temperature (Solder).....260°C
Storage Temperature ..... -55°C to +150°C

Recommended Operation Conditions (4)

V_{DD} to V_{SS} .....8V to 24V
Operating Junction Temp. (T_J).... -40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
SOIC8E	50	10	°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB. Without heatsink.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12V, T_A= 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$		60			V
V_{DD} Voltage Range			8		24	V
V_{DD} UVLO Rising			5.0	6.0	7.0	V
V_{DD} UVLO Hysteresis			0.8	1.2	1.5	V
Operating Current	I_{CC}	f_{SW}=100kHz		4.5	8	mA
Light-Load Current				260	360	µA
CONTROL CIRCUITRY						
V_{SS} –V_D Forward Voltage	V_{fwd}		55	70	85	mV
Turn-On Delay [6]	t_{Don}			200		ns
Turn Off Threshold (V_{SS}-V_D) [6]			20	30	40	mV
Turn-Off Delay [6]	t_{Doff}	V_D =V_{SS}		30	45	ns
Minimum On-Time [6]	t_{MIN}			1.6		µs
Light-Load-Enter Delay	$t_{LL\text{-}Delay}$			120		µs
Light-Load-Enter Pulse Width	t_{LL}			2.2		µs
Light-Load-Enter Pulse Width Hysteresis	$t_{LL\text{-}H}$			0.2		µs
Light-Load Mode Exit Pulse Width Threshold (V_{DS})	$V_{LL\text{-}DS}$			-250		mV
POWER SWITCH CHARACTERISTICS						
Single Pulse Avalanche Current [7]	I_{AS}			41		A
Single Pulse Avalanche Energy [7]	E_{AS}			250		mJ
Drain-Source On-State Resistance	$R_{DS(ON)}$			9.5	11.4	mΩ
Input Capacitance	C_{iss}	V_{DS}=25V, f=1MHz		3696		pF
Output Capacitance	C_{oss}			258		pF
Reverse Transfer Capacitance	C_{rss}			104		pF
DRAIN-SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{rr}	I_F=10A, dI_F/dt=300A/us		29		ns
Diode Reverse Charge	Q_{rr}			80		nC

Notes:

6) Guaranteed by Design and Characterization.

7) Starting T_J=25°C, L=0.3mH

PIN FUNCTIONS

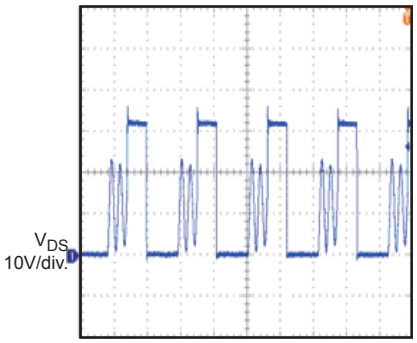
Pin # (SOIC8E)	Name	Description
1,2,3	VSS	MOSFET Source, also used as reference for VDD
6	SENSE	Drain sense, connect this pin with exposed pad on the layout
4	VDD	Supply Voltage
5,7,8	NC	No connection
EXPOSED PAD	VD	MOSFET Drain

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD}=12V, unless otherwise noticed.

Operation In 36W Flyback Application

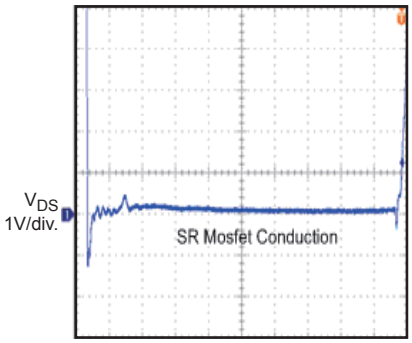
V_{IN} = 110V_{AC}, V_{OUT} =12V, I_{OUT} = 1A



10µs/div.

Operation In 36W Flyback Application

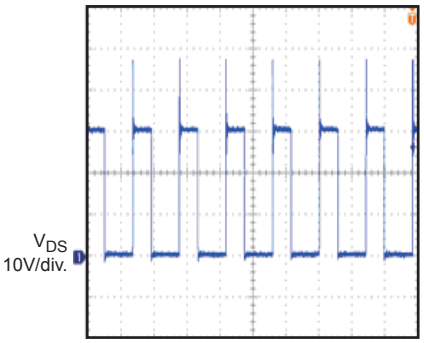
V_{IN} = 110V_{AC}, V_{OUT} =12V, I_{OUT} = 1A



1µs/div.

Operation In 36W Flyback Application

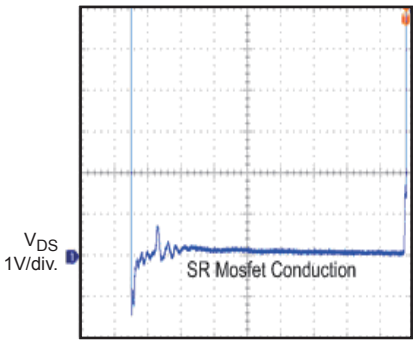
V_{IN}=110V_{AC}, V_{OUT}=12V, I_{OUT}=3A



10µs/div.

Operation In 36W Flyback Application

V_{IN}=110V_{AC}, V_{OUT}=12V, I_{OUT}=3A



1µs/div.

BLOCK DIAGRAM

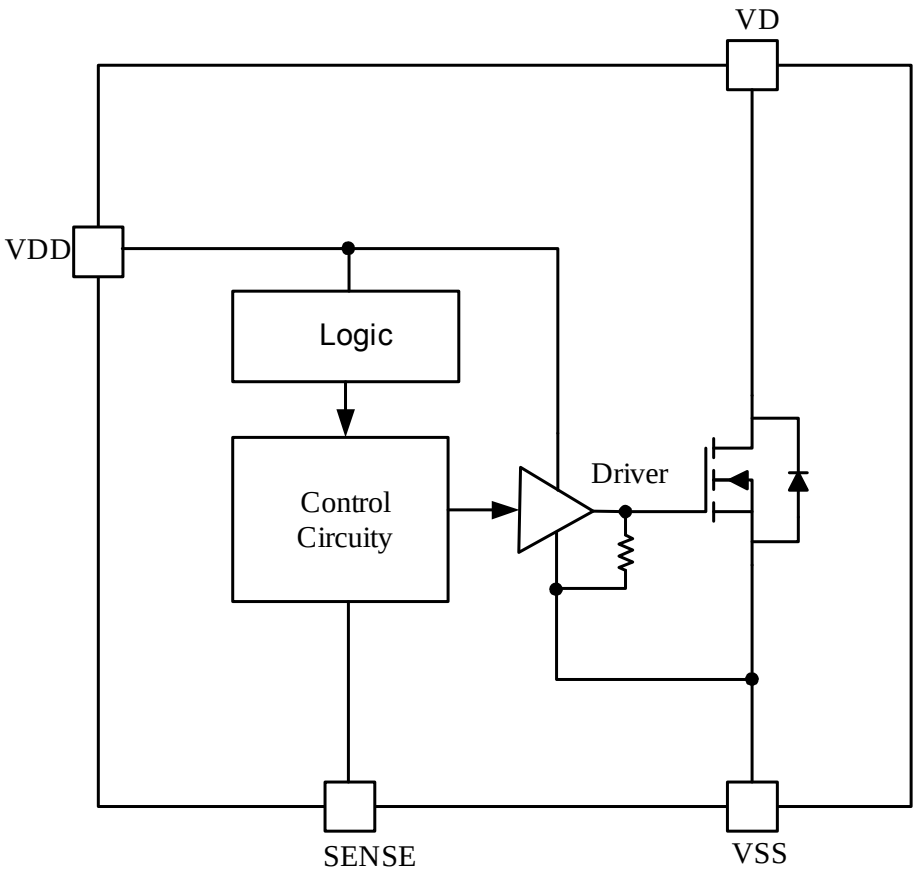


Figure 1: Functional Block Diagram

OPERATION

The MP6920 supports operation in discontinuous conduction mode (DCM) and Quasi-Resonant Flyback converters. The internal control circuitry of the MP6920 controls the integrated MOSFET gate in forward mode and will turn the gate off when the MOSFET current is fairly low.

Blanking

The control circuitry contains a blanking function. When it pulls the integrated MOSFET on/off, it makes sure that the on/off state at least lasts for some time. The turn-on blanking time is 1.6μs, which determines the minimum on-time. During the turn-on blanking period, the turn-off threshold is not totally blanked, but changes to +50mV (instead of -30mV). This ensures that the part can always turn off even during the turn-on blanking period (albeit slower).

Under-Voltage Lockout

When V_{DD} is below the under-voltage lockout (UVLO) threshold, the part enters sleep mode and the integrated MOSFET will not turn on.

Basic Operation

The basic operations of flyback converter with the MP6920 are:

- **Turn-On Phase**
  When the switch current flows through the body diode of the integrated MOSFET, it generates a negative V_{DS} (V_D-V_{SS}) across it (<-500mV); the V_{DS} is much lower than the turn-on threshold of the control circuitry (-70mV), which then turns on the integrated MOSFET after a 200ns turn-on delay (defined in Figure 2).
- **Conducting Phase**
  When the integrated MOSFET turns on, V_{DS} ($-I_{SD}$ x $R_{DS(ON)}$) rises according to the switch current (I_{SD}) drop: As soon as V_{DS} rises above the turn-on threshold (-70mV), the control circuitry stops pulling up the internal gate driver and the driver voltage of the integrated MOSFET drops, which makes the MOSFET ON-resistance $R_{DS(ON)}$ larger. By doing that, V_{DS} ($-I_{SD}$ x $R_{DS(ON)}$) stabilizes to around -70mV even when the switch current I_{SD} is fairly small. This function can avoid triggering the turn-off threshold (-30mV) of the internal driver until the current through the integrated MOSFET has dropped to near zero.

  Figure 3 shows the MP6920 operating in heavy-load condition. Due to the high current, the internal driver voltage initially saturates; after V_{DS} goes to above -70mV, driver voltage decreases to adjust the V_{DS} to around -70mV.

  Figure 4 shows the MP6920 operating at light-load condition. Due to the low current, the driver voltage never saturates but begins to decrease as soon as the integrated MOSFET turns on and adjusts the V_{DS}.
- **Turn-Off Phase**
  When V_{DS} rises to trigger the turn-off threshold (-30mV), the driver voltage of the switch goes zero after a 20ns turn-off delay (shown in Figure 2) by the control circuitry. Similar to turn-on phase, a 200ns blanking time after the switch turns off avoid erroneous trigging.

Light-Load Latch-Off Function

The gate driver of integrated MOSFET in the MP6920 is latched to save the driver loss at light-load condition to improve light-load efficiency. The light-load-enter pulse width (t_{LL}) is internally fixed at 2.2μs. During each switching cycle, if the integrated MOSFET conducting period remains below 2.2μs, the MP6920 falls into light-load mode and latches off the integrated MOSFET after a 120μs delay (light-load-enter delay, $t_{LL\text{-}Delay}$)

After entering light-load mode, the MP6920 monitors the integrated MOSFET's body diode conducting period by sensing V_{DS}—when V_{DS} exceeds -250mV ($V_{LL\text{-}DS}$), the MP6920 treats the integrated MOSFET as a body diode until the conducting period finishes. If the MOSFET's body diode conducting period is longer than 2.4μs (t_{LL}+$t_{LL\text{-}H}$), the light-load mode finishes and the integrated MOSFET of MP6920 is unlatched to restart the internal synchronous rectification (see Figure 6 for details).

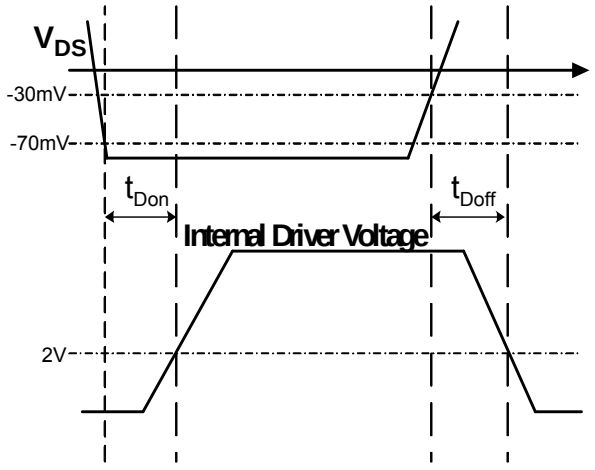


Figure 2: Turn-On and Turn-Off Delay

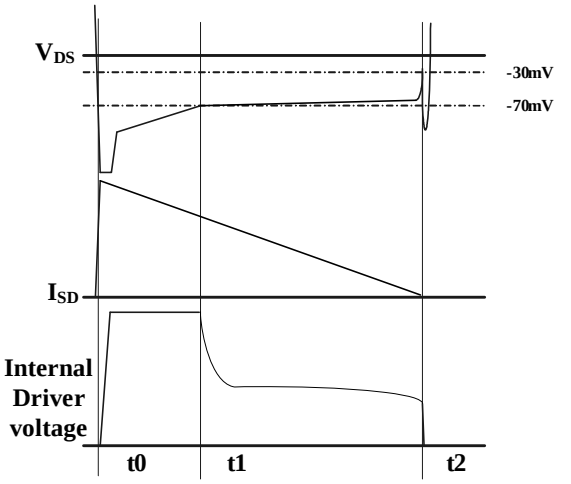


Figure 3: Synchronous Rectification Operation at heavy load

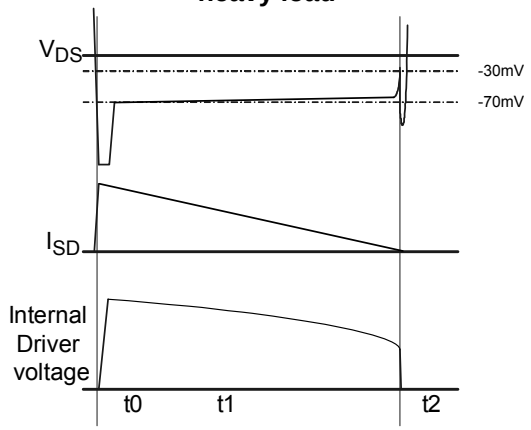


Figure 4: Synchronous Rectification Operation at light load

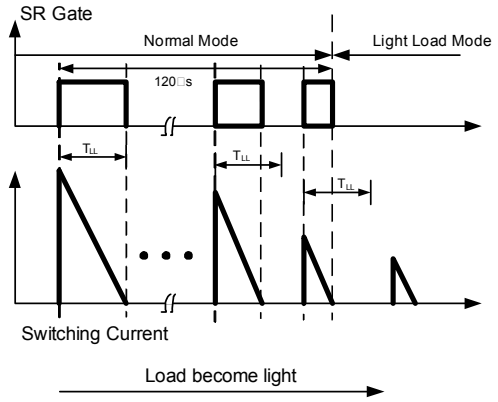


Figure 5: Enter Light Load Mode

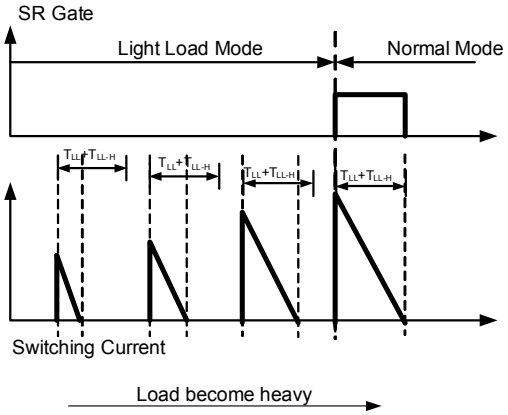


Figure 6: Exit Light Load Mode

TYPICAL APPLICATION CIRCUIT

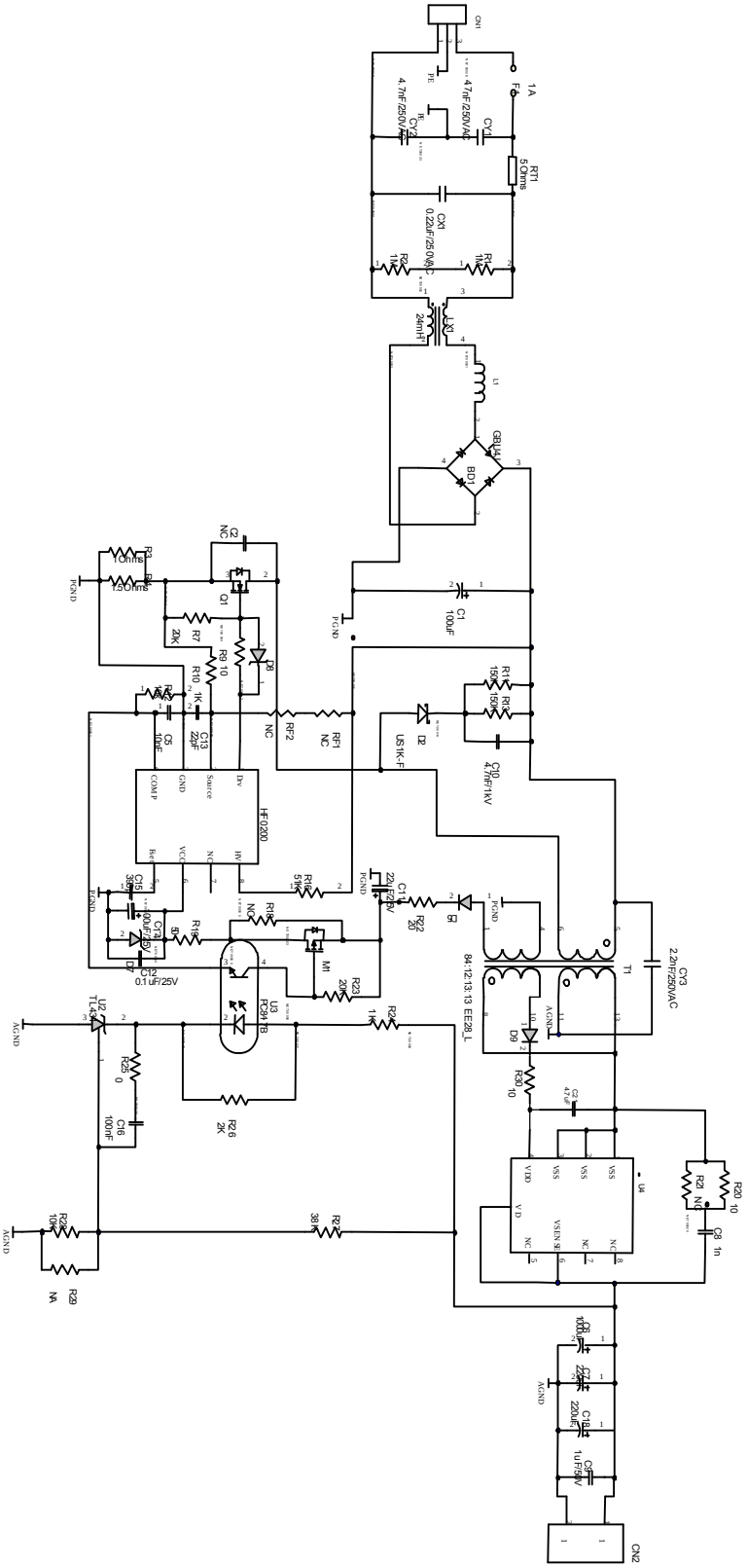
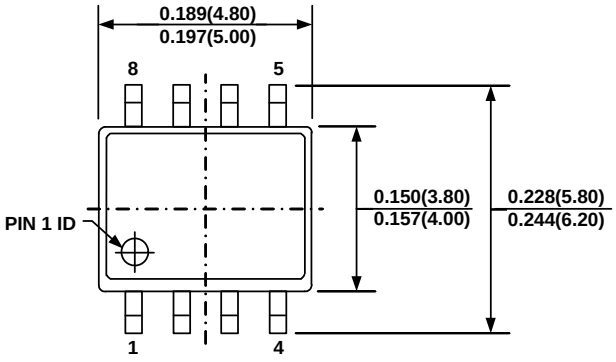


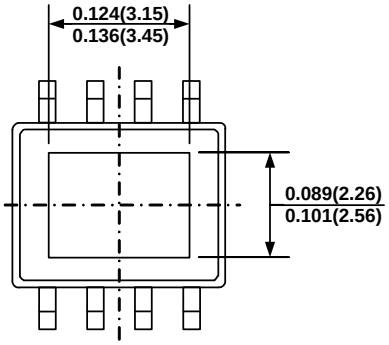
Figure 7: MP6920 for Synchronous Conduction in 36W Flyback Application

PACKAGE INFORMATION

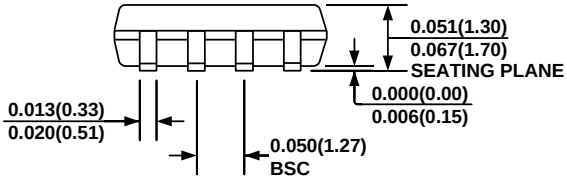
SOIC8E (Exposed Pad)



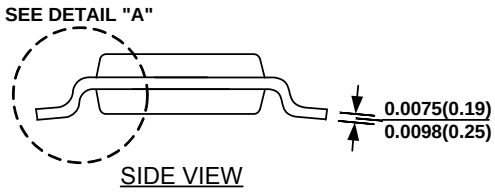
TOP VIEW



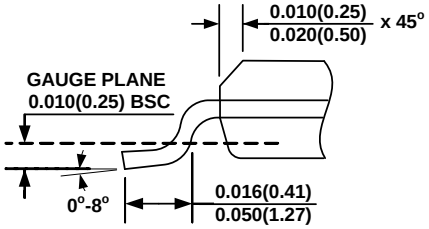
BOTTOM VIEW



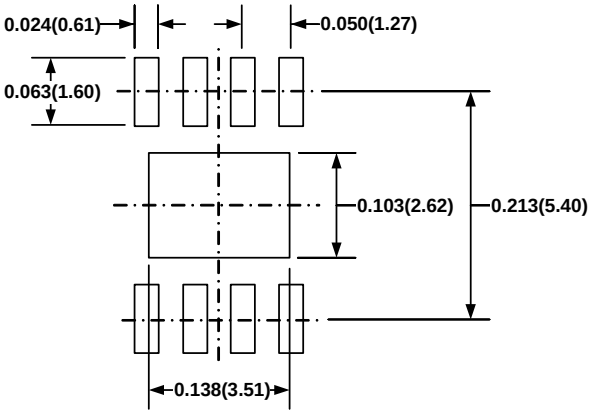
FRONT VIEW



SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.