

## DESCRIPTION

The MP6920 is a fast turn-off intelligent rectifier for Flyback converters that combines a 60V power switch that replaces diode rectifiers for high efficiency. The chip regulates the forward voltage drop of the internal power switch to about 70mV and turns it off before the voltage goes negative.

## FEATURES

- Supports DCM and Quasi-Resonant Flyback converters
- Integrated 10mΩ 60V Power Switch
- Compatible with Energy Star, 1W Standby Requirements
- $V_{DD}$  Range From 8V to 24V
- 70mV  $V_{DS}$  Regulation Function <sup>(1)</sup>
- Max 300kHz Switching Frequency
- Light Load Mode Function <sup>(1)</sup> with <300uA Quiescent Current
- Supports High-Side and Low-Side Rectification
- Power Savings of Up to 1.5W in a Typical Notebook Adapter

## APPLICATIONS

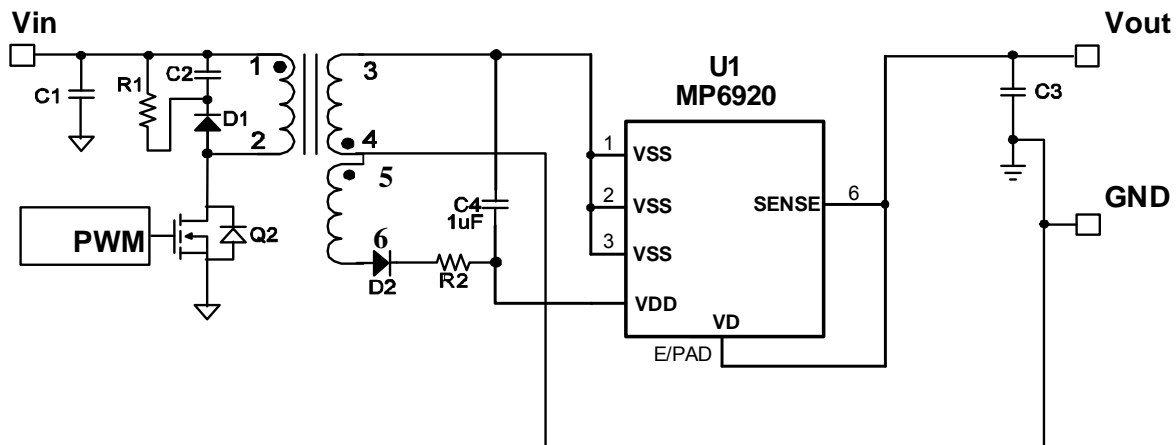
- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems
- Flyback Converters

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**Notes:**

- 1) Related issued patent: US Patent US8,067,973; US8,400,790. CN Patent ZL201010504140.4; ZL200910059751.X. Other patents pending.

## TYPICAL APPLICATION

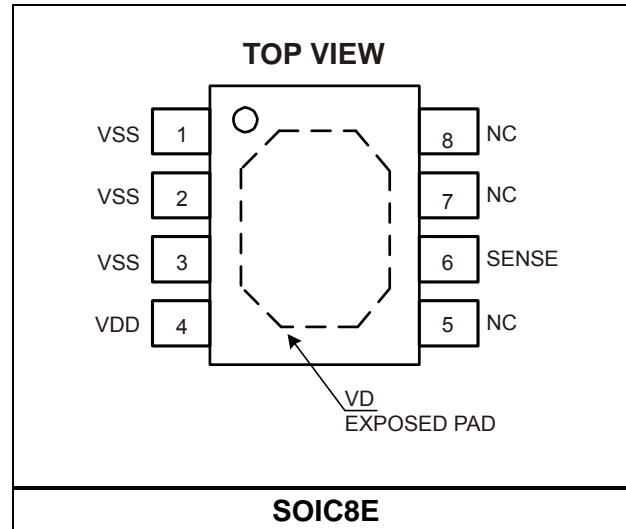


## ORDERING INFORMATION

Part Number	Package	Top Marking
MP6920DN*	SOIC8E	MP6920

\* For Tape & Reel, add suffix -Z (e.g. MP6920DN-Z);  
For RoHS Compliant Packaging, add suffix -LF; (e.g. MP6920DN-LF-Z)

## PACKAGE REFERENCE



### ABSOLUTE MAXIMUM RATINGS <sup>(2)</sup>

$V_{DD}$ to $V_{SS}$ .....	-0.3V to +26V
$V_D$ to $V_{SS}$ .....	-0.7V to +60V
Maximum Operating Frequency.....	300kHz
Continuous Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(3)</sup>	
SOIC8E.....	2.5W
Junction Temperature .....	150°C
Lead Temperature (Solder).....	260°C
Storage Temperature .....	-55°C to +150°C

### Recommended Operation Conditions <sup>(4)</sup>

$V_{DD}$ to $V_{SS}$ .....	8V to 24V
Operating Junction Temp. ( $T_J$ )....	-40°C to +125°C

### Thermal Resistance <sup>(5)</sup>

	$\theta_{JA}$	$\theta_{JC}$
SOIC8E .....	50	10 ... °C/W

#### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB. Without heatsink.

## ELECTRICAL CHARACTERISTICS

$V_{DD} = 12V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>		60			V
V <sub>DD</sub> Voltage Range			8		24	V
V <sub>DD</sub> UVLO Rising			5.0	6.0	7.0	V
V <sub>DD</sub> UVLO Hysteresis			0.8	1.2	1.5	V
Operating Current	I <sub>CC</sub>	f <sub>SW</sub> =100kHz		4.5	8	mA
Light-Load Current				260	360	μA
CONTROL CIRCUITRY						
V <sub>SS</sub> -V <sub>D</sub> Forward Voltage	V <sub>fwd</sub>		55	70	85	mV
Turn-On Delay <sup>(6)</sup>	t <sub>Don</sub>			200		ns
Turn Off Threshold (V <sub>SS</sub> -V <sub>D</sub> ) <sup>(6)</sup>			20	30	40	mV
Turn-Off Delay <sup>(6)</sup>	t <sub>DoFF</sub>	V <sub>D</sub> =V <sub>SS</sub>		30	45	ns
Minimum On-Time <sup>(6)</sup>	t <sub>MIN</sub>			1.6		μs
Light-Load-Enter Delay	t <sub>LL-Delay</sub>			120		μs
Light-Load-Enter Pulse Width	t <sub>LL</sub>			2.2		μs
Light-Load-Enter Pulse Width Hysteresis	t <sub>LL-H</sub>			0.2		μs
Light-Load Mode Exit Pulse Width Threshold (V <sub>DS</sub> )	V <sub>LL-DS</sub>			-250		mV
POWER SWITCH CHARACTERISTICS						
Single Pulse Avalanche Current <sup>(7)</sup>	I <sub>AS</sub>			41		A
Single Pulse Avalanche Energy <sup>(7)</sup>	E <sub>AS</sub>			250		mJ
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>			9.5	11.4	mΩ
Input Capacitance	C <sub>iSS</sub>	V <sub>DS</sub> =25V, f=1MHz		3696		pF
Output Capacitance	C <sub>oSS</sub>			258		pF
Reverse Transfer Capacitance	C <sub>rSS</sub>			104		pF
DRAIN-SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> =10A, dI <sub>F</sub> /dt=300A/us		29		ns
Diode Reverse Charge	Q <sub>rr</sub>			80		nC

### Notes:

6) Guaranteed by Design and Characterization.

7) Starting  $T_J=25^\circ C$ ,  $L=0.3mH$

## PIN FUNCTIONS

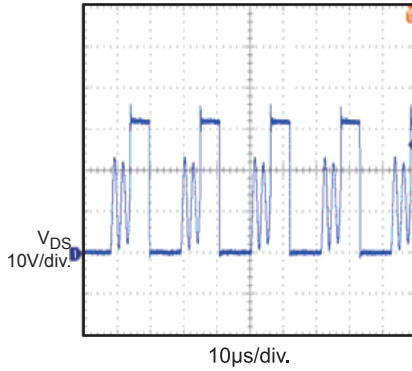
Pin # (SOIC8E)	Name	Description
1,2,3	VSS	MOSFET Source, also used as reference for VDD
6	SENSE	Drain sense, connect this pin with exposed pad on the layout
4	VDD	Supply Voltage
5,7,8	NC	No connection
EXPOSED PAD	VD	MOSFET Drain

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD}=12V$ , unless otherwise noticed.

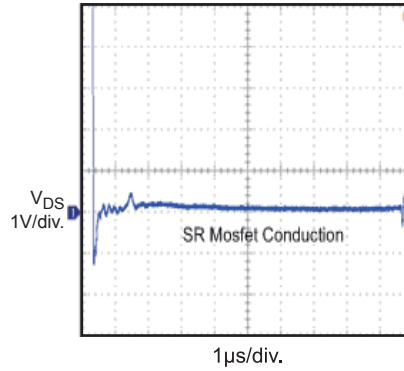
### Operation In 36W Flyback Application

$V_{IN} = 110V_{AC}$ ,  $V_{OUT} = 12V$ ,  $I_{OUT} = 1A$



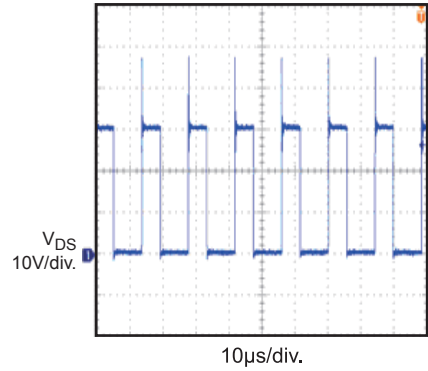
### Operation In 36W Flyback Application

$V_{IN} = 110V_{AC}$ ,  $V_{OUT} = 12V$ ,  $I_{OUT} = 1A$



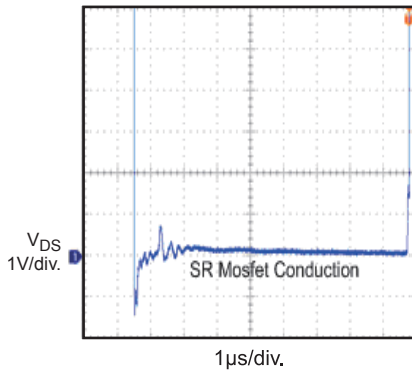
### Operation In 36W Flyback Application

$V_{IN} = 110V_{AC}$ ,  $V_{OUT} = 12V$ ,  $I_{OUT} = 3A$

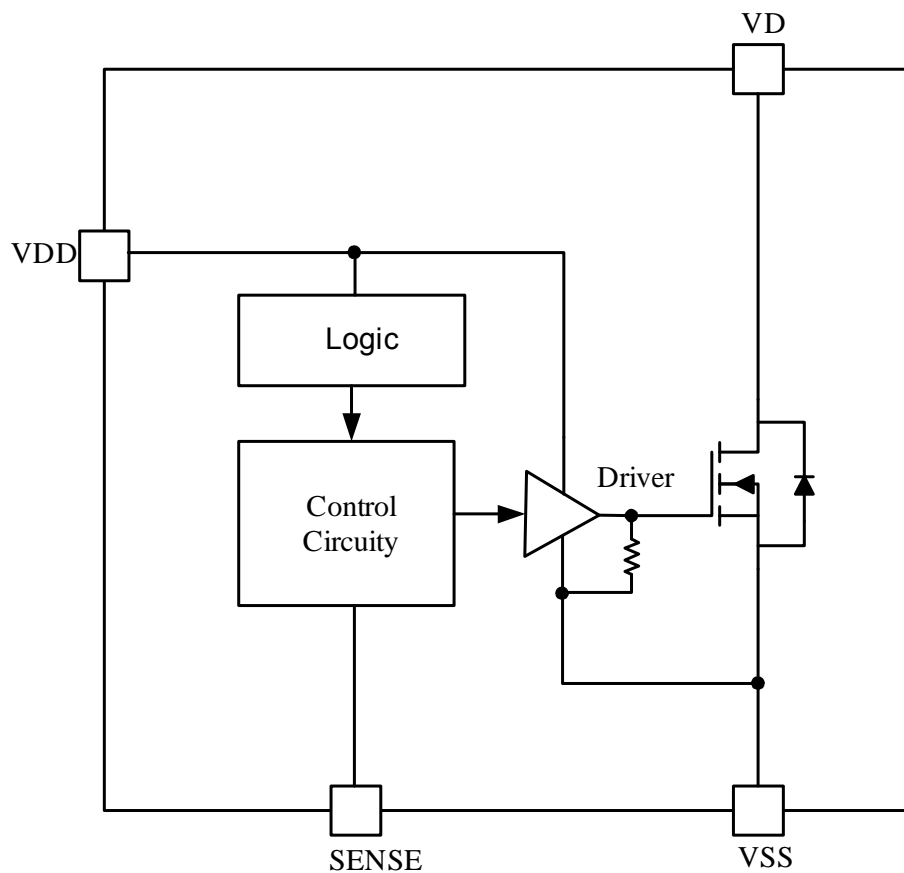


### Operation In 36W Flyback Application

$V_{IN} = 110V_{AC}$ ,  $V_{OUT} = 12V$ ,  $I_{OUT} = 3A$



## BLOCK DIAGRAM



**Figure 1: Functional Block Diagram**

## OPERATION

The MP6920 supports operation in discontinuous conduction mode (DCM) and Quasi-Resonant Flyback converters. The internal control circuitry of the MP6920 controls the integrated MOSFET gate in forward mode and will turn the gate off when the MOSFET current is fairly low.

### Blanking

The control circuitry contains a blanking function. When it pulls the integrated MOSFET on/off, it makes sure that the on/off state at least lasts for some time. The turn-on blanking time is 1.6 $\mu$ s, which determines the minimum on-time. During the turn-on blanking period, the turn-off threshold is not totally blanked, but changes to +50mV (instead of -30mV). This ensures that the part can always turn off even during the turn-on blanking period (albeit slower).

### Under-Voltage Lockout

When  $V_{DD}$  is below the under-voltage lockout (UVLO) threshold, the part enters sleep mode and the integrated MOSFET will not turn on.

### Basic Operation

The basic operations of flyback converter with the MP6920 are:

- **Turn-On Phase**

When the switch current flows through the body diode of the integrated MOSFET, it generates a negative  $V_{DS}$  ( $V_D - V_{SS}$ ) across it (<-500mV); the  $V_{DS}$  is much lower than the turn-on threshold of the control circuitry (-70mV), which then turns on the integrated MOSFET after a 200ns turn-on delay (defined in Figure 2).

- **Conducting Phase**

When the integrated MOSFET turns on,  $V_{DS}$  ( $-I_{SD} \times R_{DS(ON)}$ ) rises according to the switch current ( $I_{SD}$ ) drop: As soon as  $V_{DS}$  rises above the turn-on threshold (-70mV), the control circuitry stops pulling up the internal gate driver and the driver voltage of the integrated MOSFET drops, which makes the MOSFET ON-resistance  $R_{DS(ON)}$  larger. By doing that,  $V_{DS}$  ( $-I_{SD} \times R_{DS(ON)}$ ) stabilizes to around -70mV even when the switch current  $I_{SD}$  is fairly small. This function can avoid

triggering the turn-off threshold (-30mV) of the internal driver until the current through the integrated MOSFET has dropped to near zero.

Figure 3 shows the MP6920 operating in heavy-load condition. Due to the high current, the internal driver voltage initially saturates; after  $V_{DS}$  goes to above -70mV, driver voltage decreases to adjust the  $V_{DS}$  to around -70mV.

Figure 4 shows the MP6920 operating at light-load condition. Due to the low current, the driver voltage never saturates but begins to decrease as soon as the integrated MOSFET turns on and adjusts the  $V_{DS}$ .

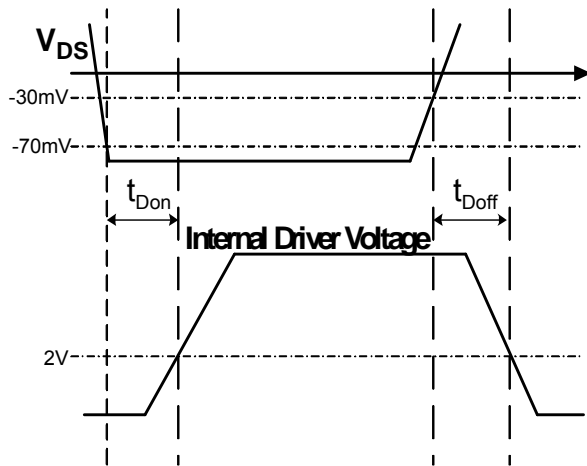
- **Turn-Off Phase**

When  $V_{DS}$  rises to trigger the turn-off threshold (-30mV), the driver voltage of the switch goes zero after a 20ns turn-off delay (shown in Figure 2) by the control circuitry. Similar to turn-on phase, a 200ns blanking time after the switch turns off avoid erroneous triggering.

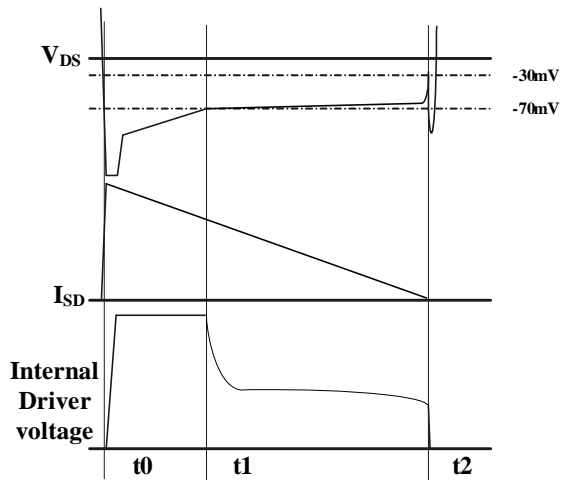
### Light-Load Latch-Off Function

The gate driver of integrated MOSFET in the MP6920 is latched to save the driver loss at light-load condition to improve light-load efficiency. The light-load-enter pulse width ( $t_{LL}$ ) is internally fixed at 2.2 $\mu$ s. During each switching cycle, if the integrated MOSFET conducting period remains below 2.2 $\mu$ s, the MP6920 falls into light-load mode and latches off the integrated MOSFET after a 120 $\mu$ s delay (light-load-enter delay,  $t_{LL-Delay}$ ).

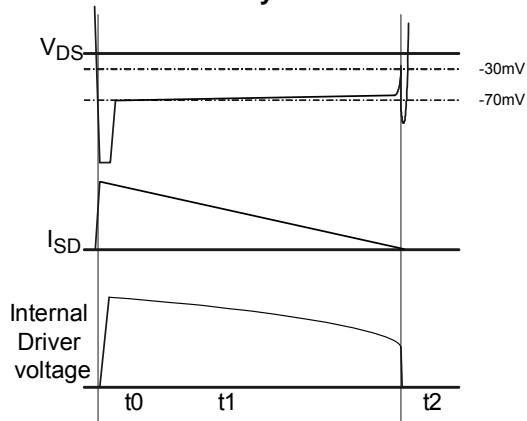
After entering light-load mode, the MP6920 monitors the integrated MOSFET's body diode conducting period by sensing  $V_{DS}$ —when  $V_{DS}$  exceeds -250mV ( $V_{LL-DS}$ ), the MP6920 treats the integrated MOSFET as a body diode until the conducting period finishes. If the MOSFET's body diode conducting period is longer than 2.4 $\mu$ s ( $t_{LL} + t_{LL-H}$ ), the light-load mode finishes and the integrated MOSFET of MP6920 is unlatched to restart the internal synchronous rectification (see Figure 6 for details).



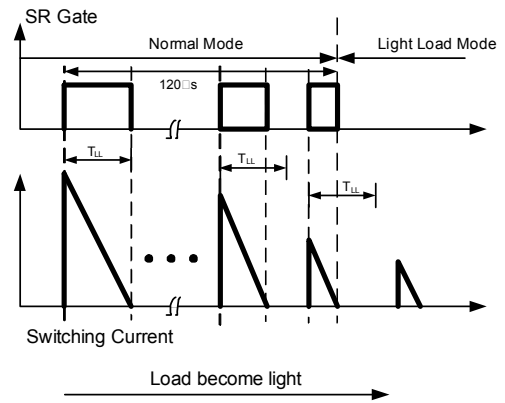
**Figure 2: Turn-On and Turn-Off Delay**



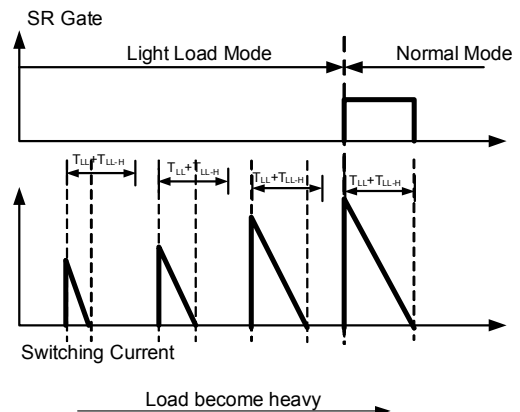
**Figure 3: Synchronous Rectification Operation at heavy load**



**Figure 4: Synchronous Rectification Operation at light load**



**Figure 5: Enter Light Load Mode**



**Figure 6: Exit Light Load Mode**

# TYPICAL APPLICATION CIRCUIT

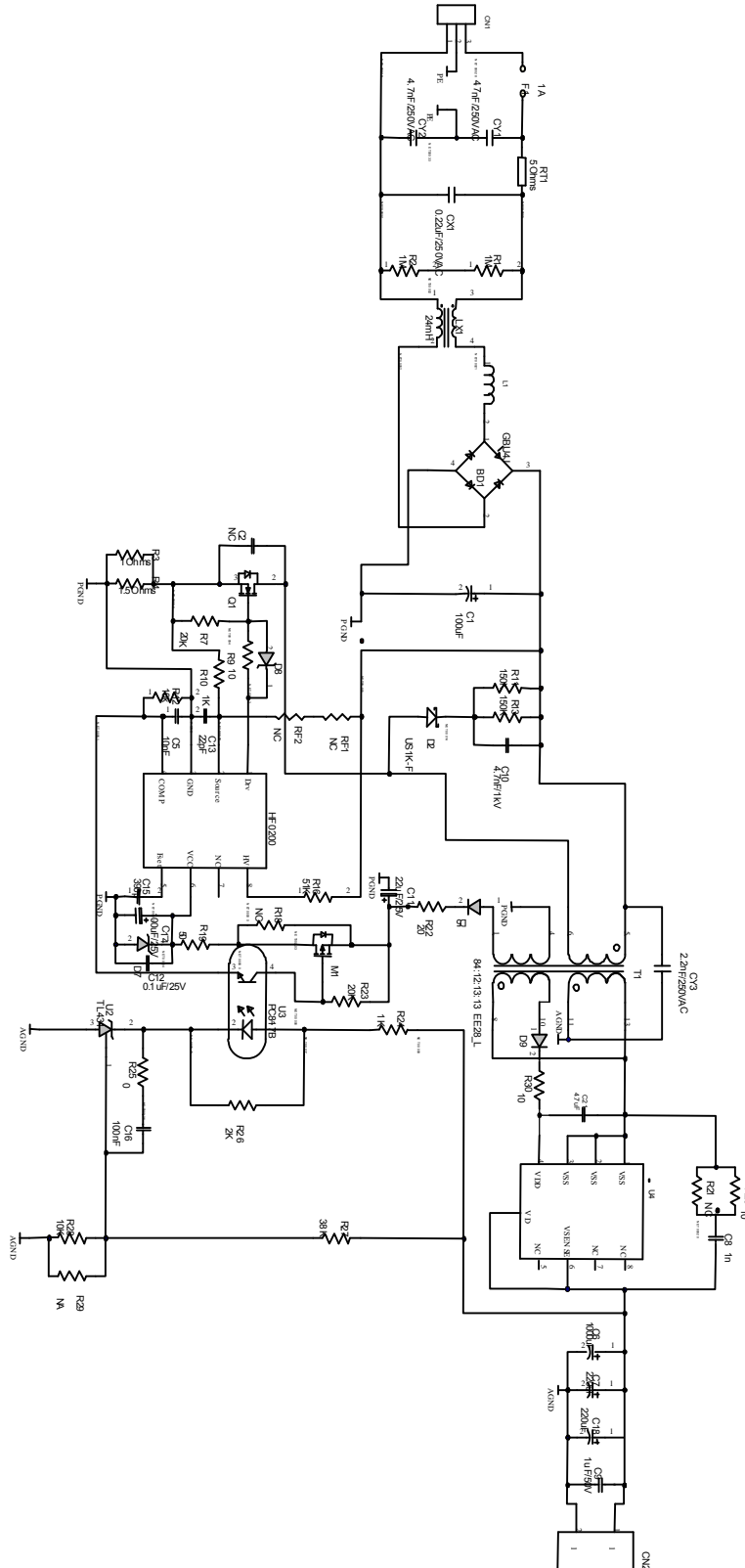
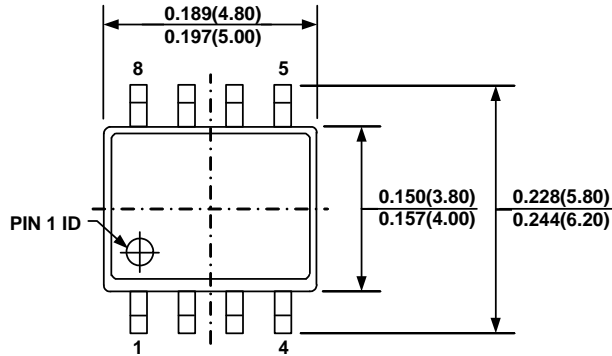


Figure 7: MP6920 for Synchronous Conduction in 36W Flyback Application

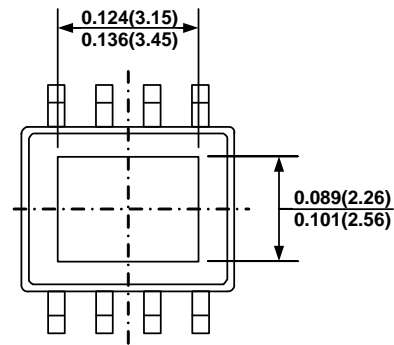


# PACKAGE INFORMATION

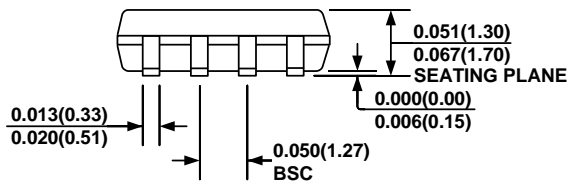
## SOIC8E (Exposed Pad)



TOP VIEW

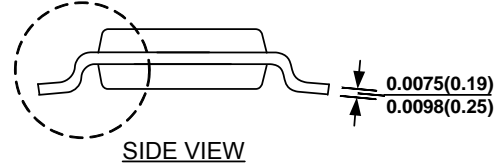


BOTTOM VIEW

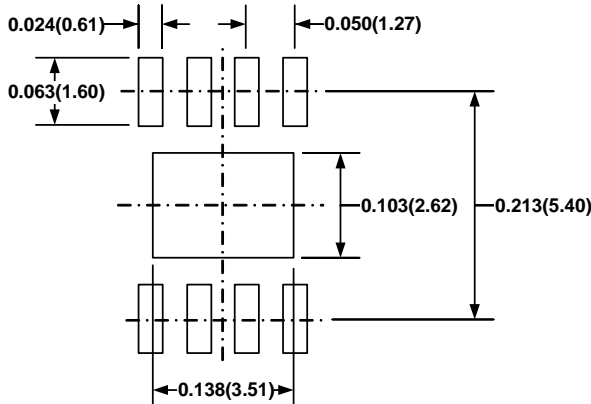


FRONT VIEW

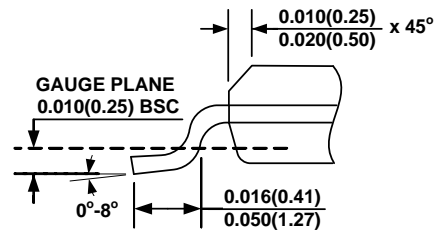
SEE DETAIL "A"



SIDE VIEW



RECOMMENDED LAND PATTERN



DETAIL "A"

### NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

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