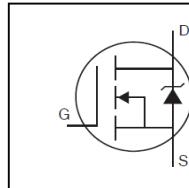
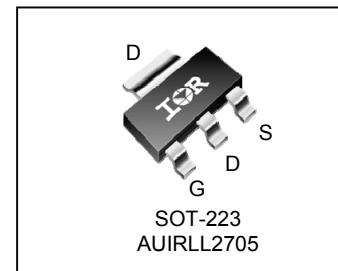


Features

- Advanced Planar Technology
- Low On-Resistance
- Logic Level Gate Drive
- Dynamic dv/dt Rating
- 150°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



| HEXFET® Power MOSFET | |
|--------------------------------|--------------|
| V_{DSS} | 55V |
| R_{DS(on)} max. | 0.04Ω |
| I_D | 3.8A |



| G | D | S |
|----------|----------|----------|
| Gate | Drain | Source |

Description

Specifically designed for Automotive applications, this cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.

| Base part number | Package Type | Standard Pack | | Orderable Part Number |
|-------------------------|---------------------|----------------------|-----------------|------------------------------|
| | | Form | Quantity | |
| AUIRLL2705 | SOT-223 | Tape and Reel | 2500 | AUIRLL2705TR |

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

| Symbol | Parameter | Max. | Units |
|----------------------------------------|-----------------------------------------------------|--------------|--------------|
| I _D @ T _A = 25°C | Continuous Drain Current, V _{GS} @ 10V ⑥ | 5.2 | A |
| I _D @ T _A = 25°C | Continuous Drain Current, V _{GS} @ 10V ⑤ | 3.8 | |
| I _D @ T _A = 70°C | Continuous Drain Current, V _{GS} @ 10V ⑤ | 3.0 | |
| I _{DM} | Pulsed Drain Current ① | 30 | |
| P _D @ T _A = 25°C | Maximum Power Dissipation (PCB Mount) ⑥ | 2.1 | W |
| P _D @ T _A = 25°C | Maximum Power Dissipation (PCB Mount) ⑤ | 1.0 | |
| | Linear Derating Factor (PCB Mount) ⑤ | 8.3 | mW/°C |
| V _{GS} | Gate-to-Source Voltage | ± 16 | V |
| E _{AS} | Single Pulse Avalanche Energy (Thermally Limited) ② | 110 | mJ |
| I _{AR} | Avalanche Current ① | 3.8 | A |
| E _{AR} | Repetitive Avalanche Energy ①⑤ | 0.10 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 7.5 | V/ns |
| T _J | Operating Junction and | -55 to + 150 | °C |
| T _{STG} | Storage Temperature Range | | |

Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|------------------|-------------------------------------------------|-------------|-------------|--------------|
| R _{θJA} | Junction-to-Ambient (PCB Mount, steady state) ⑤ | 93 | 120 | °C/W |
| R _{θJA} | Junction-to-Ambient (PCB Mount, steady state) ⑥ | 48 | 60 | |

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*Qualification standards can be found at www.infineon.com

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

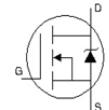
| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|-----------------------------------------------|--------------------------------------|------|-------|-------|---------------------|------------------------------------------------------|
| $V_{(\text{BR})\text{DSS}}$ | Drain-to-Source Breakdown Voltage | 55 | — | — | V | $V_{GS} = 0V, I_D = 250\mu\text{A}$ |
| $\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.061 | — | V/ $^\circ\text{C}$ | Reference to 25°C , $I_D = 1\text{mA}$ |
| $R_{DS(\text{on})}$ | Static Drain-to-Source On-Resistance | — | — | 0.040 | Ω | $V_{GS} = 10V, I_D = 3.8\text{A}$ ④ |
| | | — | — | 0.051 | | $V_{GS} = 5.0V, I_D = 3.8\text{A}$ ④ |
| | | — | — | 0.065 | | $V_{GS} = 4.0V, I_D = 1.9\text{A}$ ④ |
| $V_{GS(\text{th})}$ | Gate Threshold Voltage | 1.0 | — | 2.0 | V | $V_{DS} = V_{GS}, I_D = 250\mu\text{A}$ |
| g_{fs} | Forward Trans conductance | 5.1 | — | — | S | $V_{DS} = 25V, I_D = 1.9\text{A}$ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 25 | μA | $V_{DS} = 55V, V_{GS} = 0V$ |
| | | — | — | 250 | | $V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 16V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -16V$ |

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | | | | | | |
|--------------|------------------------------|---|-----|-----|----|------------------------------------|
| Q_g | Total Gate Charge | — | 32 | 48 | nC | $I_D = 3.8\text{A}$ |
| Q_{gs} | Gate-to-Source Charge | — | 3.5 | 5.3 | | $V_{DS} = 44V$ |
| Q_{gd} | Gate-to-Drain Charge | — | 9.7 | 14 | | $V_{GS} = 10V$, See Fig 6 and 9 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 6.2 | — | ns | $V_{DD} = 28V$ |
| t_r | Rise Time | — | 12 | — | | $I_D = 3.8\text{A}$ |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 35 | — | | $R_G = 6.2\Omega$ |
| t_f | Fall Time | — | 22 | — | | $R_D = 7.1\Omega$, See Fig. 10 ④ |
| C_{iss} | Input Capacitance | — | 870 | — | pF | $V_{GS} = 0V$ |
| C_{oss} | Output Capacitance | — | 220 | — | | $V_{DS} = 25V$ |
| C_{rss} | Reverse Transfer Capacitance | — | 92 | — | | $f = 1.0\text{MHz}$, See Fig. 5 |

Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|----------------------------------------|----------------------------------------------------------------------|------|------|-------|----------------------------------------------------------------|
| I_s | Continuous Source Current (Body Diode) | — | — | 0.91 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| I_{sM} | Pulsed Source Current (Body Diode) ① | — | — | 30 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.3 | V | $T_J = 25^\circ\text{C}, I_s = 3.8\text{A}, V_{GS} = 0V$ ④ |
| t_{rr} | Reverse Recovery Time | — | 58 | 88 | | $T_J = 25^\circ\text{C}, I_F = 3.8\text{A}$ |
| Q_{rr} | Reverse Recovery Charge | — | 140 | 210 | nC | $di/dt = 100\text{A}/\mu\text{s}$ ④ |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |


Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = 25V$, Starting $T_J = 25^\circ\text{C}$, $L = 15\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 3.8\text{A}$. (See fig. 12)
- ③ $I_{SD} \leq 3.8\text{A}$, $di/dt \leq 220\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 150^\circ\text{C}$.
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ When mounted on FR-4 board using minimum recommended footprint.
- ⑥ When mounted on 1 inch square copper board, for comparison with other SMD devices.

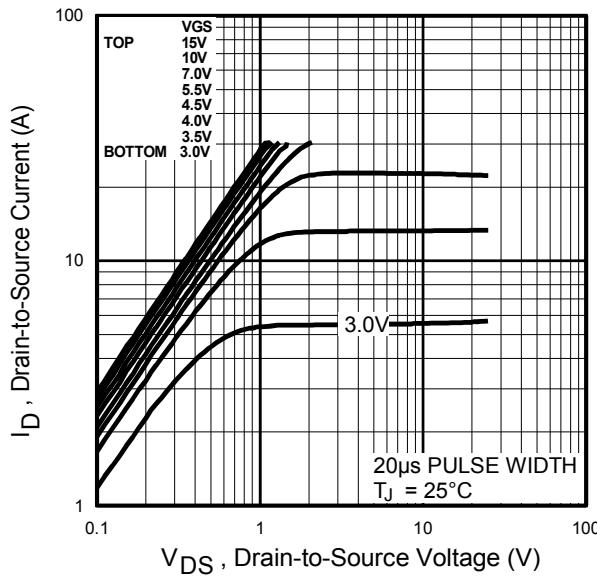


Fig. 1 Typical Output Characteristics

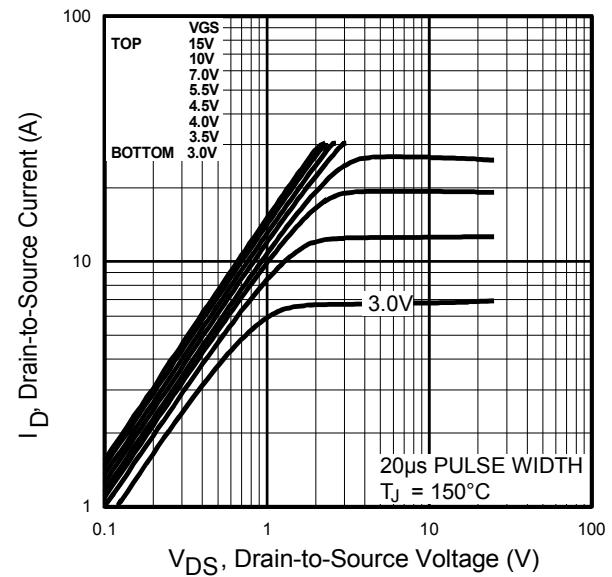


Fig. 2 Typical Output Characteristics

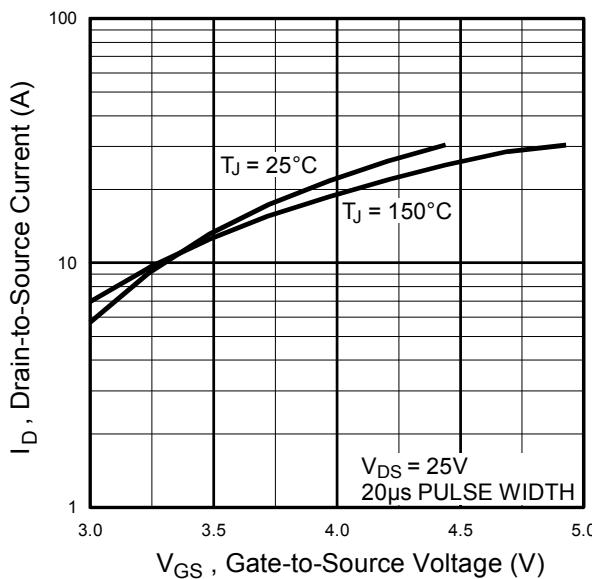


Fig. 3 Typical Transfer Characteristics

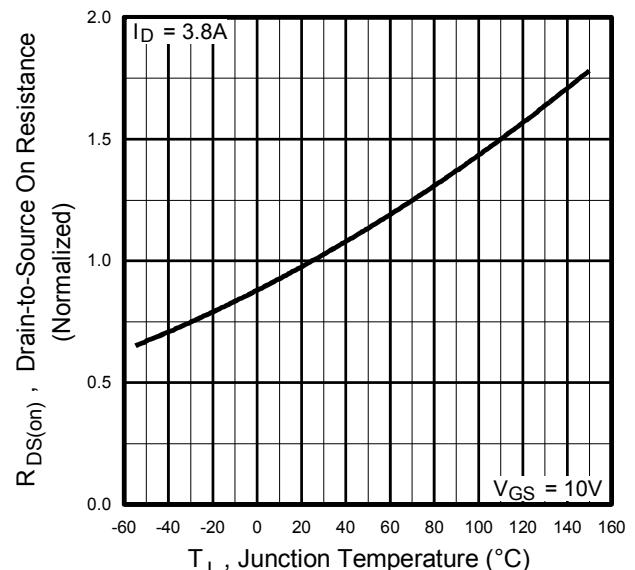


Fig. 4 Normalized On-Resistance vs. Temperature

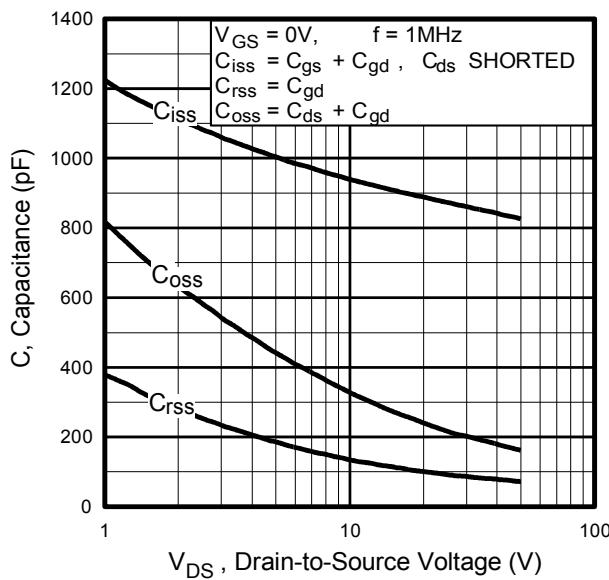


Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage

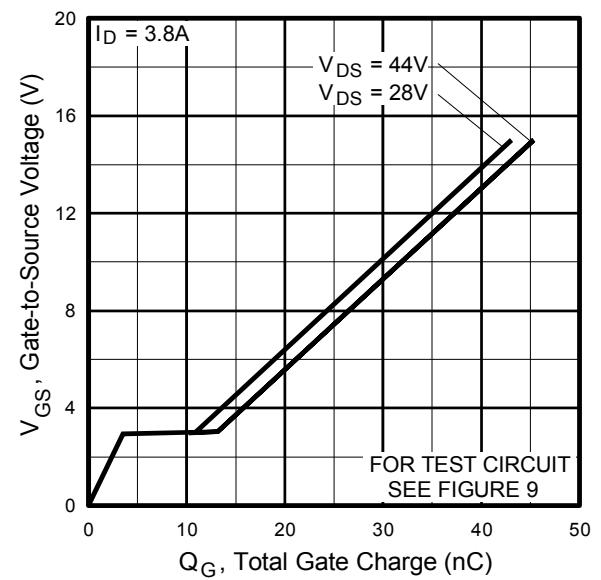


Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage

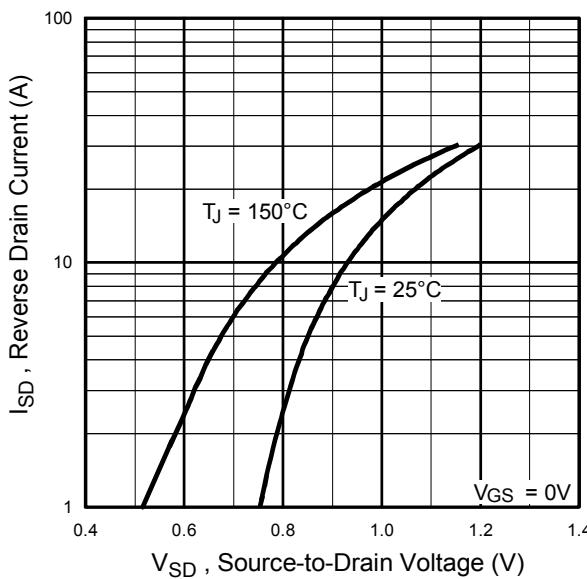


Fig. 7 Typical Source-to-Drain Diode
Forward Voltage

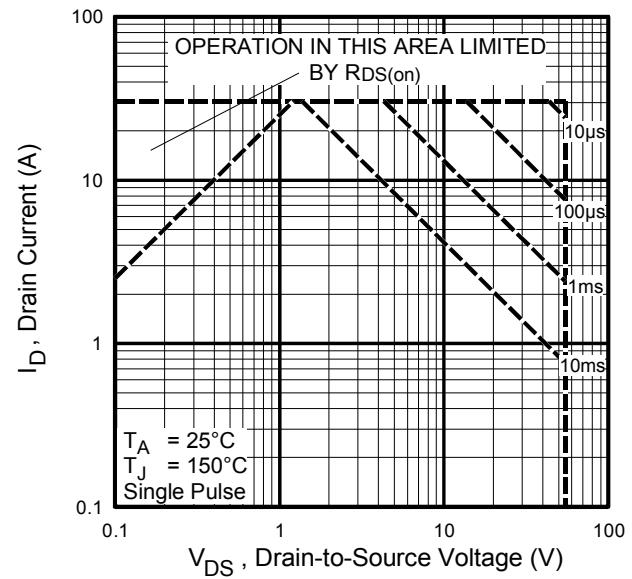


Fig 8. Maximum Safe Operating Area

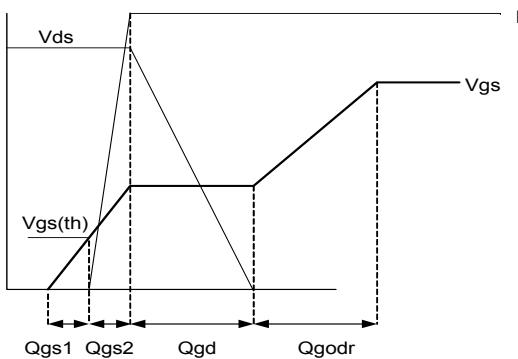


Fig 9a. Basic Gate Charge Waveform

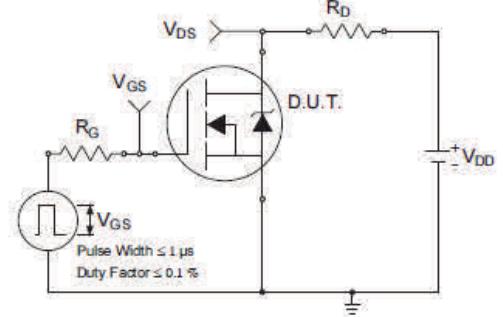


Fig 10a. Switching Time Test Circuit

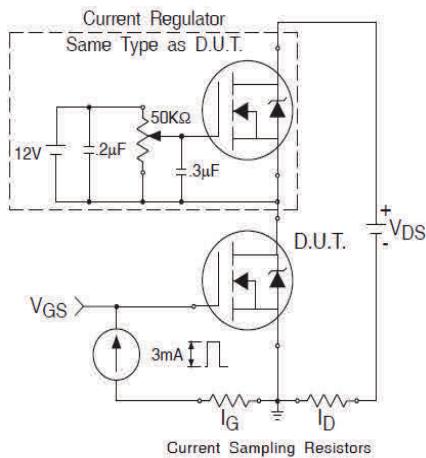


Fig 9b. Gate Charge Test Circuit

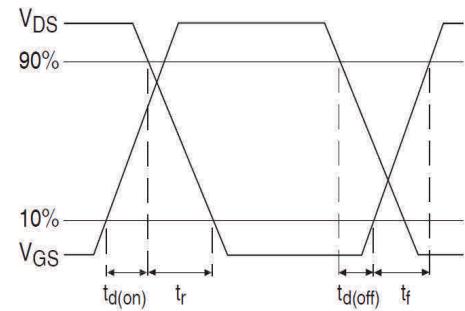


Fig 10b. Switching Time Waveforms

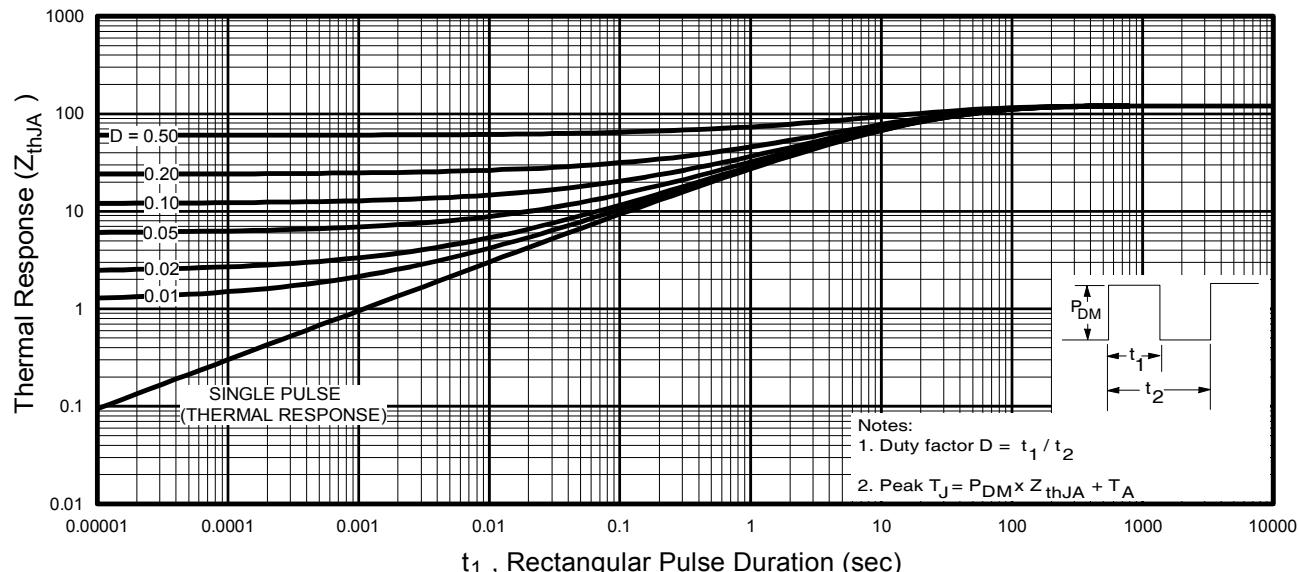


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

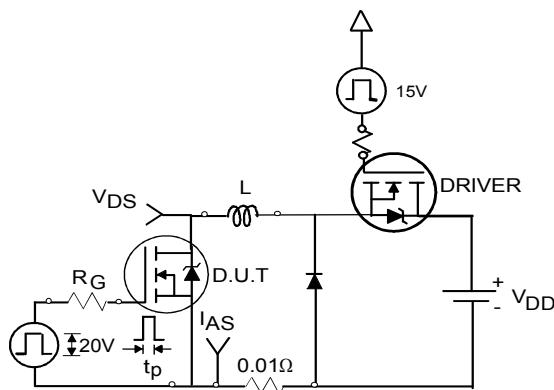


Fig 12a. Unclamped Inductive Test Circuit

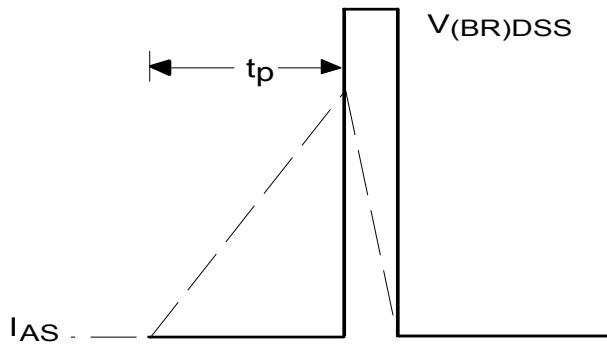


Fig 12b. Unclamped Inductive Waveforms

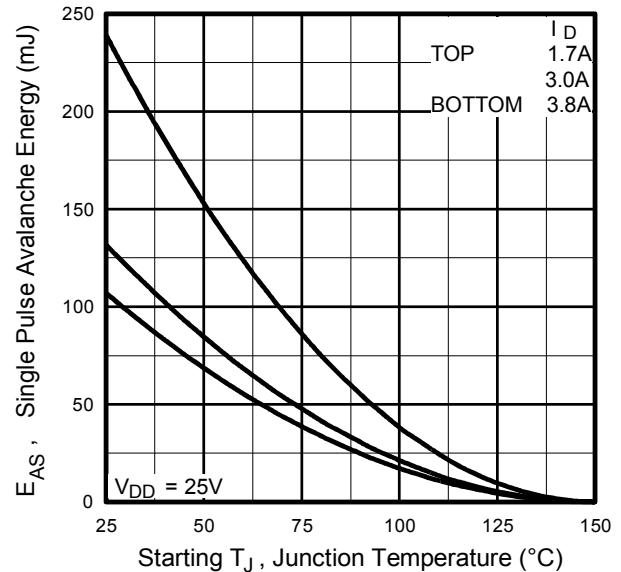
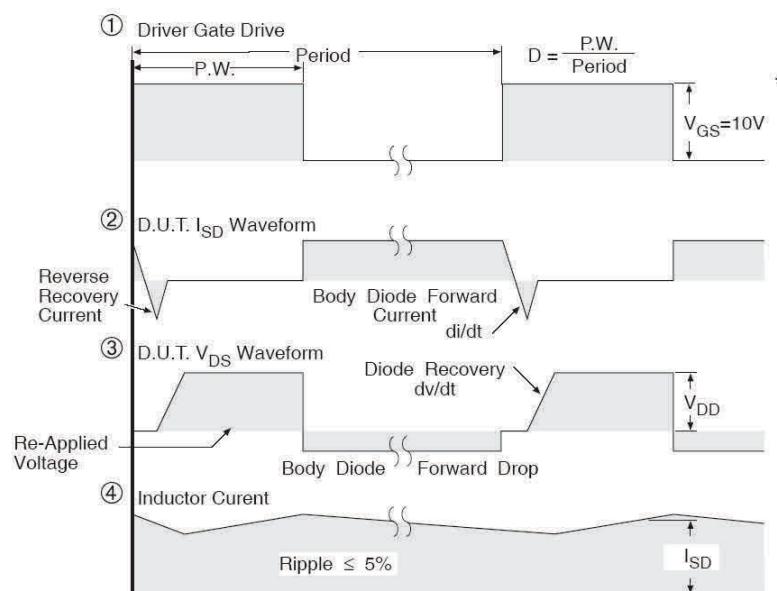
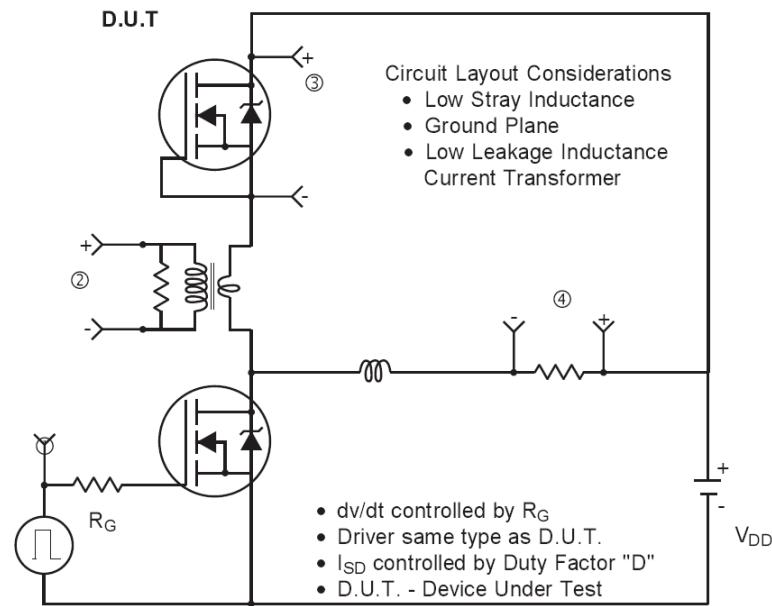


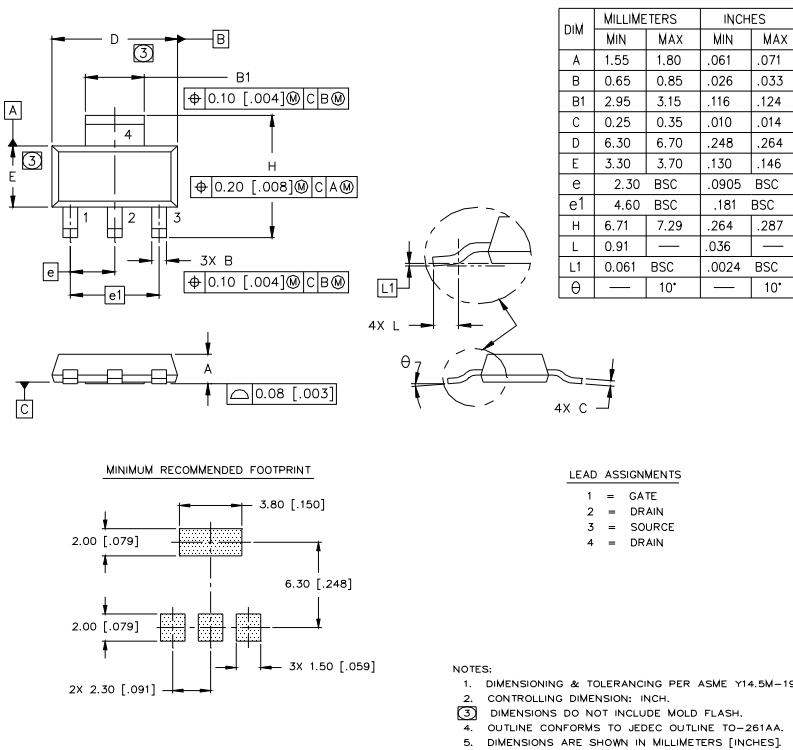
Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Peak Diode Recovery dv/dt Test Circuit

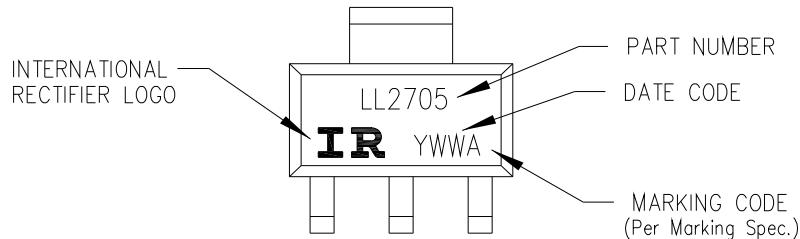
* $V_{GS} = 5V$ for Logic Level Devices

Fig 13. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

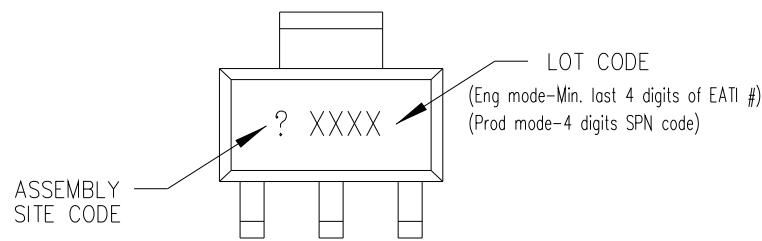
SOT-223 (TO-261AA) Package Outline (Dimensions are shown in millimeters (inches))



SOT-223(TO-261AA) Part Marking Information



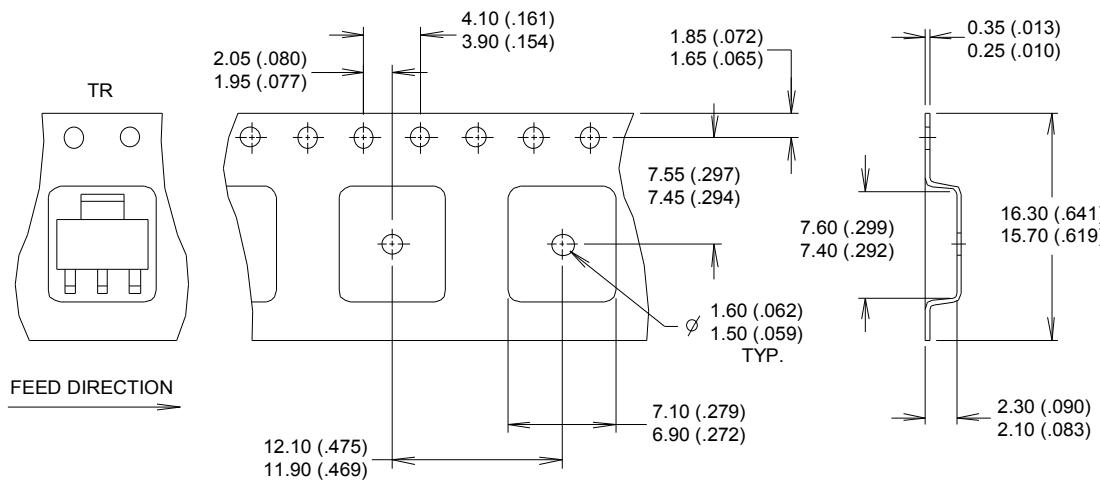
TOP MARKING



BOTTOM MARKING

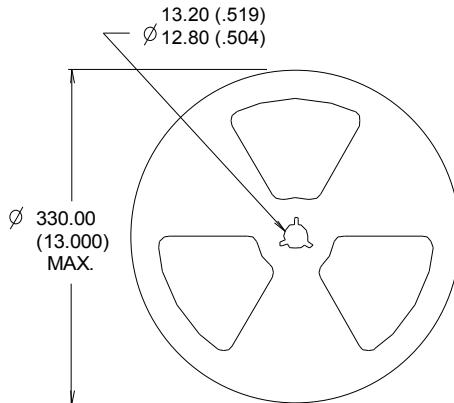
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

SOT-223(TO-261AA) Tape and Reel (Dimensions are shown in millimeters (inches))



NOTES :

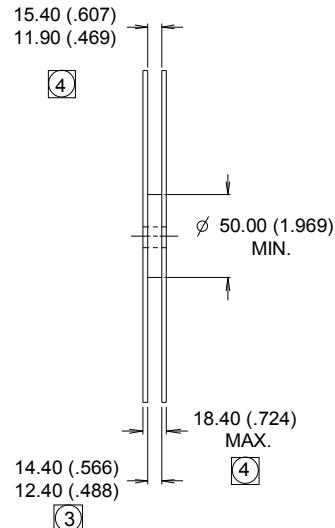
1. CONTROLLING DIMENSION: MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.
 3. EACH Ø330.00 (13.00) REEL CONTAINS 2,500 DEVICES.



NOTES :

- NOTES :

 1. OUTLINE CONFORMS TO EIA-418-1.
 2. CONTROLLING DIMENSION: MILLIMETER..
 3. DIMENSION MEASURED @ HUB.
 4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information

| | | | |
|----------------------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| Qualification Level | | Automotive (per AEC-Q101) | |
| | | Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| Moisture Sensitivity Level | | SOT-223 | MSL1 |
| ESD | Machine Model | Class M2 (+/- 200V) [†] AEC-Q101-002 | |
| | Human Body Model | Class H1B (+/- 750V) [†] AEC-Q101-001 | |
| | Charged Device Model | Class C5 (+/- 1125V) [†] AEC-Q101-005 | |
| RoHS Compliant | | Yes | |

[†] Highest passing voltage.

Revision History

| Date | Comments |
|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3/26/2014 | <ul style="list-style-type: none"> Added "Logic Level Gate Drive" bullet in the features section on page 1 Updated part marking on page 8 Updated data sheet with new IR corporate template |
| 10/29/2015 | <ul style="list-style-type: none"> Updated datasheet with corporate template Corrected ordering table on page 1. |

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