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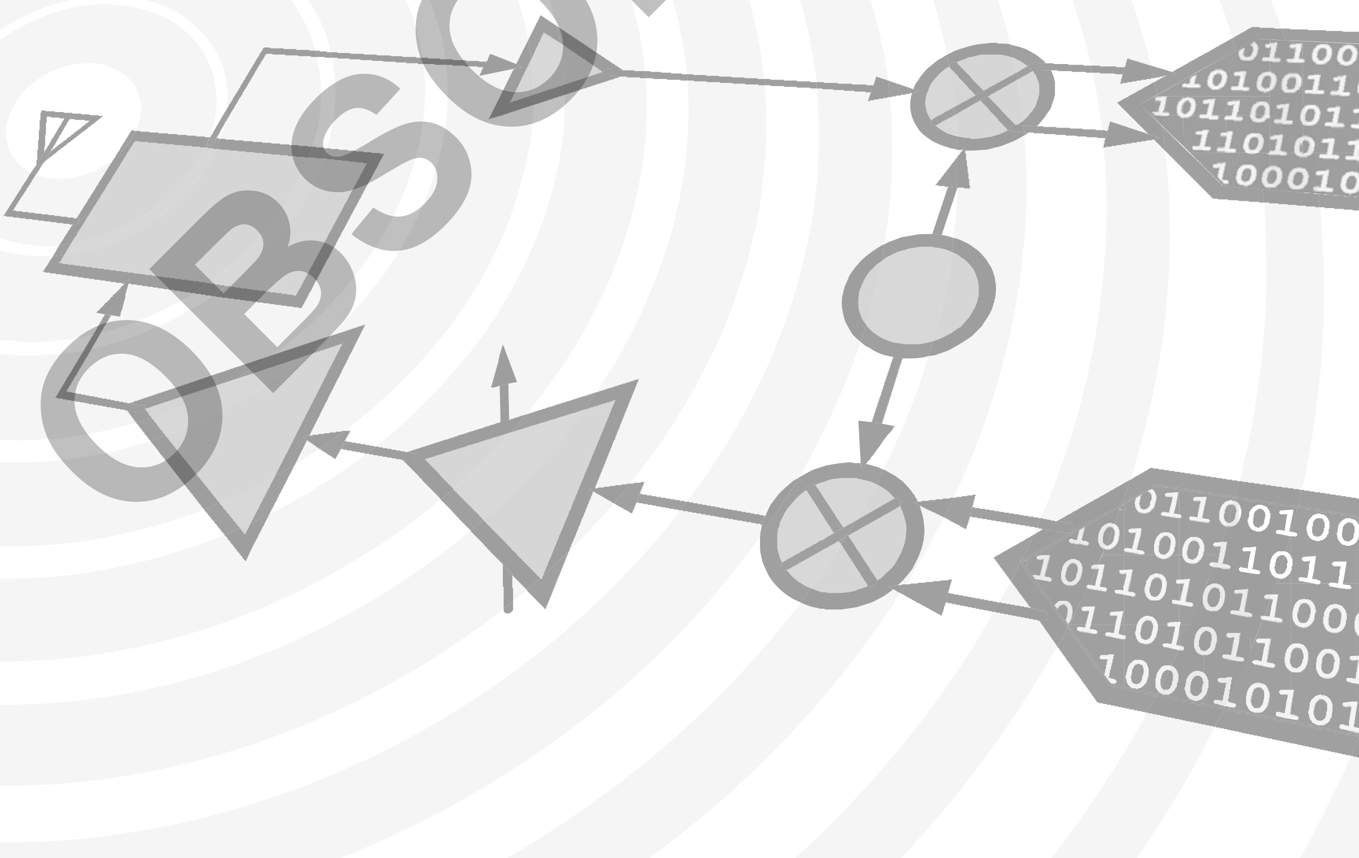
NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED



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HMC742HFLP5E

0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, 0.5 - 4 GHz

RoHS✓ EARTH FRIENDLY

Typical Applications

The HMC742HFLP5E is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

-19 to 12.5 dB Gain Control in 0.5 dB Steps

Power-up State Selection

High Output IP3: +39 dBm

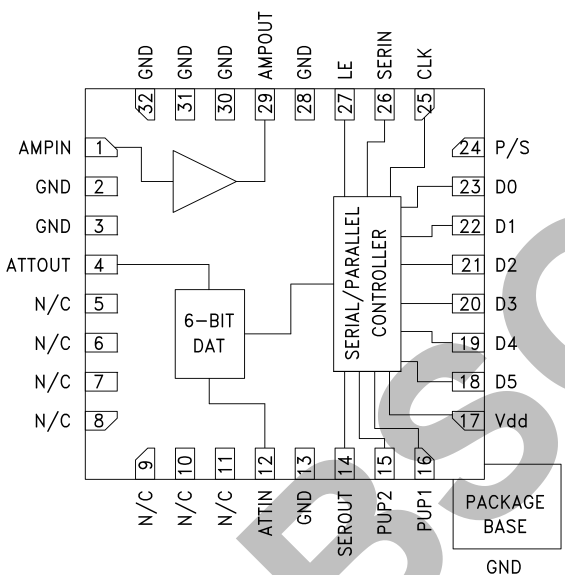
TTL/CMOS Compatible
Serial, Parallel, or latched Parallel Control

±0.25 dB Typical Gain Step Error

Single +5V Supply

32 Lead 5x5mm SMT Package: 25mm²

Functional Diagram



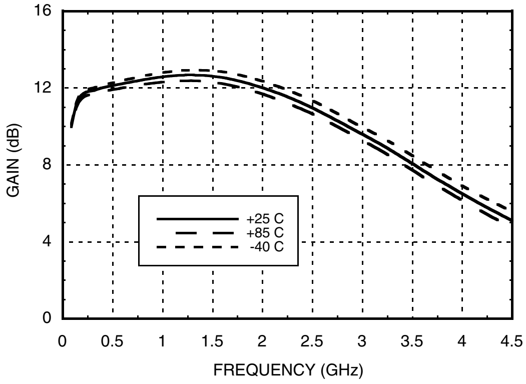
General Description

The HMC742HFLP5E is a digitally controlled variable gain amplifier which operates from 0.5 GHz to 4 GHz, and can be programmed to provide from -19 dB attenuation, to 12.5 dB of gain, in 0.5 dB steps. The HMC742HFLP5E delivers noise figure of 4 dB in its maximum gain state, with output IP3 of up to +39 dBm in any state. The dual mode gain control interface accepts either a three-wire serial input or a 6 bit parallel word. The HMC742HFLP5E also features a user selectable power up state and a serial output for cascading other serially controlled Hittite components. The HMC742HFLP5E is housed in an RoHS compliant 5x5 mm QFN leadless package, and requires minimal external components.

Electrical Specifications, T_A = +25° C, 50 Ohm System Vdd = +5V, Vs= +5V

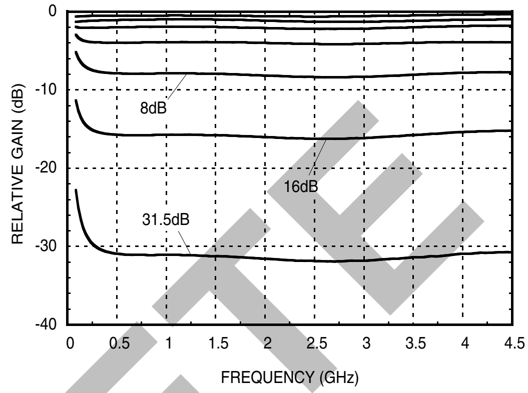
Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		500 - 2700			2700-4000		MHz
Gain (Maximum Gain State)		12.5			9		dB
Gain Control Range		31.5			31.5		dB
Input Return Loss		14			12		dB
Output Return Loss		10			12		dB
Gain Accuracy: (Referenced to Maximum Gain State) All Gain States		± (0.3 + 4% of relative gain setting) Max					dB
Output Power for 1 dB Compression		21			22		dBm
Output Third Order Intercept Point (Two-Tone Output Power= 12 dBm Each Tone)		39			38		dBm
Noise Figure (Max Gain State)		4			4.5		dB
Switching Characteristics tRISE, tFall (10 / 90% RF)		30			30		ns
tON, tOFF (Latch Enable to 10 / 90% RF)		60			60		ns
Supply Current (Amplifier)	130	150	175	130	150	175	mA
Supply Current (Controller) Idd		0.12	0.25		0.12	0.25	mA

Maximum Gain vs. Frequency

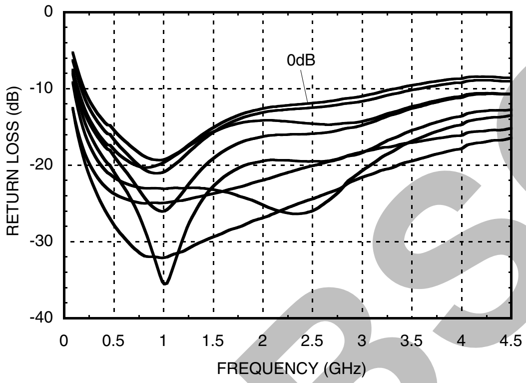


Relative Gain Setting

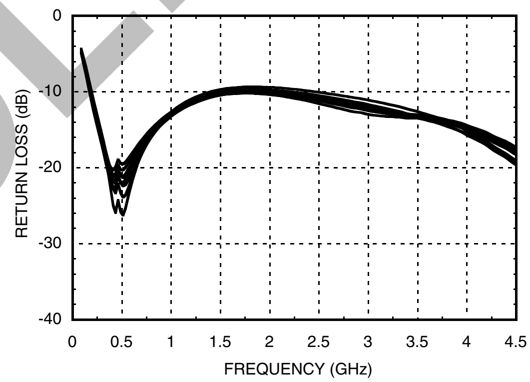
(Referenced to Maximum Gain State)



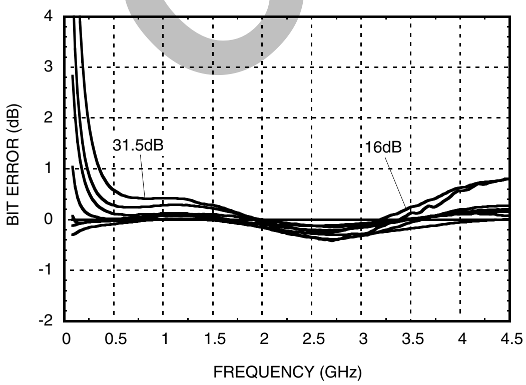
Input Return Loss



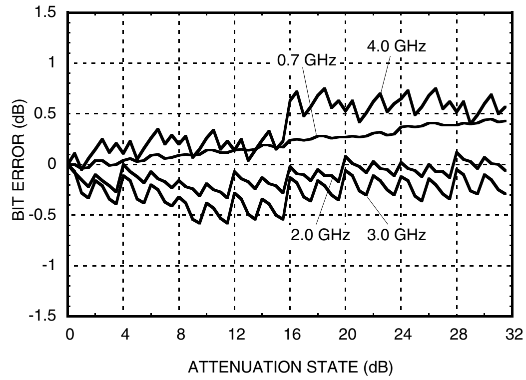
Output Return Loss



Bit Error vs. Frequency



Bit Error vs. Attenuation State



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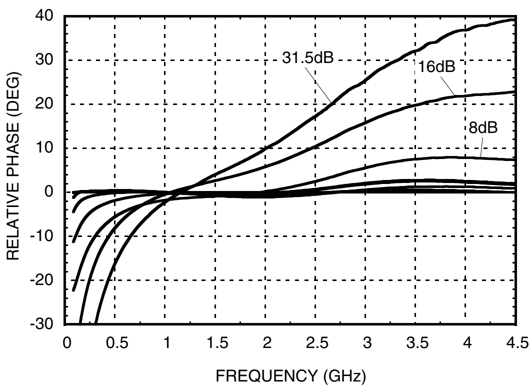
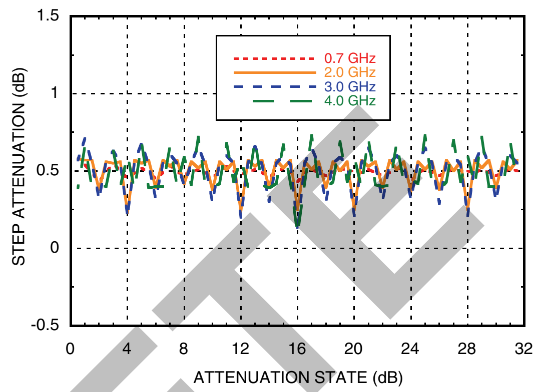
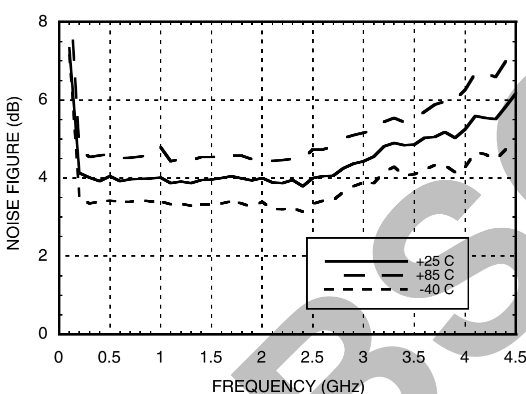
Relative Phase vs. Frequency (Referenced to Maximum Gain State)



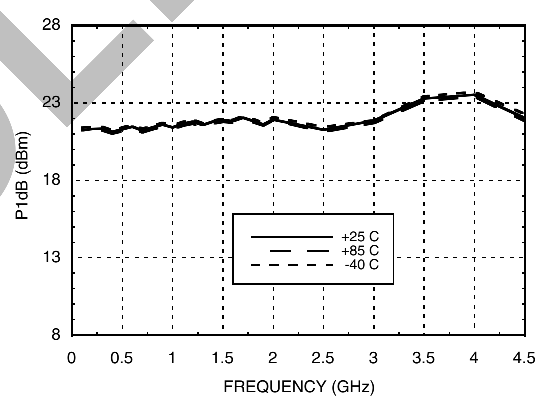
Step Attenuation vs. Attenuation State



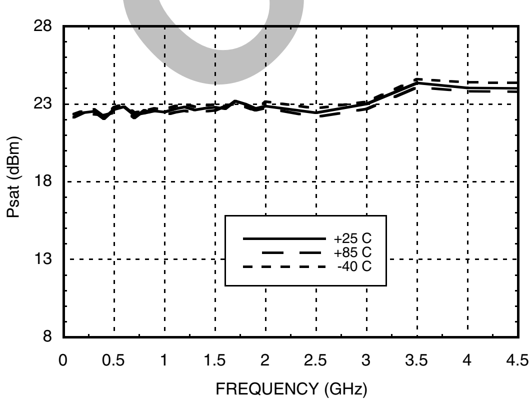
Noise Figure vs. Frequency [1]



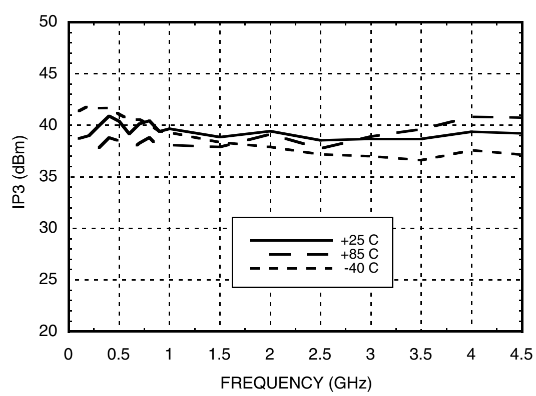
Output P1dB vs. Temperature



Psat vs. Temperature



Output IP3 vs. Temperature



[1] Max Gain State

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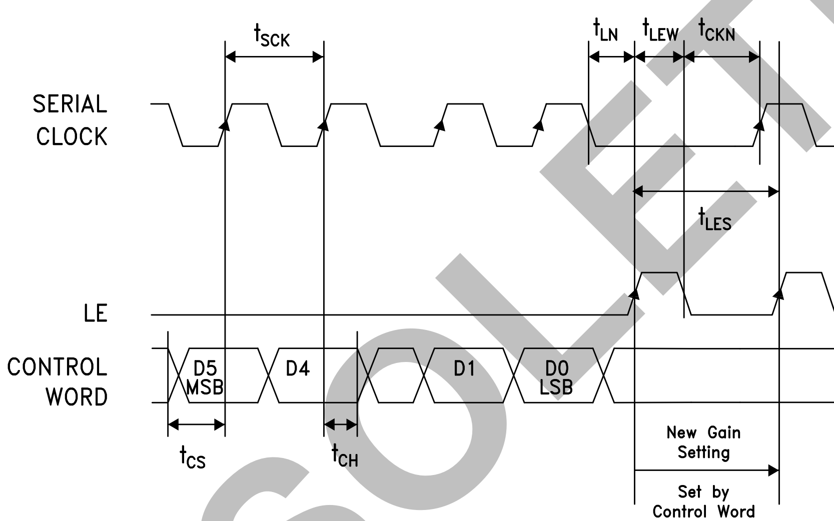
Serial Control Interface

The HMC742HFLP5E contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). The serial control interrface is activated when P/S is kept high. The 6-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. If mechanical switches are used, sufficient debouncing should be provided. When LE is high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high CLK is masked to prevent data transition during output loading.

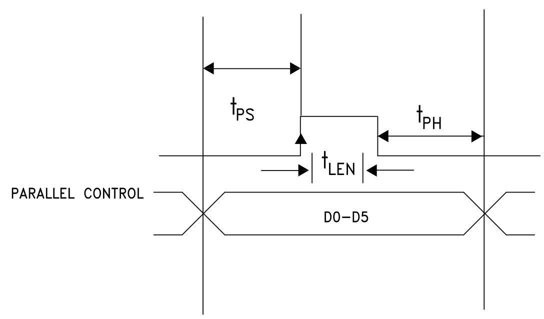
When P/S is low, 3-wire SPI interface inputs (SERIN, CLK, LE) are disabled and the input register is loaded with parallel digital inputs (D0-D5). When LE is high, 6-bit parallel data changes the state of the part per truth table.

For all modes of operations, the DVGA state will stay constant while LE is kept low.



Parameter	Typ.
Min. serial period, t_{SCK}	100 ns
Control set-up time, t_{CS}	20 ns
Control hold-time, t_{CH}	20 ns
LE setup-time, t_{LN}	10 ns
Min. LE pulse width, t_{LEW}	10 ns
Min LE pulse spacing, t_{LES}	630 ns
Serial clock hold-time from LE, t_{CKN}	10 ns
Hold Time, $t_{PH.}$	0 ns
Latch Enable Minimum Width, t_{LEN}	10 ns
Setup Time, t_{PS}	2 ns

Timing Diagram (Latched Parallel Mode)



Parallel Mode
(Direct Parallel Mode & Latched Parallel Mode)

Note: The parallel mode is enabled when P/S is set to low.

Direct Parallel Mode - The attenuation state is changed by the control voltage inputs D0-D5 directly. The LE (Latch Enable) must be at a logic high at all times to control the attenuator in this manner.

Latched Parallel Mode - The attenuation state is selected using the control voltage inputs D0-D5 and set while the LE is in the Low state. The attenuator will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram above for reference.

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Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. If the LE is set to logic HIGH at power-up, the logic state of D0-D5 determines the power-up state of the part per truth table. The DVGA latches in the desired power-up state approximately 200 ms after power-up.

Power-On Sequence

The ideal power-up sequence is: GND, Vdd, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after Vdd / GND

PUP Truth Table

LE	PUP1	PUP2	Gain Relative to Maximum Gain
0	0	0	-31.5
0	1	0	-24
0	0	1	-16
0	1	1	Insertion Loss
1	X	X	0 to -31.5 dB

Note: The logic state of D0 - D5 determines the power-up state per truth table shown below when LE is high at power-up.

Absolute Maximum Ratings

RF Input Power at Max Gain [1]	17.5 dBm (T = +85 °C)
Digital Inputs (LE, SERIN, CLK, P/S, DO-D5, PUP1, PUP2)	-0.5 to Vdd +0.5V
Controller Bias Voltage (Vdd)	5.6V
Amplifier Bias Voltage (Vcc)	5.5V
Channel Temperature	175 °C
Continuous Pdiss (T = 85 °C) (derate 13.3 mW/°C above 85 °C) [2]	1.2 W
Thermal Resistance [3]	75.6 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

[1] The maximum RF input power increases by the same amount the gain is reduced. The maximum input power at any state is no more than 28 dBm.

[2] This value does not include the RF power dissipation in the attenuator. The loss in the attenuator depends on the state of the attenuator. The loss in the attenuator should be included to determine the total power dissipation in the part.

[3] This value does not include the RF power dissipation in the attenuator. The thermal resistance at different states of the attenuator can be determined based on note [2]

Truth Table

Control Voltage Input						Gain Relative to Maximum Gain
D5	D4	D3	D2	D1	D0	
High	High	High	High	High	High	0 dB
High	High	High	High	High	Low	-0.5 dB
High	High	High	High	Low	High	-1 dB
High	High	High	Low	High	High	-2 dB
High	High	Low	High	High	High	-4 dB
High	Low	High	High	High	High	-8 dB
Low	High	High	High	High	High	-16 dB
Low	Low	Low	Low	Low	Low	-31.5 dB
Any combination of the above states will provide a reduction in gain approximately equal to the sum of the bits selected.						

Control Voltage Table

State	Vdd = +3V	Vdd = +5V
Low	0 to 0.5V @ <1 µA	0 to 0.8V @ <1 µA
High	2 to 3V @ <1 µA	2 to 5V @ <1 µA

Bias Voltage

Vdd (V)	Idd (Typ.) (mA)
+5.0	0.12
Vs (V)	Is (mA)
+5.0	150

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

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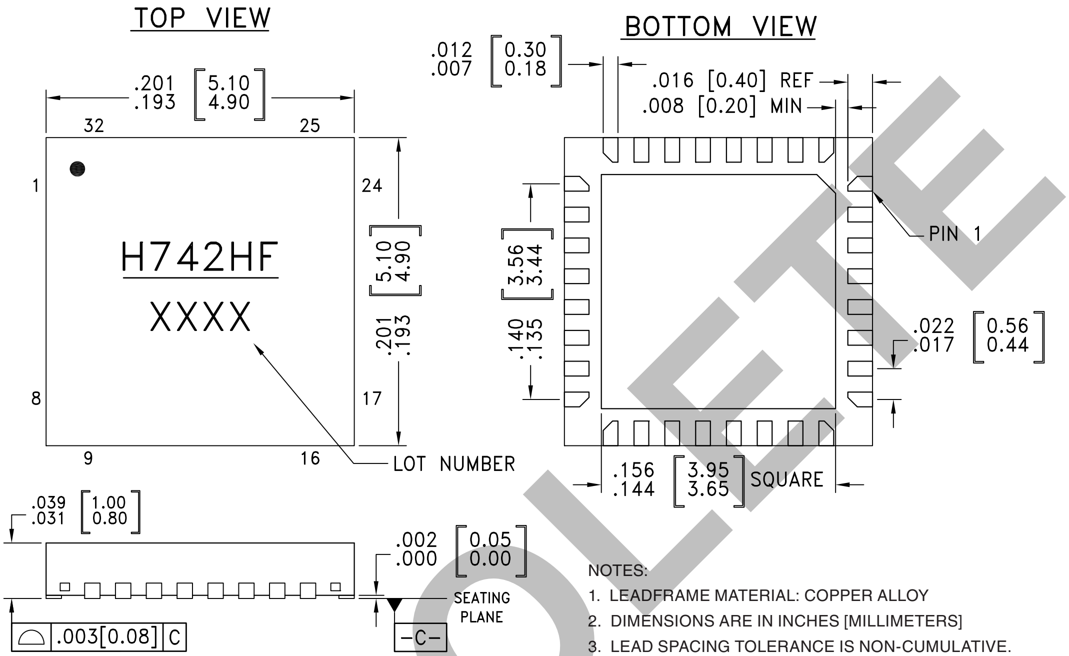
Outline Drawing



NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC742HFLP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H742HF XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

For price, delivery and to place orders: Hittite Microwave Corporation, 20 Alpha Road, Chelmsford, MA 01824
Phone: 978-250-3343 Fax: 978-250-3373 Order On-line at www.hittite.com
Application Support: Phone: 978-250-3343 or apps@hittite.com

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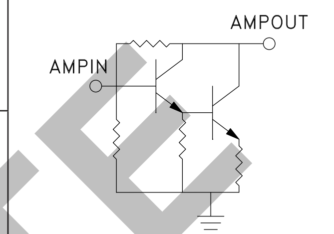
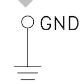
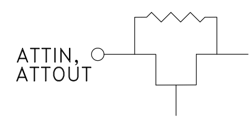
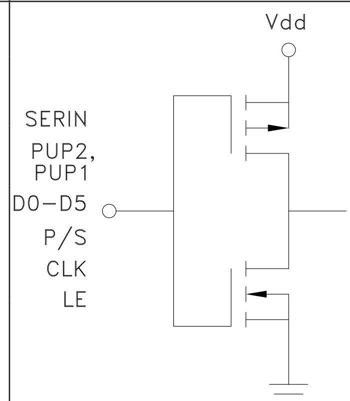
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	AMPIN	This pin is DC coupled. An off chip DC blocking capacitor is required.	
29	AMPOUT	RF output and DC bias (Vcc) for the output stage of the amplifier.	
2, 3, 13, 28, 30 - 32	GND	These pins and package bottom must be connected to RF/DC ground.	
4, 12	ATTIN, ATTOUT	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
5 - 11	N/C	No connection	
14	SEROUT	Serial input data delayed by 6 clock cycles.	
15, 16	PUP2, PUP1		
18 - 23	D5, D4, D3, D2, D1, D0		
24	P/S		
25	CLK		
26	SERIN		
27	LE		
17	Vdd	Supply Voltage	

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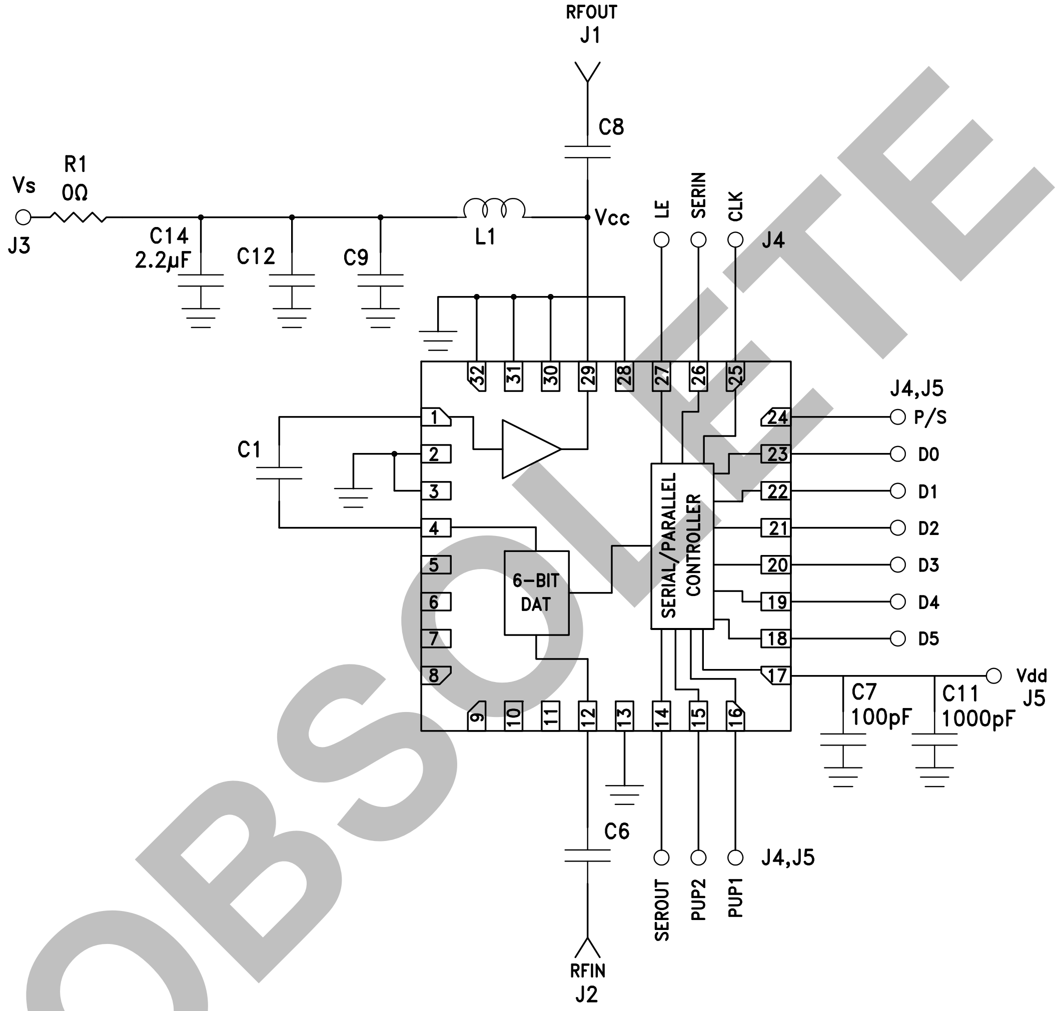
Application Circuit



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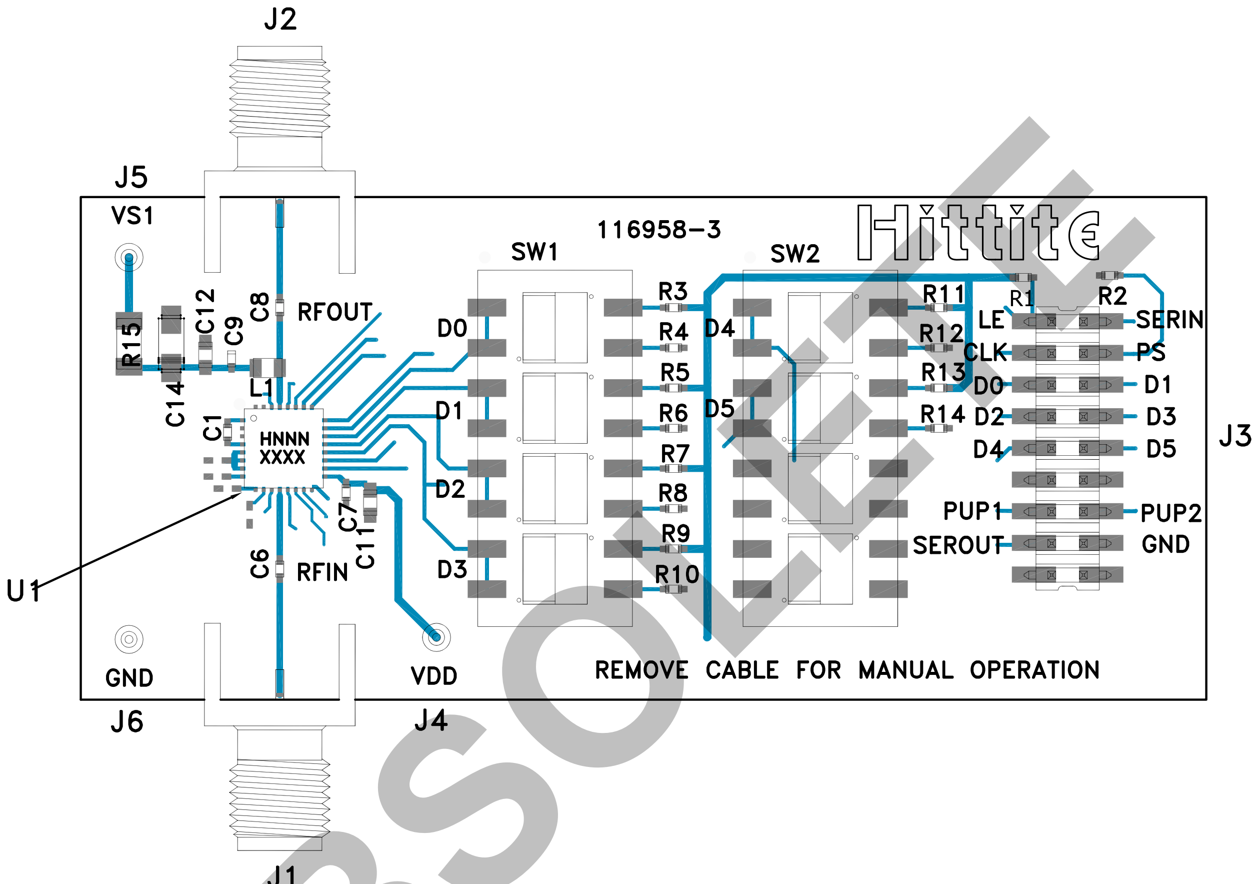
Evaluation PCB



List of Materials for Evaluation PCB 124695[1]

Item	Description
J1 - J2	PCB Mount SMA Connectors
J3	18 Pin DC Connector
J4 - J6	DC Pin
C1, C6, C8, C9	330pF Capacitor, 0402 Pkg.
C7	100pF Capacitor. 0402 Pkg.
C11	1000 pF Capacitor, 0402 Pkg.
C12	1000 pF Capacitor, 0603 Pkg.
C14	2.2 μF Capacitor, CASE A Pkg.
R1 - R14	100 kOhm Resistor, 0402 Pkg.
R15	0 Ohm Resistor, 1206 Pkg.
L1	47 nH Inductor, 0603 Pkg.
SW1, SW2	SPDT 4 Position DIP Switch
U1	HMC742HFLP5E Variable Gain Amplifier
PCB [2]	116958 Evaluation PCB

[1] Reference this number when ordering evaluation PCB
[2] Circuit Board Material: Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Notes: