

N- and P-Channel 20V (D-S) Power MOSFET

FEATURES

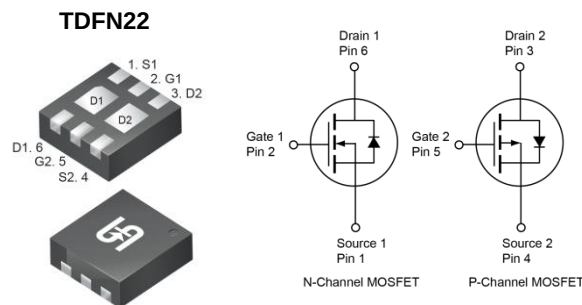
- Low $R_{DS(on)}$ to minimize conductive losses
- Low gate charge for fast power switching
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

APPLICATIONS

- Load Switch
- Power Management
- Portable Devices

KEY PERFORMANCE PARAMETERS

PARAMETER		TYPE	VALUE	UNIT
V_{DS}		N-ch	20	V
		P-ch	-20	
$R_{DS(on)}$ (max)	$V_{GS} = 4.5V$	N-ch	30	mΩ
	$V_{GS} = 2.5V$		36	
	$V_{GS} = 1.8V$		42	
	$V_{GS} = -4.5V$	P-ch	55	
	$V_{GS} = -2.5V$		78	
	$V_{GS} = -1.8V$		90	
Q_g		N-ch	9.1	nC
		P-ch	9.8	



Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	N-ch	P-ch	UNIT
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	± 12	± 12	V
Continuous Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_D	11.6	-9	A
	$T_A = 25^\circ\text{C}$		6.4	-5	
Pulsed Drain Current		I_{DM}	46.4	-36	A
Total Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	6.25	6.25	W
	$T_C = 125^\circ\text{C}$		1.25	1.25	
Total Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	1.89	1.89	W
	$T_A = 125^\circ\text{C}$		0.38	0.38	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150		$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	20	$^\circ\text{C/W}$
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	66	

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)							
PARAMETER	CONDITIONS	SYMBOL	TYPE	MIN	TYP	MAX	UNIT
Static							
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	N-ch	20	--	--	V
	V _{GS} = 0V, I _D = -250μA		P-ch	-20	--	--	
Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250μA	V _{GS(TH)}	N-ch	0.5	0.8	1	V
	V _{GS} = V _{DS} , I _D = -250μA		P-ch	-0.45	-0.7	-1	
Gate-Source Leakage Current	V _{GS} = ±12V, V _{DS} = 0V	I _{GSS}	N-ch	--	--	±100	nA
	V _{GS} = ±12V, V _{DS} = 0V		P-ch	--	--	±100	
Drain-Source Leakage Current	V _{GS} = 0V, V _{DS} = 20V	I _{DSS}	N-ch	--	--	1	μA
	V _{GS} = 0V, V _{DS} = 20V T _J = 125°C			--	--	100	
	V _{GS} = 0V, V _{DS} = -20V		P-ch	--	--	-1	
	V _{GS} = 0V, V _{DS} = -20V T _J = 125°C			--	--	-100	
Drain-Source On-State Resistance ^(Note 2)	V _{GS} = 4.5V, I _D = 6.4A	R _{DS(on)}	N-ch	--	17	30	mΩ
	V _{GS} = 2.5V, I _D = 5.8A			--	22	36	
	V _{GS} = 1.8V, I _D = 5.4A			--	32	42	
	V _{GS} = -4.5V, I _D = -5A		P-ch	--	48	55	
	V _{GS} = -2.5V, I _D = -4.2A			--	60	78	
	V _{GS} = -1.8V, I _D = -3.9A			--	78	90	
Forward Transconductance ^(Note 2)	V _{DS} = 5V, I _D = 6.4A	g _{fs}	N-ch	--	28	--	S
	V _{DS} = -5V, I _D = -5A		P-ch	--	15	--	
Dynamic ^(Note 3)							
Total Gate Charge	N-ch V _{GS} = 4.5V, V _{DS} = 10V, I _D = 6.4A P-ch	Q _g	N-ch	--	9.1	--	nC
Gate-Source Charge			P-ch	--	9.8	--	
		Gate-Drain Charge	Q _{gs}	N-ch	--	1.3	
P-ch				--	1.1	--	
Gate-Drain Charge	V _{GS} = -4.5V, V _{DS} = -10V, I _D = -5A	Q _{gd}	N-ch	--	2.7	--	
			P-ch	--	2.7	--	
Input Capacitance	N-ch V _{GS} = 0V, V _{DS} = 10V f = 1.0MHz P-ch	C _{iss}	N-ch	--	677	--	pF
P-ch			--	744	--		
Output Capacitance		C _{oss}	N-ch	--	120	--	
			P-ch	--	106	--	
Reverse Transfer Capacitance	V _{GS} = 0V, V _{DS} = -10V f = 1.0MHz	C _{rss}	N-ch	--	89	--	
			P-ch	--	97	--	
Gate Resistance	f = 1.0MHz	R _g	N-ch	--	3	--	Ω
			P-ch	--	80	--	

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	TYPE	MIN	TYP	MAX	UNIT
Switching ^(Note 3)							
Turn-On Delay Time	N-ch V _{GS} = 4.5V, R _G = 2Ω V _{DS} = 10V, I _D = 6.4A P-ch V _{GS} = -4.5V, R _G = 2Ω V _{DS} = -10V, I _D = -5A	t _{d(on)}	N-ch	--	8	--	ns
			P-ch	--	10	--	
Turn-On Rise Time		t _r	N-ch	--	41	--	
			P-ch	--	34	--	
Turn-Off Delay Time		t _{d(off)}	N-ch	--	25	--	
			P-ch	--	69	--	
Turn-Off Fall Time		t _f	N-ch	--	30	--	
			P-ch	--	68	--	
Source-Drain Diode							
Forward Voltage ^(Note 2)	V _{GS} = 0V, I _S = 6.4A	V _{SD}	N-ch	--	0.7	--	V
	V _{GS} = 0V, I _S = -5A		P-ch	--	-0.8	--	
Reverse recovery Time	N-ch I _S = 6.4A, dI/dt=100A/μs	t _{rr}	N-ch		22		nc
			P-ch		113		
Reverse Recovery Charge	P-ch I _S = -5A, dI/dt=100A/μs	Q _{rr}	N-ch	--	6		nc
			P-ch	--	160		

Notes:

1. Silicon limited current only.
2. Pulse test: Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Switching time is essentially independent of operating temperature.

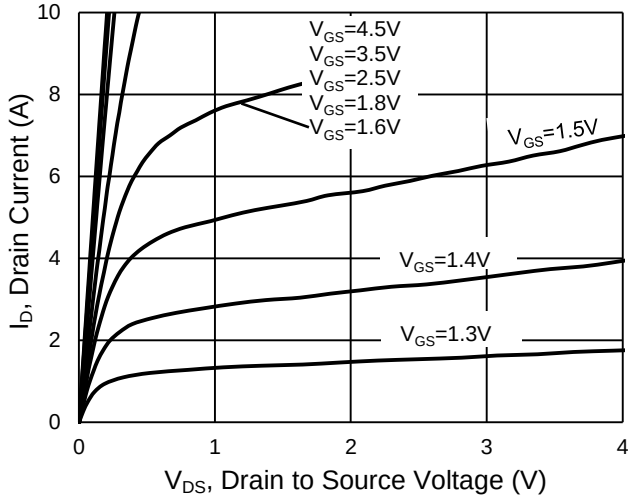
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM2537CQ RFG	TDFN22	3,000pcs / 7" Reel

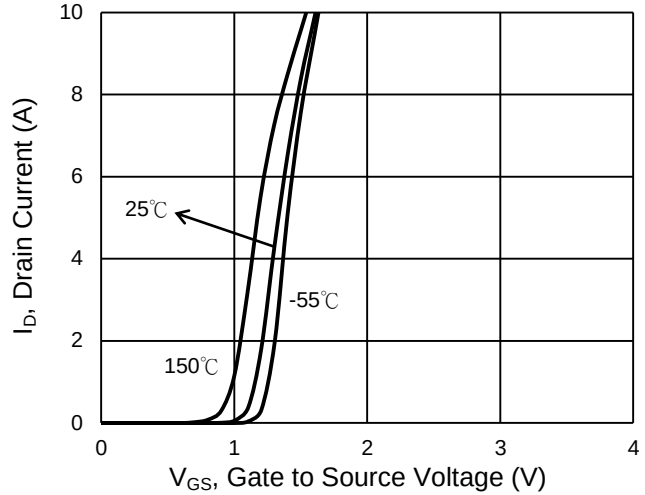
CHARACTERISTICS CURVES (N-Channel)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

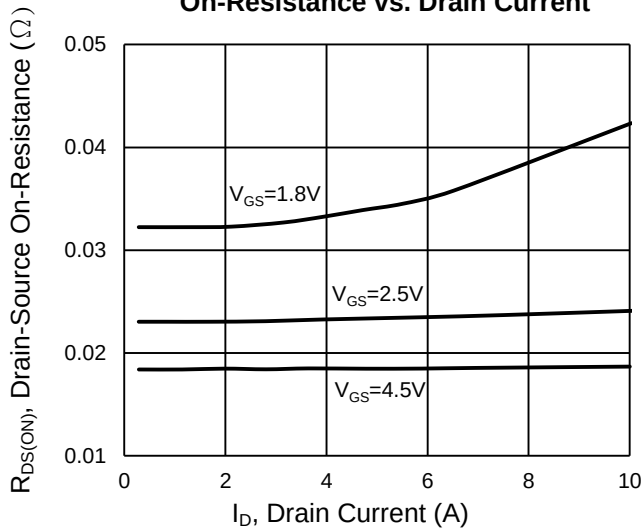
Output Characteristics



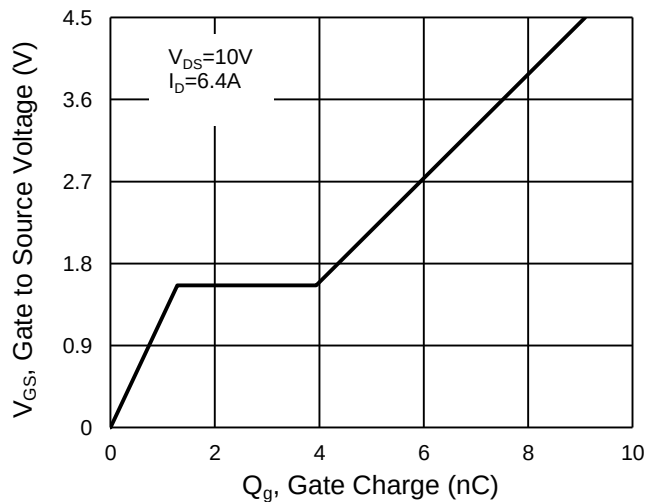
Transfer Characteristics



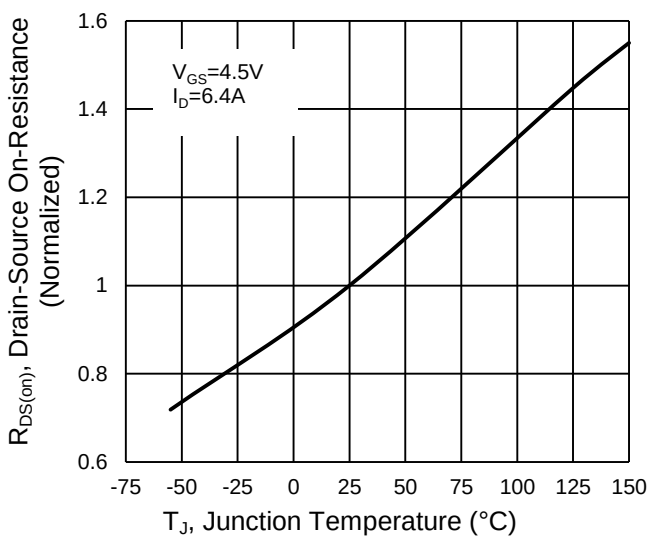
On-Resistance vs. Drain Current



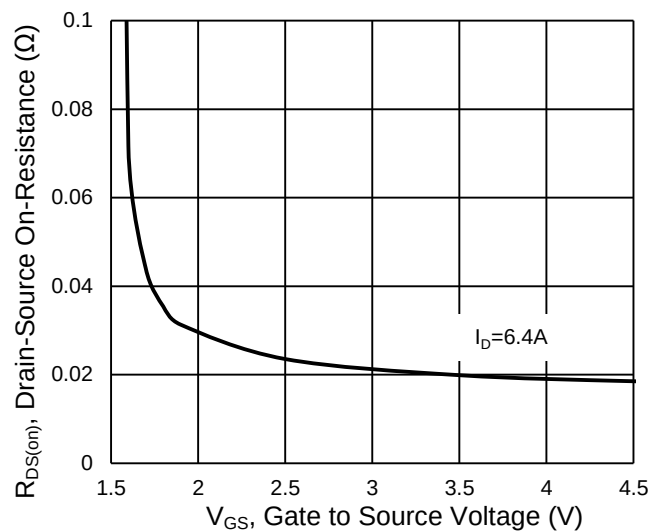
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



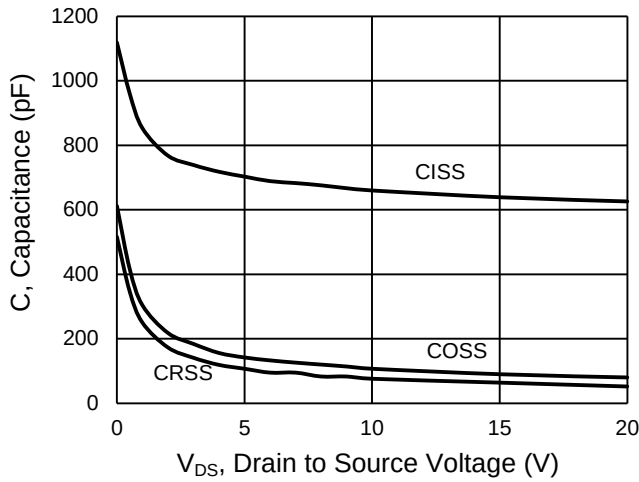
On-Resistance vs. Gate-Source Voltage



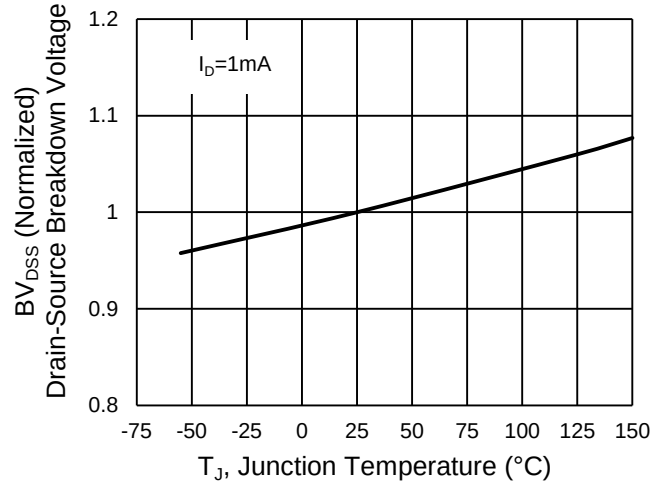
CHARACTERISTICS CURVES (N-Channel)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

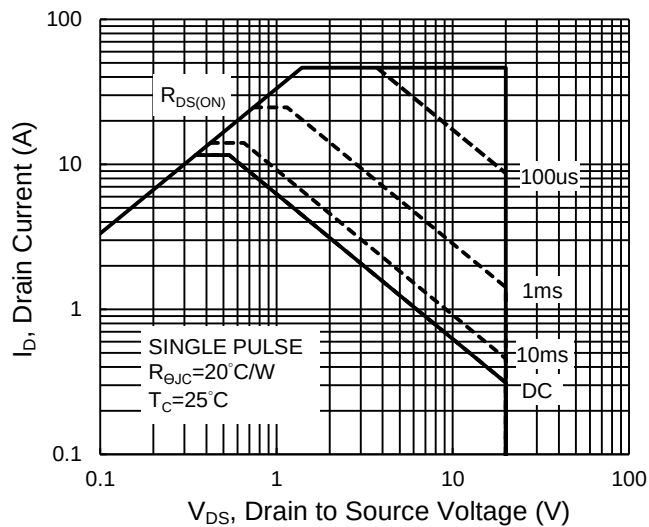
Capacitance vs. Drain-Source Voltage



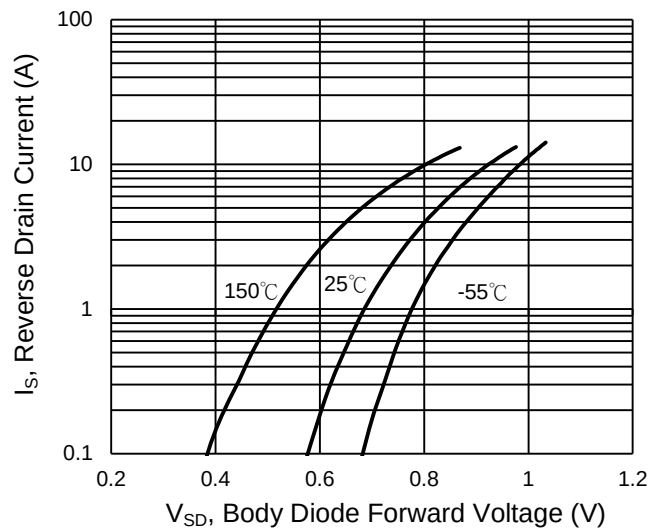
BV_{DSS} vs. Junction Temperature



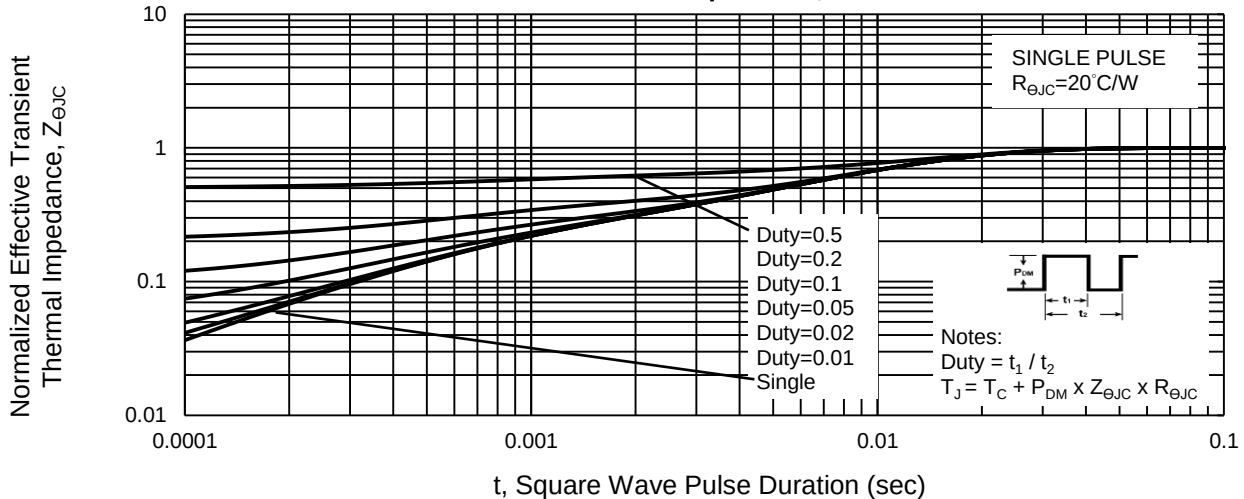
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



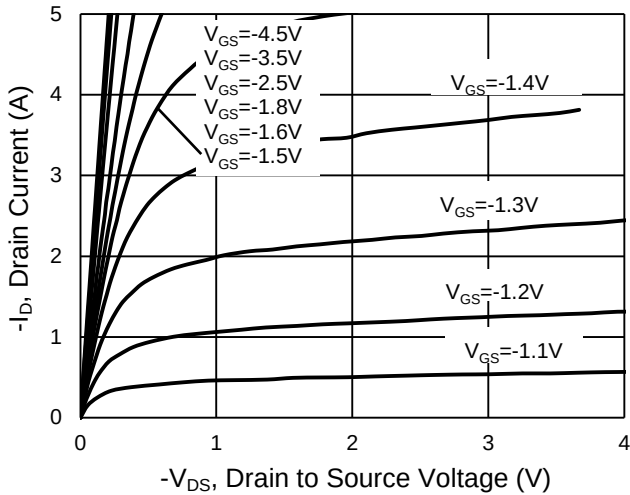
Normalized Thermal Transient Impedance, Junction-to-Case



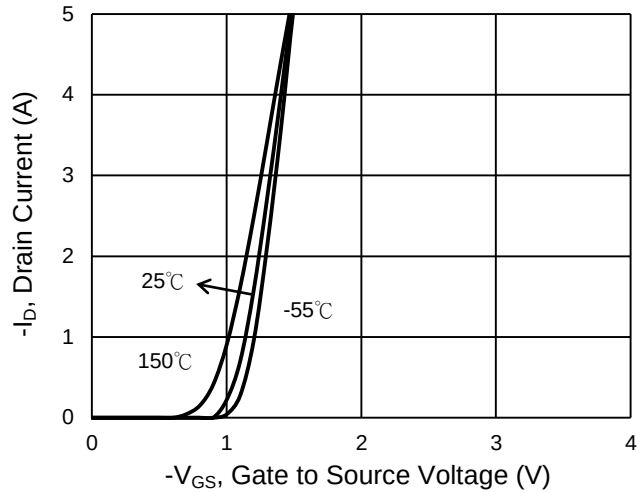
CHARACTERISTICS CURVES (P-Channel)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

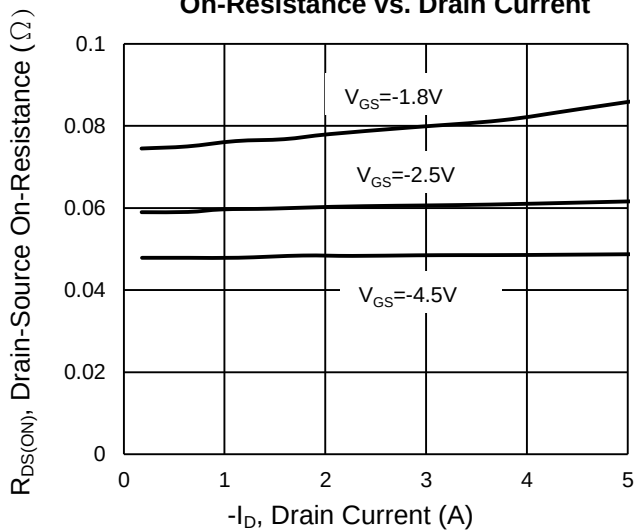
Output Characteristics



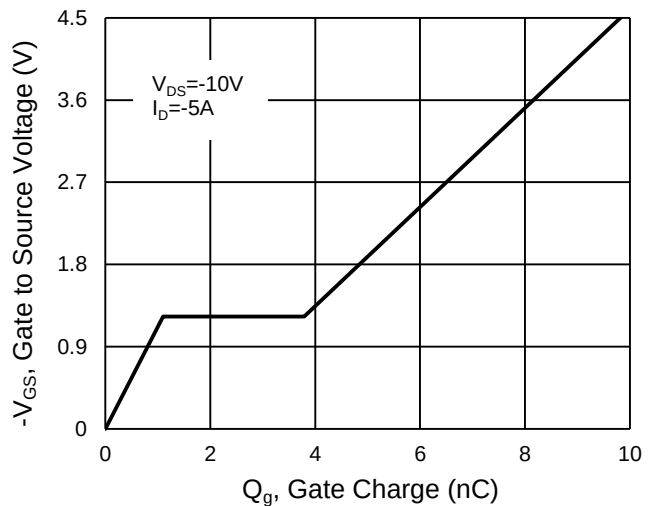
Transfer Characteristics



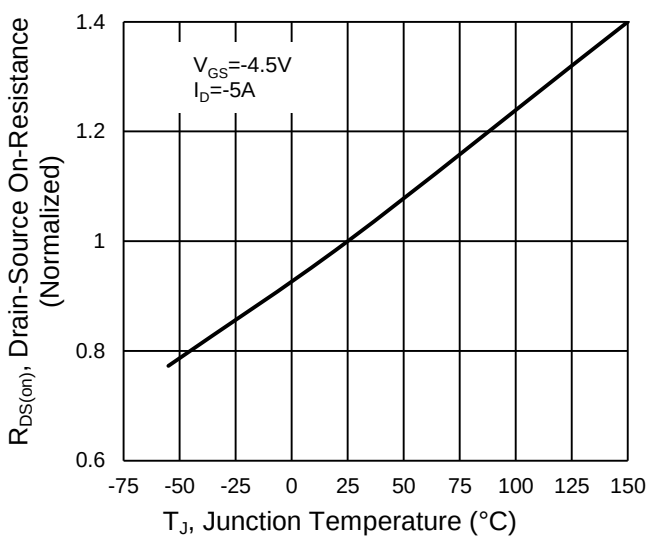
On-Resistance vs. Drain Current



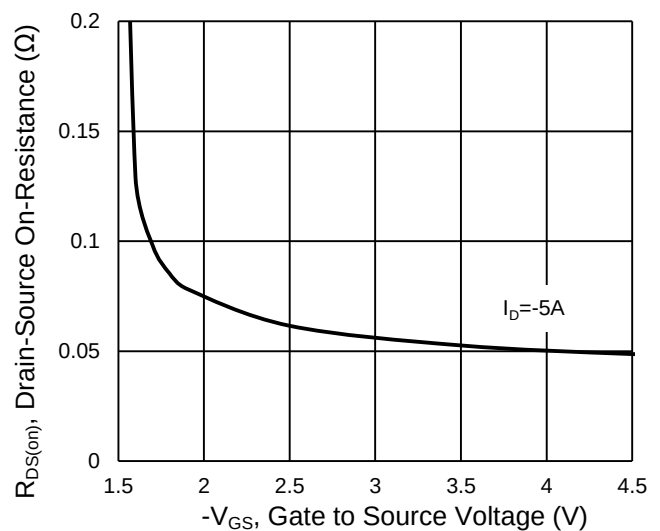
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



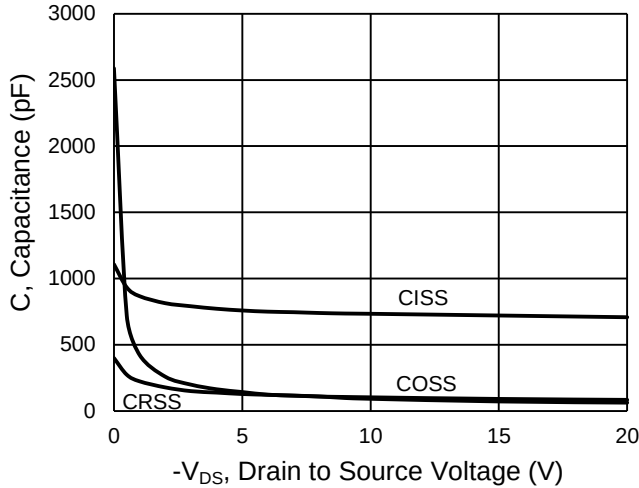
On-Resistance vs. Gate-Source Voltage



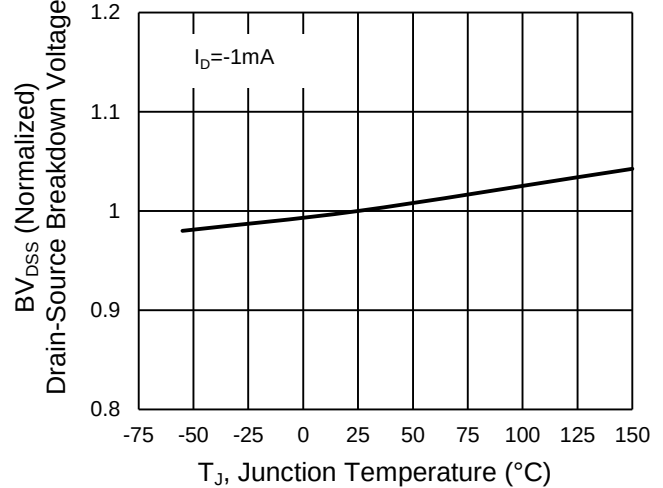
CHARACTERISTICS CURVES (P-Channel)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

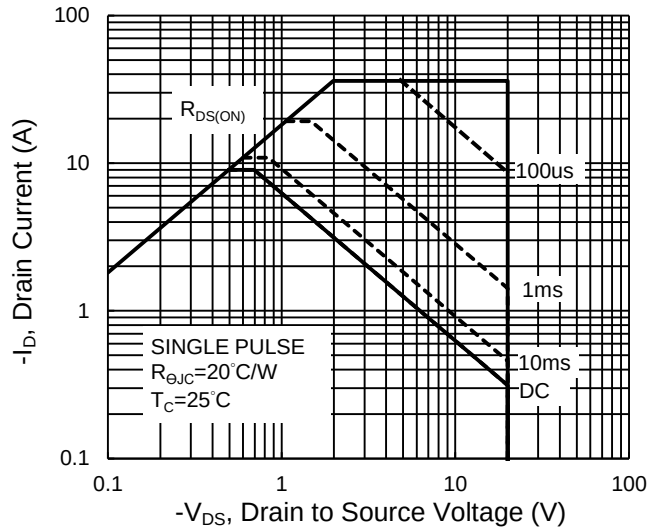
Capacitance vs. Drain-Source Voltage



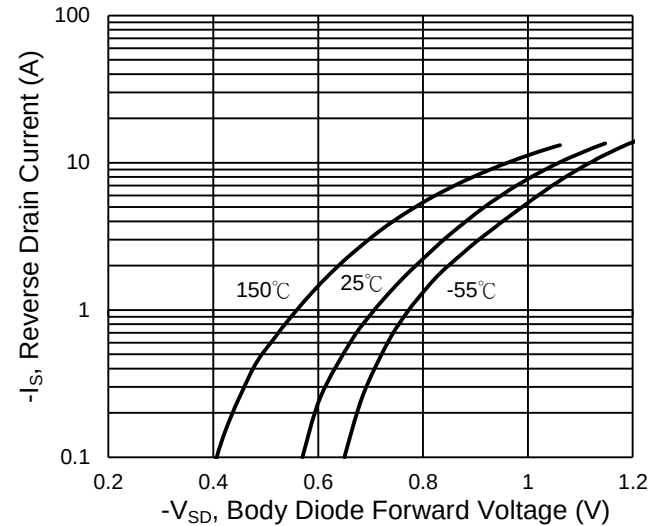
BV_{DSS} vs. Junction Temperature



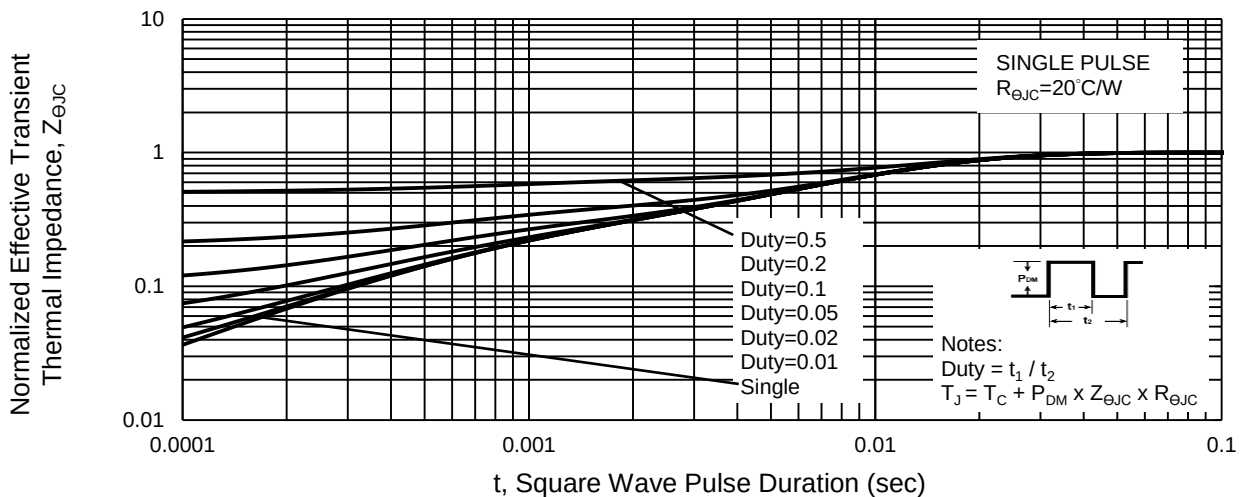
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

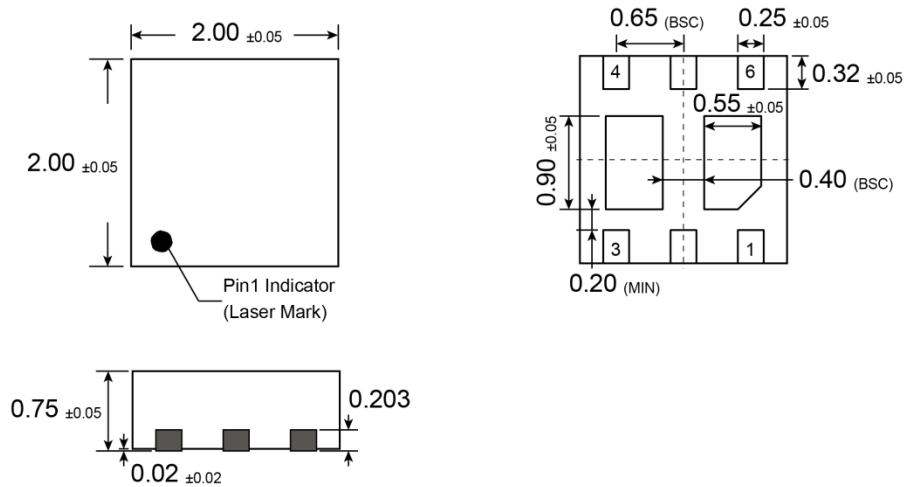


Normalized Thermal Transient Impedance, Junction-to-Case

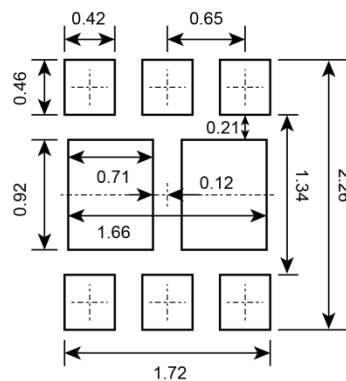


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

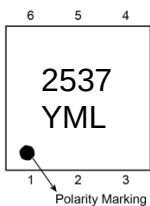
TDFN22



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



Y = Year Code

M = Month Code for Halogen Free

O =Jan **P** =Feb **Q** =Mar **R** =Apr

S =May **T** =Jun **U** =Jul **V** =Aug

W =Sep **X** =Oct **Y** =Nov **Z** =Dec

L = Lot Code (1~9, A~Z)

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