

Multimode (LVD/SE) SCSI 9 Line Terminator

FEATURES

- Auto Selection Multi-Mode Single Ended or Low Voltage Differential Termination
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Built-in SPI-3 Mode Change Filter/Delay
- Meets SCSI-1, SCSI-2, Ultra2 (SPI-2 LVD), Ultra3/Ultra160 (SPI-3) and Ultra320 (SPI-4) Standards
- Supports Active Negation
- 3pF Channel Capacitance

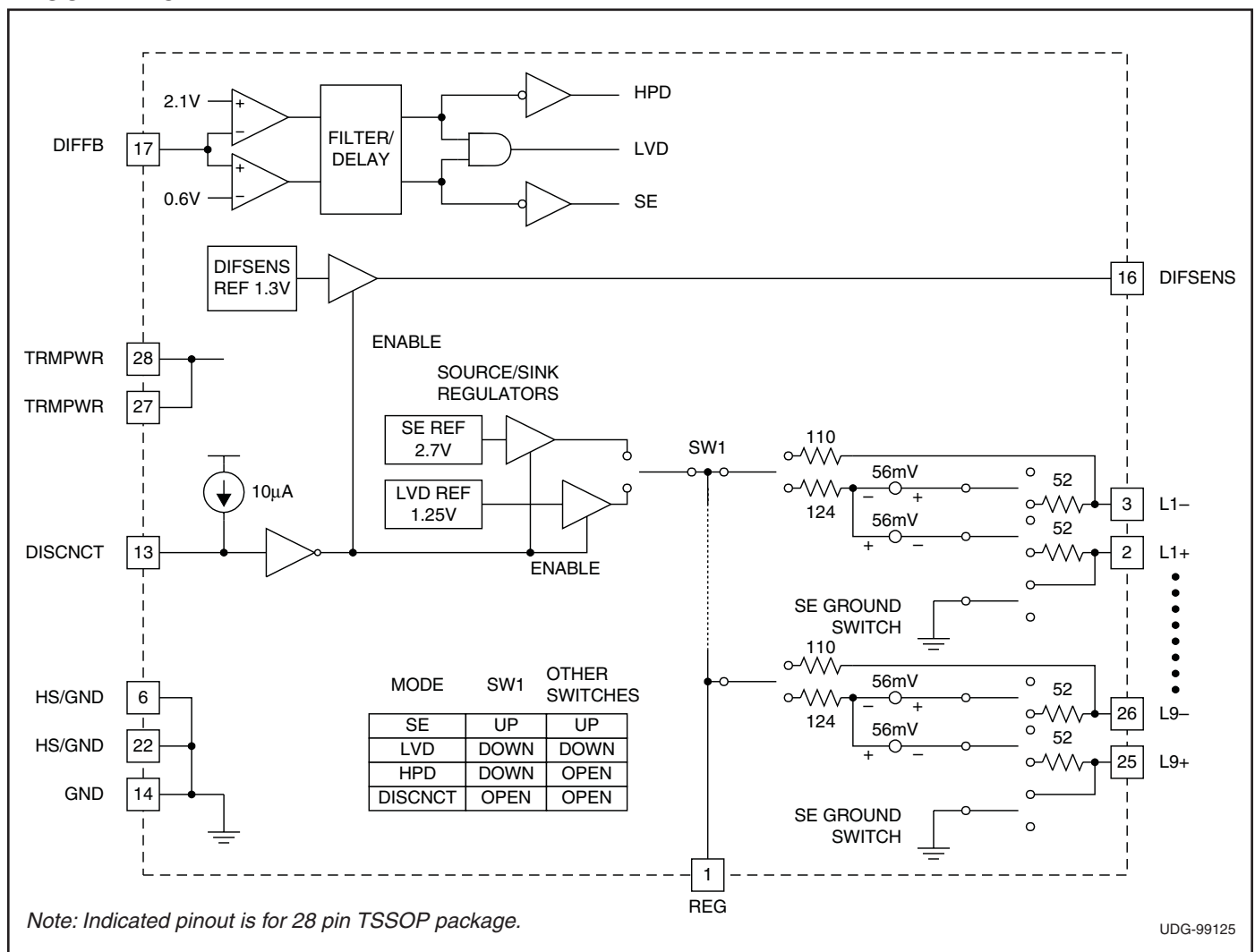
DESCRIPTION

The UCC5672 Multi-Mode Low Voltage Differential and Single Ended Terminator is both a single ended terminator and a low voltage differential terminator for the transition to the next generation SCSI Parallel Interface (SPI-3). The low voltage differential is a requirement for the higher speeds at a reasonable cost and is the only way to have adequate skew budgets.

The automatic mode select/change feature switches the terminator between Single Ended or LVD SCSI Termination, depending on the bus mode. If the bus is in High Voltage Differential Mode, the terminator lines transition into a High Impedance state.

The UCC5672 is SPI-4, SPI-3, SPI-2, and SCSI-2 compliant. This device is offered in a 28 pin TSSOP package to minimize the footprint. The UCC5672 is also available in a 36 pin MWP package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage 6V
 Signal Line Voltage 0V to 5V
 Storage Temperature -65°C to +150°C
 Junction Temperature -55°C to +150°C
 Lead Temperature (Soldering, 10sec.) +300°C

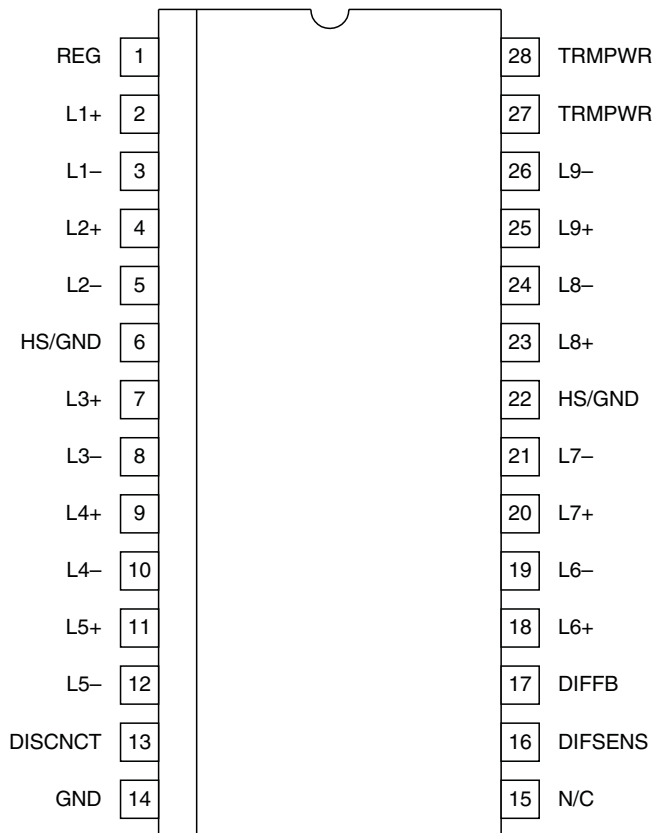
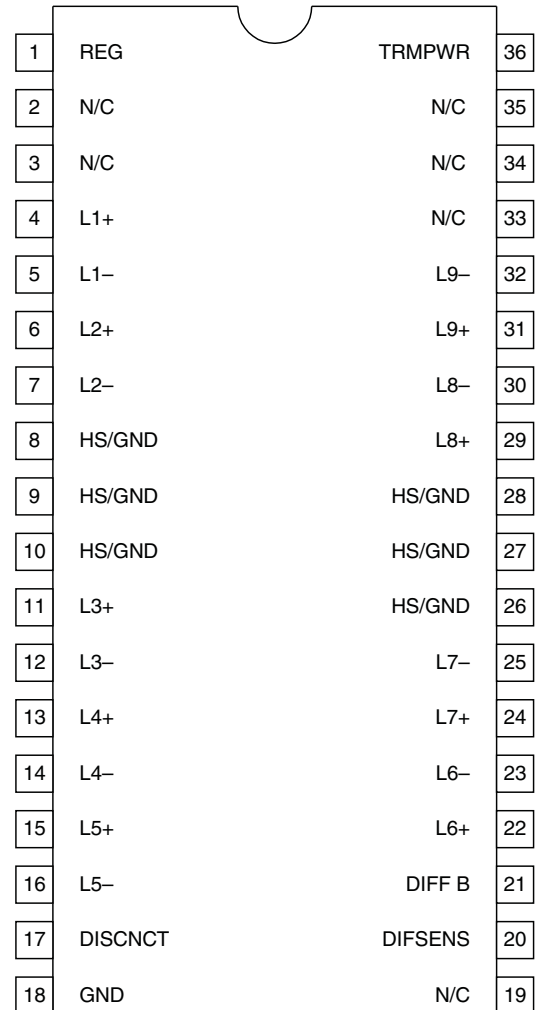
All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

TRMPWR Voltage 2.7V to 5.25V

AVAILABLE OPTIONS

T _A	Packaged Devices
0°C to 70°C	UCC5672MWP
	UCC5672PWP

CONNECTION DIAGRAM**TSSOP-28 (TOP VIEW)
PWP Package****QSOP-36 (TOP VIEW)
MWP Package**

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0^\circ\text{C}$ to 70°C ,
TRMPWR = 2.7V to 5.25V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current	LVD SCSI Mode		23	35	mA
	SE Mode		14	25	mA
	DISCNCT Mode		250	500	μA
Regulator Section					
1.25V Regulator Output Voltage	LVD SCSI Mode	1.15	1.25	1.35	V
1.25V Regulator Source Current	$V_{\text{REG}} = 0\text{V}$	-225	-420	-800	mA
1.25V Regulator Sink Current	$V_{\text{REG}} = 3.3\text{V}$	100	180	420	mA
2.7V Regulator Output Voltage	SE Mode	2.5	2.7	3.0	V
2.7V Regulator Source Current	$V_{\text{REG}} = 0\text{V}$	-225	-420	-800	mA
2.7V Regulator Sink Current	$V_{\text{REG}} = 3.3\text{V}$	100	180	420	mA
Diff Sense Driver (DIFSENS) Section					
1.3V DIFSENS Output Voltage	DIFSENS	1.2	1.3	1.4	V
1.3V DIFSENS Source Current	$V_{\text{DIFSENS}} = 0\text{V}$	-5		-15	mA
1.3V DIFSENS Sink Current	$V_{\text{DIFSENS}} = 2.75\text{V}$	50		200	μA
Differential Termination Section					
Differential Impedance		100	105	110	Ω
Common Mode Impedance	(Note 2)	110	150	165	Ω
Differential Bias Voltage		100		125	mV
Common Mode Bias		1.15	1.25	1.35	V
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended Termination Section					
Impedance	$Z = (V_{LX} - 0.2\text{V}) / I_{LX}$, (Note 3)	100	108	116	Ω
Termination Current	Signal Level 0.2V, All Lines Low	-20	-23	-25.4	mA
	Signal Level 0.5V	-17		-22.4	mA
Output Leakage				400	nA
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended GND SE Impedance	$I = 10\text{mA}$		20	60	Ω
Disconnect (DISCNCT) and Diff Buffer (DIFFB) Input Section					
DISCNCT Threshold		0.8		2.0	V
DISCNCT Input Current			-10	-30	μA
DIFFB SE to LVD SCSI Threshold		0.5		0.7	V
DIFFB LVD SCSI to HPD Threshold		1.9		2.4	V
DIFFB Input Current		-1		1	μA

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0^\circ\text{C}$ to 70°C , $\text{TRMPWR} = 2.7\text{V}$ to 5.25V .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Time Delay/Filter Section					
Mode Change Delay	A new mode change can start any time after a previous mode change has been detected. (Note4)	100	180	300	ms

Note 1: Guaranteed by design. Not 100% tested in production.

Note 2: $Z_{CM} = \frac{1.2\text{V}}{I_{(V_{CM}+0.6\text{V})} - I_{(V_{CM}-0.6\text{V})}}$; Where V_{CM} = Voltage measured with $L+$ tied to $L-$ and zero current applied;

Note 3: V_{LX} = Output voltage for each terminator minus output pin ($L1-$ through $L9-$) with each pin unloaded.
 I_{LX} = Output current for each terminator minus output pin ($L1-$ through $L9-$) with the minus output pin forced to 0.2V .

Note 4: Noise on DIFFB will not cause a false mode change. The time delay is that same for a change from any mode to any other mode. Within 300ms after power is applied the mode is defined by the voltage of DIFFB .

PIN DESCRIPTIONS

DIFFB: Input pin for the comparators that select SE, LVD SCSI, or HIPD modes of operation. This pin should be decoupled with a $0.1\mu\text{F}$ capacitor to ground and then coupled to the DIFSENS pin through a $20\text{k}\Omega$ resistor.

DIFSENS: Connects to the Diff Sense line of the SCSI bus. The bus mode is controlled by the voltage level on this pin.

DISCNCT: Input pin used to shut down the terminator if the terminator is not connected at the end of the bus. Connect this pin to ground to activate the terminator or open pin to disable the terminator.

HS/GND: Heat sink ground pins. These should be connected to large ground area PC board traces to increase the power dissipation capability.

GND: Power Supply return.

L1– thru L9–: Termination lines. These are the active lines in SE mode and are the negative lines for LVD SCSI mode. In HIPD mode, these lines are high impedance.

L1+ thru L9+: Termination lines. These lines switch to ground in SE mode and are the positive lines for LVD SCSI mode. In HIPD mode, these lines are high impedance.

REG: Regulator bypass pin, must be connected to a $4.7\mu\text{F}$ capacitor to ground.

TRMPWR: 2.7V to 5.25V power input pin. Bypass near the terminators with a $4.7\mu\text{F}$ capacitor to ground.

APPLICATION INFORMATION

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI devices are present on the bus.

The UCC5672 is used in multi-mode active termination applications, where single ended (SE) and low voltage differential (LVD) SCSI devices might coexist. The UCC5672 has both SE and LVD SCSI termination networks integrated into a single monolithic component. The correct termination network is automatically determined by the SCSI bus "DIFSENS" signal.

The SCSI bus DIFSENS signal line is used to identify which types of SCSI devices are present on the bus. On power-up, the UCC5672 DIFSENS drivers will try to de-

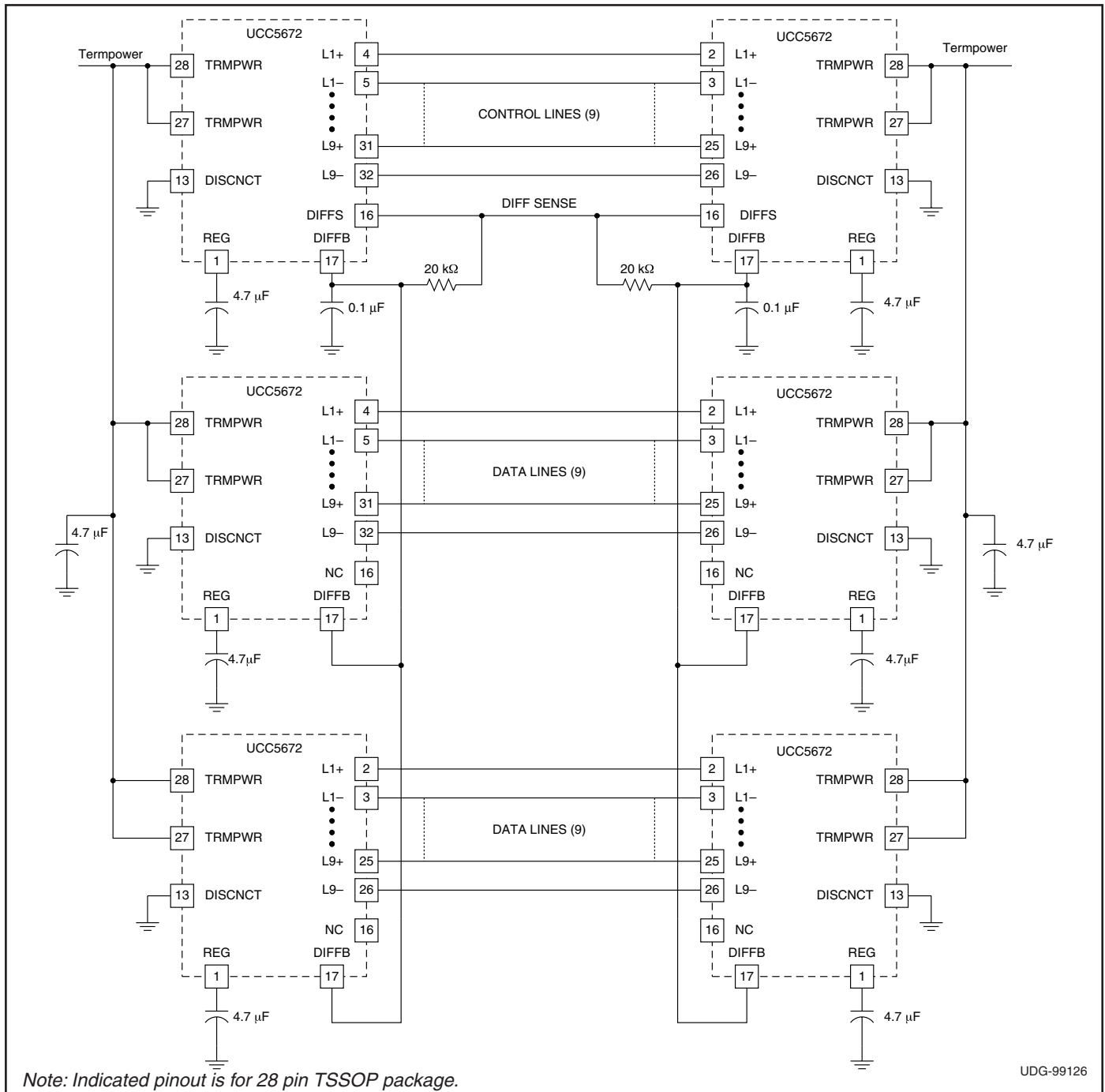
liver 1.3V to the DIFSENS line. If only LVD SCSI devices are present, the DIFSENS line will be successfully driven to 1.3V and the terminators will configure for LVD SCSI operation. If any single ended devices are present, they will present a short to ground on the DIFSENS line, signaling the UCC5672(s) to configure into the SE mode, accommodating the SE devices. Or, if any high voltage differential (HVD) SCSI devices are present, the DIFSENS line is pulled high and the terminator will enter a high impedance state, effectively disconnecting from the bus.

The DIFSENS line is monitored by each terminator through a 50Hz noise filter at the DIFFB input pin. A set of comparators detect and select the appropriate termi-

APPLICATION INFORMATION (cont.)

nation for the bus as follows. If the DIFSENS signal is below 0.5V, the termination network is set for single ended. Between 0.7V and 1.9V, the termination network switches to LVD SCSI, and above 2.4V indicates HVD SCSI, causing the terminators to disconnect from the bus. These thresholds accommodate differences in ground potential that can occur with long lines.

Three UCC5672 multi-mode parts are required at each end of the bus to terminate 27 (18 data, plus 9 control) lines. Each part includes a DIFSENS driver, but only one is necessary to drive the line. The DIFFB inputs on all three parts are connected together, allowing them to share the same 50Hz noise filter. This multi-mode terminator operates in full specification down to 2.7V TRMPWR voltage. This accommodates 3.3V systems,



UDG-99126

Figure 1. Application diagram.

APPLICATION INFORMATION (cont.)

with allowance for the 3.3V supply tolerance (+/- 10%), a unidirectional fusing device and cable drop. In 3.3V TRMPWR systems, the UCC3918 is recommended in place of the fuse and diode. The UCC3918's lower voltage drop allows additional margin over the fuse and diode, for the far end terminator.

Layout is critical for Ultra2, Ultra3/Ultra160 and Ultra320 systems. The SPI-2 standard for capacitance loading is 10pF maximum from each positive and negative signal line to ground, and a maximum of 5pF between the positive and negative signal lines of each pair is allowed. These maximum capacitances apply to differential bus termination circuitry that is not part of a SCSI device, (e.g. a cable terminator). If the termination circuitry is included as part of a SCSI device, (e.g., a host adaptor, disk or tape drive), then the corresponding requirements are 30pF maximum from each positive and negative signal line to ground and 15pF maximum between the positive and negative signal lines of each pair.

The SPI-2 standard for capacitance balance of each pair and balance between pairs is more stringent. The standard is 0.75pF maximum difference from the positive and negative signal lines of each pair to ground. An additional requirement is a maximum difference of 2pF when comparing pair to pair. These requirements apply to differential bus termination circuitry that is not part of a SCSI device. If the termination circuitry is included as part of a device, then the corresponding balance requirements are 2.25pF maximum difference within a pair, and 3pF from pair to pair.

Feed-throughs, through-hole connections, and etch lengths need to be carefully balanced. Standard multi-layer power and ground plane spacing add about

1pF to each plane. Each feed-through will add about 2.5pF to 3.5pF. Enlarging the clearance holes on both power and ground planes will reduce the capacitance. Similarly, opening up the power and ground planes under the connector will reduce the capacitance for through-hole connector applications. Capacitance will also be affected by components, in close proximity, above and below the circuit board.

Unitrode multi-mode terminators are designed with very tight balance, typically 0.1pF between pins in a pair and 0.3pF between pairs. At each L+ pin, a ground driver drives the pin to ground, while in single ended mode. The ground driver is specially designed to not effect the capacitive balance of the bus when the device is in LVD SCSI or disconnect mode.

Multi-layer boards need to adhere to the 120Ω impedance standard, including the connectors and feed-throughs. This is normally done on the outer layers with 4 mil etch and 4 mil spacing between runs within a pair, and a minimum of 8 mil spacing to the adjacent pairs to reduce crosstalk. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50Ω rather than 120Ω differential systems. Careful consideration must be given to the issue of heat management. A multi-mode terminator, operating in SE mode, will dissipate as much as 130mW of instantaneous power per active line with TRMPWR = 5.25V. The UCC5672 is offered in a 28 pin TSSOP. This package includes two heat sink ground pins. These heat sink/ground pins are directly connected to the die mount paddle under the die and conduct heat from the die to reduce the junction temperature. Both of the HS/GND pins need to be connected to etch area or four feed-through per pin connecting to the ground plane layer on a multi-layer board.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UCC5672MWP	ACTIVE	SSOP	DCE	36	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5672MWP	Samples
UCC5672MWPG4	ACTIVE	SSOP	DCE	36	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5672MWP	Samples
UCC5672PWP	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5672PWP	Samples
UCC5672PWPG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5672PWP	Samples
UCC5672PWPTR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5672PWP	Samples
UCC5672PWPTRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5672PWP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

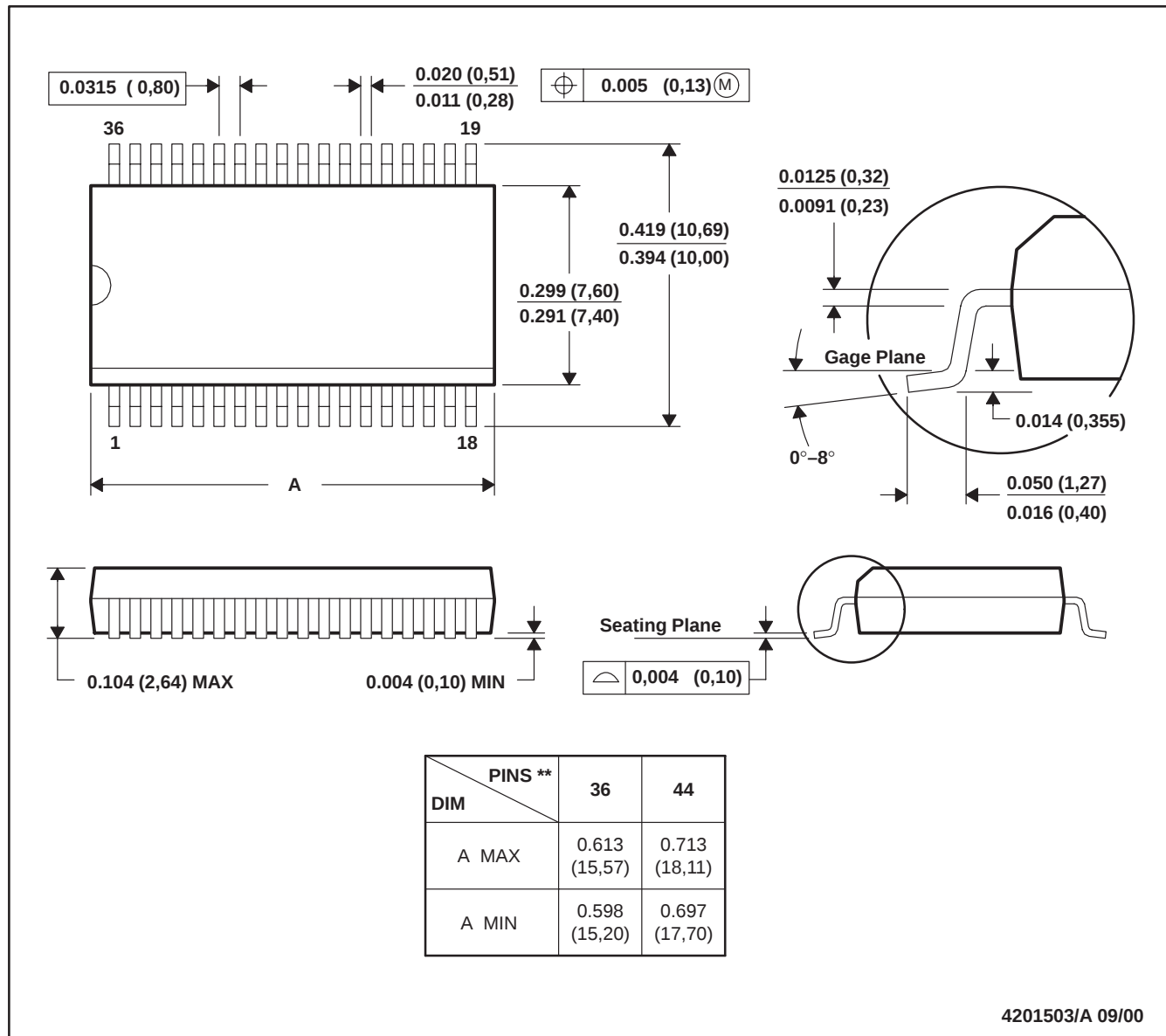
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DCE (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

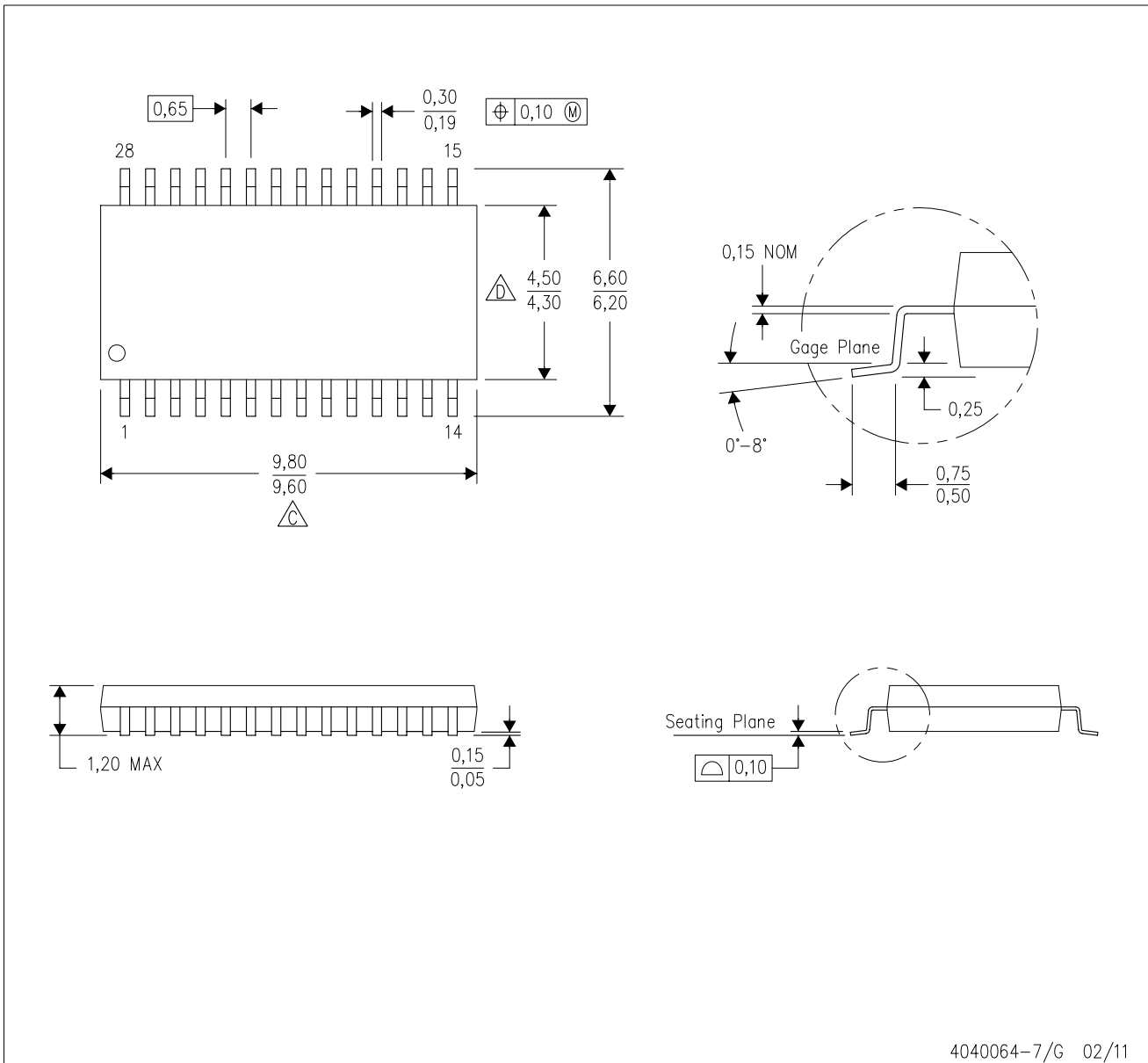
36 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



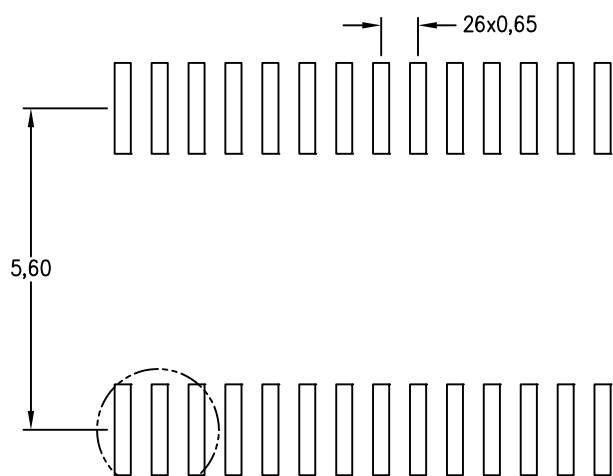
4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

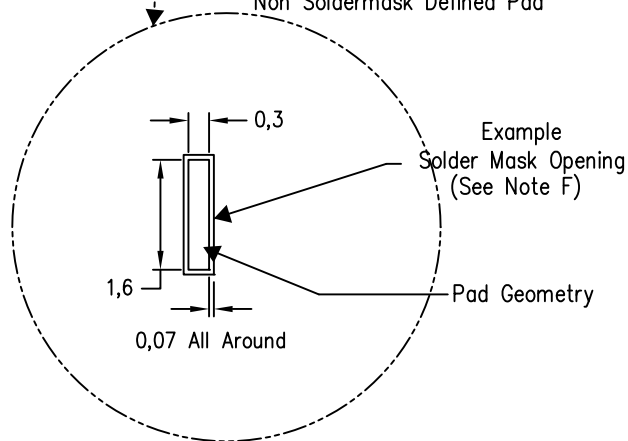
PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

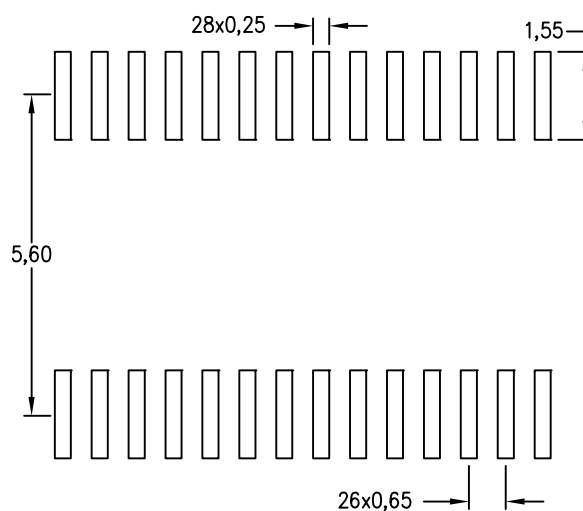
Example Board Layout



Example
Non Soldermask Defined Pad



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



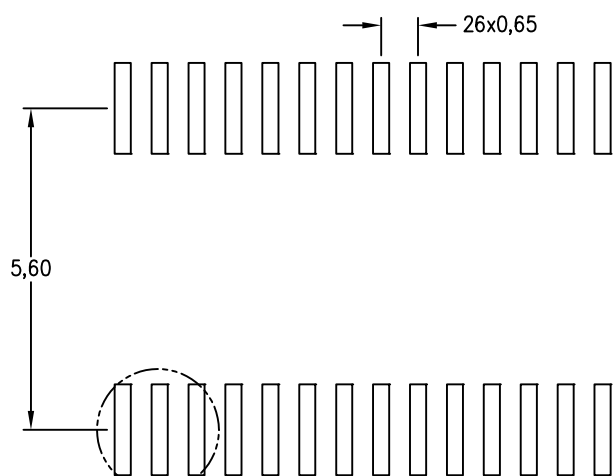
4211284-6/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

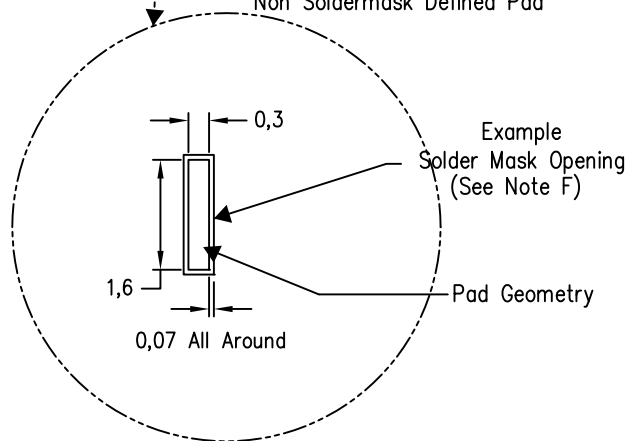
PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

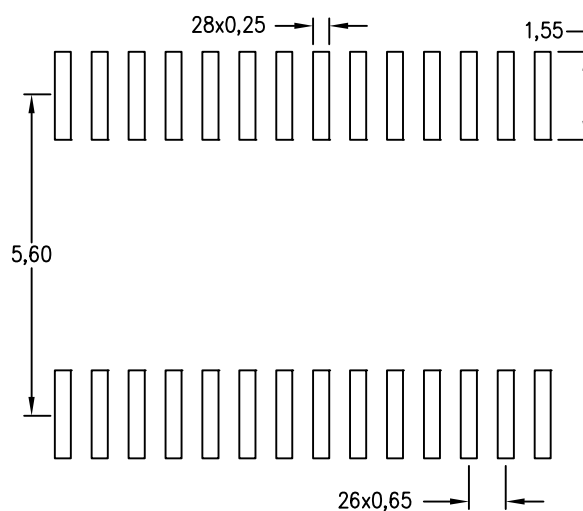
Example Board Layout



Example
Non Soldermask Defined Pad



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



4211284-6/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com