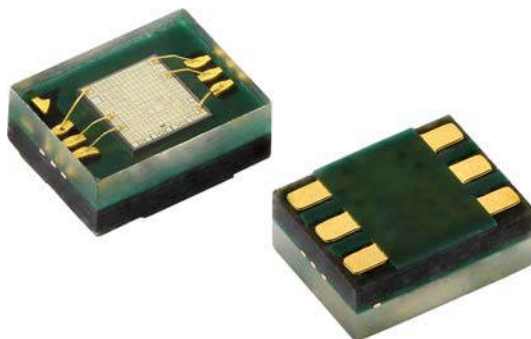


## UV Light Sensor with I<sup>2</sup>C Interface



### DESCRIPTION

VEML6070 is an advanced ultraviolet (UV) light sensor with I<sup>2</sup>C protocol interface and designed by the CMOS process. It is easily operated via a simple I<sup>2</sup>C command. The active acknowledge (ACK) feature with threshold windows setting allows the UV sensor to send out a UVI alert message. Under a strong solar UVI condition, the smart ACK signal can be easily implemented by the software programming.

VEML6070 incorporates a photodiode, amplifiers, and analog / digital circuits into a single chip. VEML6070's adoption of Filtron™ UV technology provides the best spectral sensitivity to cover UV spectrum sensing. It has an excellent temperature compensation and a robust refresh rate setting that does not use an external RC low pass filter. VEML6070 has linear sensitivity to solar UV light and is easily adjusted by an external resistor. Software shutdown mode is provided, which reduces power consumption to be less than 1  $\mu$ A. VEML6070's operating voltage ranges from 2.7 V to 5.5 V.

### FEATURES

- Package type: surface mount
- Dimensions (L x W x H in mm): 2.35 x 1.8 x 1.0
- Integrated modules: ultraviolet sensor (UV), and signal conditioning IC
- Converts solar UV light intensity to digital data
- Excellent UV sensitivity and linearity via Filtron™ technology
- Excellent performance of UV radiation measurement under long time solar UV exposure
- Excellent temperature compensation
- High dynamic detection resolution
- Standard I<sup>2</sup>C protocol interface
- Support acknowledge feature (ACK)
- Immunity on fluorescent light flicker software shutdown mode control
- Package: OPLGA
- Temperature compensation: -40 °C to +85 °C
- Floor life: 168 h, MSL 3, according to J-STD-020
- Output type: I<sup>2</sup>C bus
- Operation voltage: 2.7 V to 5.5 V
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



### APPLICATIONS

- Solar UV indicator
- Cosmetic / outdoor sport handheld product
- Consumer products

### PRODUCT SUMMARY

PART NUMBER	OPERATING VOLTAGE RANGE (V)	I <sup>2</sup> C BUS VOLTAGE RANGE (V)	PEAK SENSITIVITY (nm)	RANGE OF SPECTRAL BANDWIDTH $\lambda_{0.5}$ (nm)	OUTPUT CODE
VEML6070	2.7 to 5.5	1.7 to 5.5	355	$\pm 20$	16 bit, I <sup>2</sup> C

#### Note

(1) Adjustable through I<sup>2</sup>C interface

### ORDERING INFORMATION

ORDERING CODE	PACKAGING	VOLUME (1)	REMARKS
VEML6070	Tape and reel	MOQ: 2500 pcs	2.35 mm x 1.8 mm x 1.0 mm

#### Note

(1) MOQ: minimum order quantity

### ABSOLUTE MAXIMUM RATINGS (T<sub>amb</sub> = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	MAX.	UNIT
Supply voltage		V <sub>DD</sub>	0	6.0	V

**ABSOLUTE MAXIMUM RATINGS** ( $T_{amb} = 25^{\circ}\text{C}$ , unless otherwise specified)

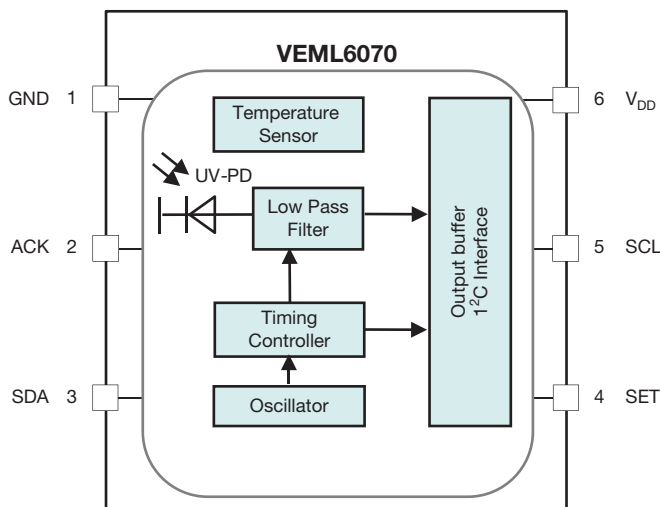
PARAMETER	TEST CONDITION	SYMBOL	MIN.	MAX.	UNIT
Operation temperature range		$T_{amb}$	-40	+85	$^{\circ}\text{C}$

**RECOMMENDED OPERATING CONDITIONS** ( $T_{amb} = 25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	MAX.	UNIT
Supply voltage		$V_{DD}$	2.7	5.5	V
Operation temperature range		$T_{amb}$	-40	+85	$^{\circ}\text{C}$
I <sup>2</sup> C bus operating frequency		$f_{(I^2CCLK)}$	10	400	kHz

**PIN DESCRIPTIONS**

PIN ASSIGNMENT	SYMBOL	TYPE	FUNCTION
1	GND	I	Power supply ground, all voltage are reference to GND
2	ACK	O (open drain)	Acknowledge pin
3	SDA	I / O (open drain)	I <sup>2</sup> C digital serial data output to the host
4	SET		Light reading adjustment, connect a resistor to GND
5	SCL	I	I <sup>2</sup> C digital serial clock input from the host
6	$V_{DD}$	I	Supply voltage

**BLOCK DIAGRAM**

**BASIC CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply operation voltage		$V_{DD}$	2.7		5.5	V
Supply current	$R_{SET} = 270\text{ k}\Omega$ (1)(2)	$I_{DD}$		100	250	$\mu\text{A}$
I <sup>2</sup> C signal input	Logic high	$V_{IH}$	1.5		$V_{DD}$	V
	Logic low	$V_{IL}$			0.8	
Peak sensitivity wavelength		$\lambda_p$		355		nm
Range of spectral sensitivity		$\lambda$	280		400	nm
Dark offset	$R_{SET} = 200\text{ k}\Omega$ , $I_T = 1\text{ T}$ (1)		0	1	5	steps
Output offset	$R_{SET} = 200\text{ k}\Omega$ , $I_T = 1\text{ T}$ (1)(3)			2		steps
Shutdown current	Light condition = dark (1)	$I_{DD}$		1	15	$\mu\text{A}$

**Notes**

- (1) Test condition:  $V_{DD} = 3.3\text{ V}$ , temperature:  $25^{\circ}\text{C}$
- (2) Light source: solar light source
- (3) Ambient light intensity =  $500\text{ lx}$

<b>I<sup>2</sup>C TIMING CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)						
PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
Clock frequency	$f_{(SMBCLK)}$	10	100	10	400	kHz
Bus free time between start and stop condition	$t_{(BUF)}$	4.7		1.3		$\mu\text{s}$
Hold time after (repeated) start condition; after this period, the first clock is generated	$t_{(HDSTA)}$	4.0		0.6		$\mu\text{s}$
Repeated start condition setup time	$t_{(SUSTA)}$	4.7		0.6		$\mu\text{s}$
Stop condition setup time	$t_{(SUSTO)}$	4.0		0.6		$\mu\text{s}$
Data hold time	$t_{(HDDAT)}$		3450		900	ns
Data setup time	$t_{(SUDAT)}$	250		100		ns
I <sup>2</sup> C clock (SCK) low period	$t_{(LOW)}$	4.7		1.3		$\mu\text{s}$
I <sup>2</sup> C clock (SCK) high period	$t_{(HIGH)}$	4.0		0.6		$\mu\text{s}$
Detect clock / data low timeout	$t_{(TIMEOUT)}$	25	35			ms
Clock / data fall time	$t_{(F)}$		300		300	ns
Clock / data rise time	$t_{(R)}$		1000		300	ns

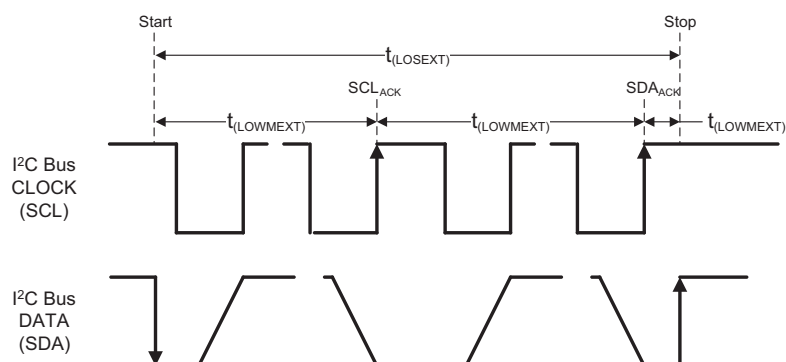
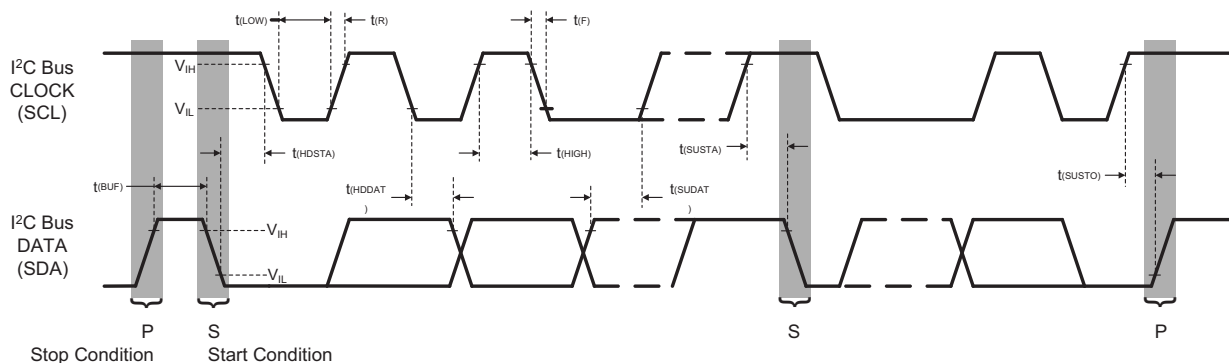


Fig. 1 - I<sup>2</sup>C Timing Diagram

## PARAMETER TIMING INFORMATION

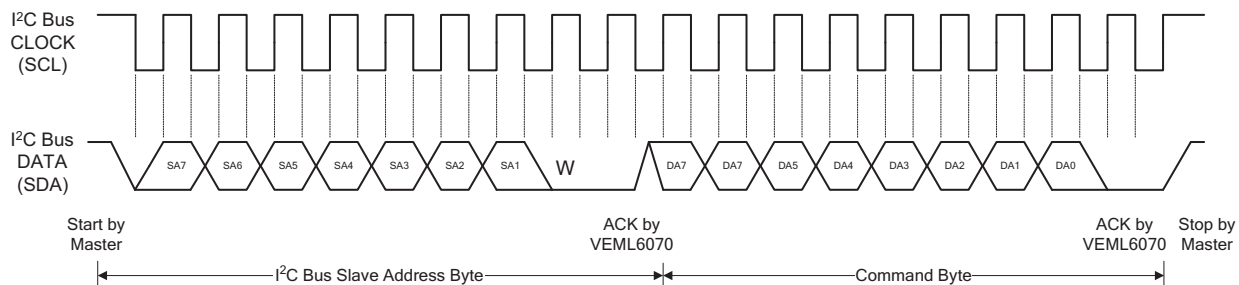


Fig. 2 - Timing for Send Byte Command Format

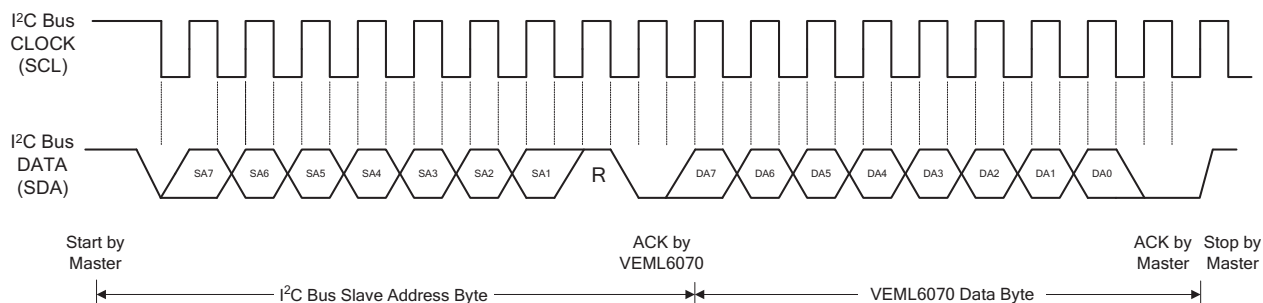


Fig. 3 - I<sup>2</sup>C Timing for Receive Byte Command Format

## TYPICAL PERFORMANCE CHARACTERISTICS ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

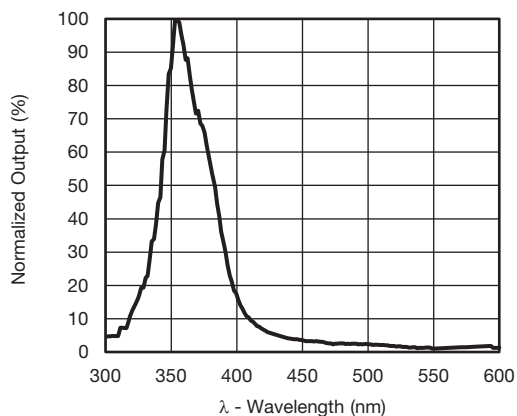


Fig. 4 - Normalized Spectral Response

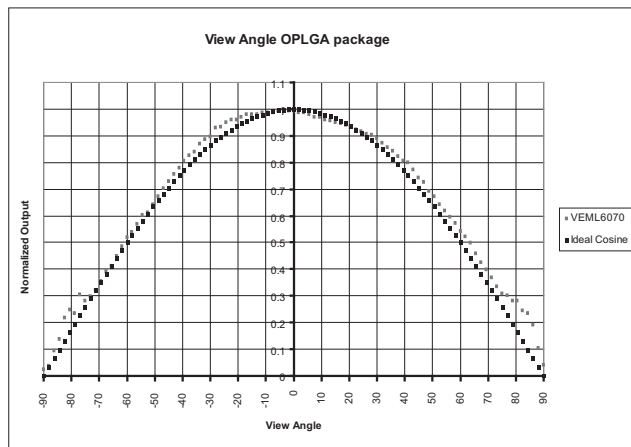


Fig. 5 - Normalized Output vs. View Angle

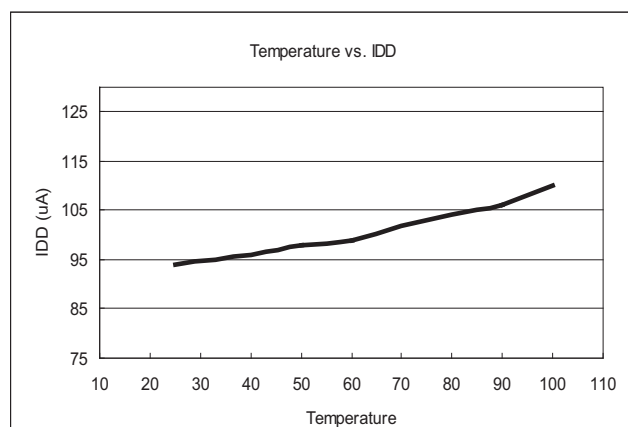
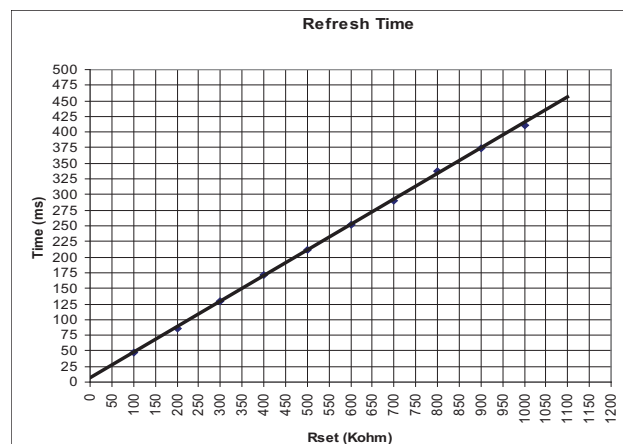

Fig. 6 -  $I_{DD}$  vs. Temperature


Fig. 7 - Refresh Time

## APPLICATION INFORMATION

### Pin Connection with the Host

VEML6070 is a cost effective solution for ultraviolet light sensing with I<sup>2</sup>C interface. The standard serial digital interface easily accesses “UV light intensity” digital data.

The additional capacitor near the V<sub>DD</sub> pin is used for power supply noise rejection. For the I<sup>2</sup>C bus design, the pull-up voltage refers to the I/O of the baseband due to the “open drain” design. The pull-up resistors for the I<sup>2</sup>C bus design are recommended to be 2.2 kΩ. The circuit diagram as an example is shown in figure 8.

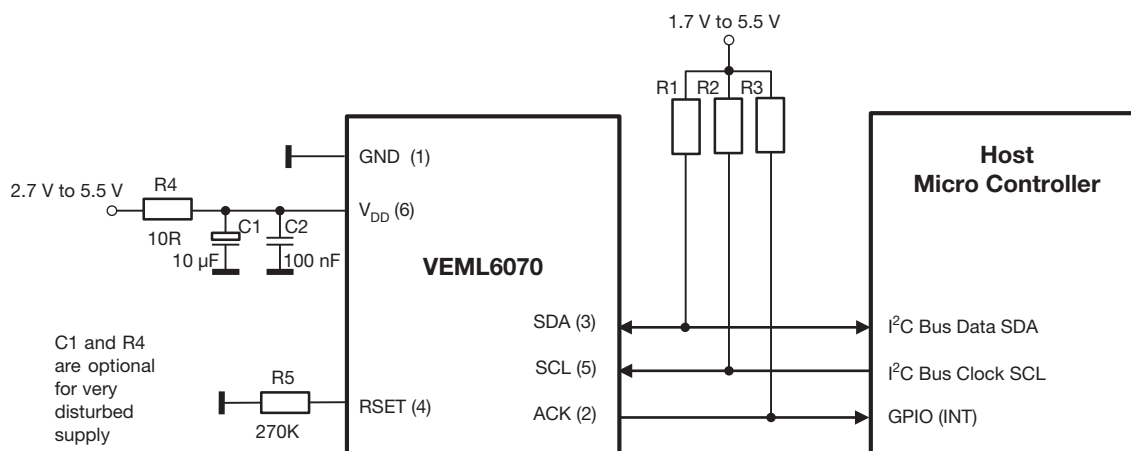


Fig. 8 - Hardware Pin Connection Diagram

## Digital Interface

VEML6070 contains a 8-bit command register written via the I<sup>2</sup>C bus. All operations can be controlled by the command register. The simple command structure enables users to easily program the operation setting and latch the light data from VEML6070. In figure 9, VEML6070 I<sup>2</sup>C command format description for reading and writing operation between the host and VEML6070 are shown. The white sections indicate host activity and the gray sections indicate VEML6070's acknowledgement of the host access activity.

Receive byte → read data from UVS

S	Slave address	Rd	A	Light data (1 byte)	A	P
---	---------------	----	---	---------------------	---	---

Send byte → write command to UVS

S	Slave address	Wr	A	Command (1 byte)	A	P
---	---------------	----	---	------------------	---	---

S = start condition

P = stop condition

A = acknowledge

Shaded area = VEML6070 acknowledge

Fig. 9 - VEML6070 Command Protocol

## Slave Address and Function Description

VEML6070 has a fixed group of slave addresses(8 bits) that ranges from 0x70 to 0x73 (0x72 is reserved).

For write command setting, the slave address should use 0x70. For read command setting, the host uses addresses 0x71 and 0x73. For data reading, the host reads the data from the 0x73 address first and then reads the 0x71 address data to complete all data collection. A description for each slave address operation is shown in table 1.

TABLE 1 - VEML6070 SLAVE ADDRESS AND FUNCTION DESCRIPTION	
SLAVE ADDRESS	OPERATION
0x70	Write command to VEML6070
0x72	Reserved
0x71	Read LSB 8 bits of VEML6070 ultraviolet light data
0x73	Read MSB 8 bits of VEML6070 ultraviolet light data

## Command Register Format

VEML6070 provides a command to set device operations and sensitivity adjustment. This command is 8-bit long and includes 4 parameter groups for programming. The command format descriptions and register setting explanations are shown in tables 2 and 3.

TABLE 2 - COMMAND REGISTER BITS DESCRIPTION							
COMMAND FORMAT							
Reserved		ACK	ACK_THD	IT		Reserved	SD
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	ACK	THD	IT1	IT0	1	SD
DESCRIPTION							
Reserved		Reserved					
ACK		Acknowledge activity setting					
ACK_THD		Acknowledge threshold window setting for byte mode usage					
IT		Integration time setting					
SD		Shutdown mode setting					

**TABLE 3 - REGISTER TABLE SETTING**

BITS SETTING	DESCRIPTION		BITS SETTING	DESCRIPTION
Reserved	Set initial value to (0 : 0)		(IT1 : ITO) <sup>(1)</sup>	(0 : 0) = ½T (0 : 1) = 1T (1 : 0) = 2T (1 : 1) = 4T
ACK	0 = disable 1 = enable		Reserved	Set initial value to 1
ACK_THD	0 = 102 steps 1 = 145 steps		SD	0 = disable 1 = enable

**Note**

<sup>(1)</sup> Please refer to table 5, "Example of Refresh Time and R<sub>SET</sub> Value Relation"

**Data Access**

VEML6070 has 16-bit resolution to give high resolution for light intensity sensing. Examples of the application setting are shown in table 4.

**TABLE 4 - DATA ACCESS DESCRIPTION**

	VEML6070 16-BIT DATA BUFFER															
Data bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sequence 1																
Sequence 2																

**Notes**

- Slave addresses (8 bits) for data read: 0x71 and 0x73
- Data reading sequence for the host:
  - Set read command to 0x73, read MSB 8 bits of 16 bits light data (sequence 1)
  - Set read command to 0x71, read LSB 8 bits of 16 bits light data for completing data structure (sequence 2)

**Initialization**

VEML6070 needs to be initialized while the system's power is on. The initialization includes two major steps: (1) clear ACK state of UVS and (2) fill the initial value, 06 (HEX), into the 0x70 addresses. After the initialization is completed, VEML6070 can be programmable for operation by write command setting from the host. VEML6070 initialization is recommended to be completed within 150 ms.

**Acknowledge Activity**

VEML6070 provides a function for sending an acknowledge signal (ACK) to the host when the value of sensed UV light is over the programmed threshold (ACK\_THD) value. The purpose of the ACK signal is similar to the interrupt feature which informs the host once the sensed data level goes beyond the interrupt threshold setting. VEML6070 has two ACK threshold values, 102 steps and 145 steps.

There are two methods of driving acknowledge condition and read / write command to VEML6070:

- If the host implements the INT function, it performs a modified received byte operation to disengage VEML6070's acknowledge signal and acknowledge alert response address (ARA), 0x18 (Hex). A command format for responses to an ARA is shown in figure 10.

S	ARA (0x18)	Rd	A	UVS Slave Address	A	P
---	------------	----	---	-------------------	---	---

Fig. 10 - Command Format for Responds to an ARA

- If the host does not implement this feature, it should periodically access the ARA or read ARA before setting each read / write command.

The behavior of an ACK signal is similar to the INT definition in I<sup>2</sup>C specification. For the hardware circuit design, this pin connects to an INT pin or GPIO pin of the MCU. The threshold ACK\_THD definition is based on the sensitivity setting of VEML6070.



The ACK or UVI interrupt function allows the UVI sensing system to perform data pooling based on the interrupt event. The system sensor manager does not need to do continual data pooling and this significantly reduced the MCU loading. The ACK signal can also be used as a trigger event for popping up a warning UVI message.

#### Refresh Time Determination

VEML6070's refresh time can be determined by the  $R_{SET}$  value. Cooperating with the command register setting, the designer has a flexible way of defining the timing for light data collection. The default refresh time is 1T, (IT1 : IT0) = (0 : 1). If the  $R_{SET}$  value is changed, the default timing changes and the other parts in the register table also change by comparing itself with the default timing (refer to figure 7).

Table 5 is an example of two  $R_{SET}$  resistors that show the timing table that the system designer can use a flexible way to determine the desired refresh time.

TABLE 5 - EXAMPLE OF REFRESH TIME AND $R_{SET}$ VALUE RELATION			
REGISTER	SETTING	REFRESH TIME	
		$R_{SET} = 270\text{ k}\Omega$	$R_{SET} = 540\text{ k}\Omega$
(IT1 : IT0)	(0 : 0) = $\frac{1}{2}T$	90 ms	180 ms
	(0 : 1) = 1T	180 ms	360 ms
	(1 : 0) = 2T	360 ms	720 ms
	(1 : 1) = 4T	720 ms	1440 ms

If VEML6070's refresh time reaches 360 ms, there are two ways to obtain the refresh time:

3. If  $R_{SET}$  uses 270 k $\Omega$ , the "IT" register value should set to (1 : 0), 2T.
4. If  $R_{SET}$  uses 540 k $\Omega$ , the "IT" register value should set to (0 : 1), 1T.

The register operation is independent to the setting of other command registers. The designer can decide the refresh timing range requirement first, then choose an appropriate  $R_{SET}$  value for the timing range, and then write the correct value for the system application via I<sup>2</sup>C protocol.



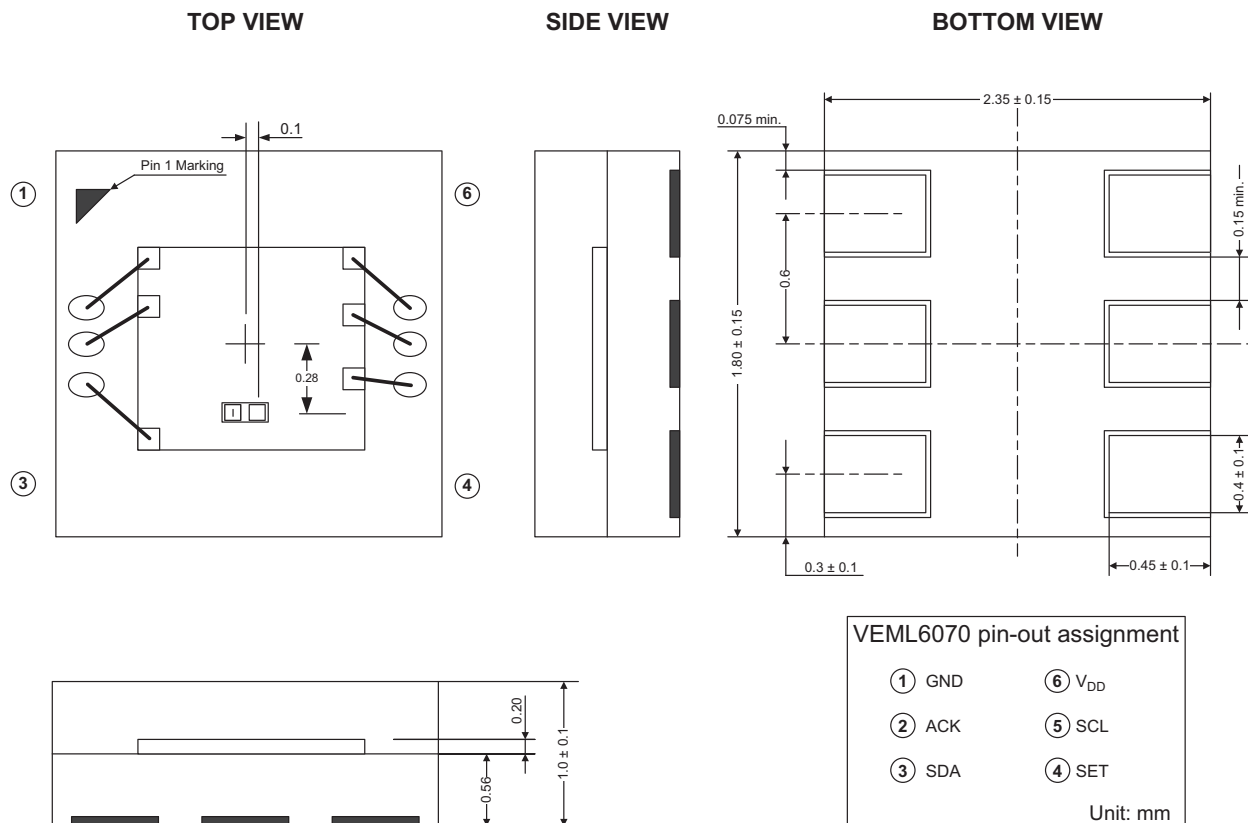
**PACKAGE INFORMATION** in millimeters


Fig. 11 - VEML6070 A3OP Package Dimensions

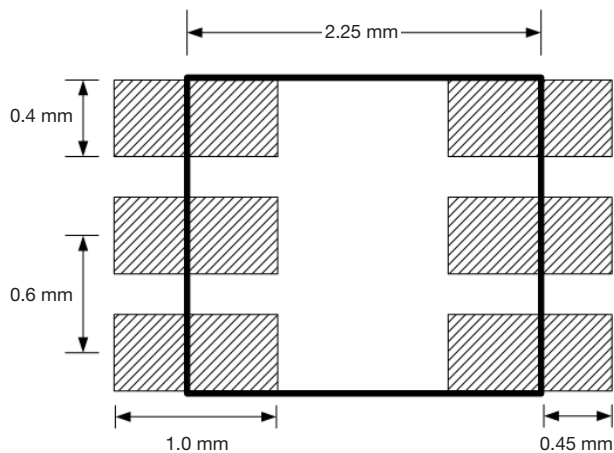
**LAYOUT NOTICE**


Fig. 12 - VEML6070 OPLGA PCB Layout Footprint

## APPLICATION CIRCUIT BLOCK REFERENCE

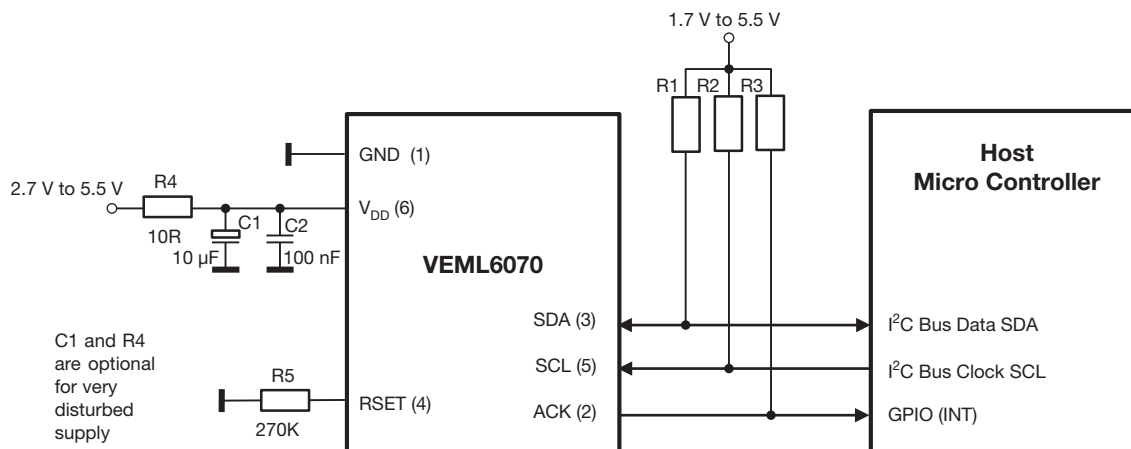


Fig. 13 - VEML6070 Application Circuit

### Notes

- $V_{DD}$  range: 2.7 V to 5.5 V
- The pull-up voltage for I<sup>2</sup>C bus is referring to the I/O specification of baseband

RECOMMENDED STORAGE AND REBAKING CONDITIONS				
PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Storage temperature		5	50	°C
Relative humidity			60	%
Open time	Rebaking process should be done when aluminized envelope reopened			
Total time	From the date code on the aluminized envelope (unopened)		6	months
Rebaking	Tape and reel: 60 °C		22	h
	Tube: 60 °C		22	h

## RECOMMENDED INFRARED REFLOW

Soldering conditions are based on J-STD-020 C definition.

1. After opening the tape and reel, IR reflow process should be done
2. IR reflow profile conditions

IR REFLOW PROFILE CONDITION			
PARAMETER	CONDITIONS	TEMPERATURE	TIME
Peak temperature		255 °C + 0 °C / - 5 °C (max.: 260 °C)	10 s
Preheat temperature range and timing		150 °C to 200 °C	60 s to 180 s
Timing within 5 °C to peak temperature			10 s to 30 s
Timing maintained above temperature / time		217 °C	60 s to 150 s
Timing from 25 °C to peak temperature			8 min (max.)
Ramp-up rate		3 °C/s (max.)	
Ramp-down rate		6 °C/s (max.)	

3. Recommend Normal Solder Reflow is 235 °C to 255 °C

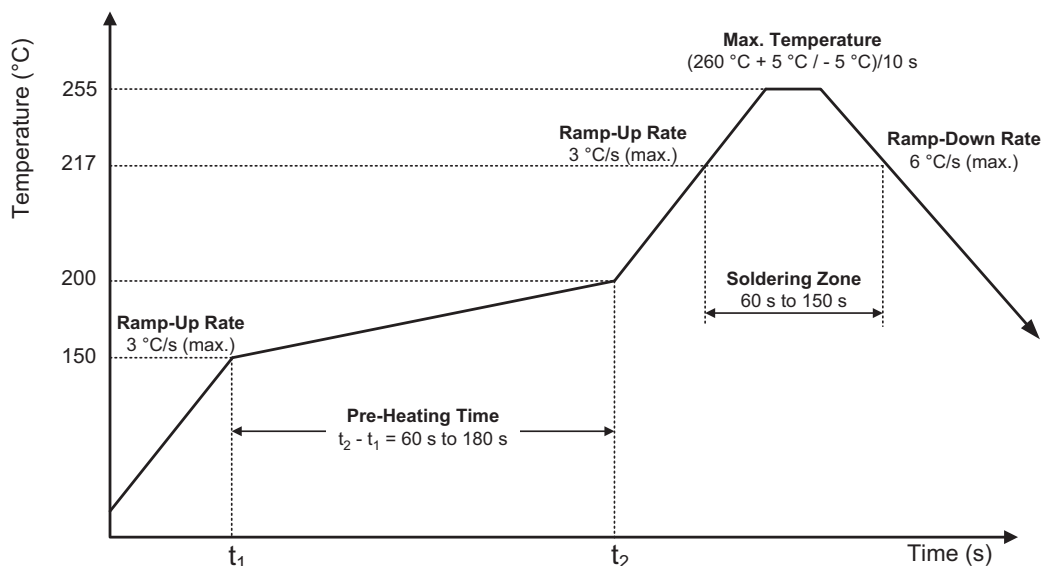


Fig. 14 - VEML6070 A3OP Solder Reflow Profile Chart

## RECOMMENDED IRON TIP SOLDERING CONDITION AND WARNING HANDLING

1. Solder the device with the following conditions:
  - 1.1. Soldering temperature: 400 °C (max.)
  - 1.2. Soldering time: 3 s (max.)
2. If the temperature of the method portion rises in addition to the residual stress between the leads, the possibility that an open or short circuit occurs due to the deformation or destruction of the resin increases.
3. The following methods: VPS and wave soldering, have not been suggested for the component assembly.
4. Cleaning method conditions:
  - 4.1. Solvent: methyl alcohol, ethyl alcohol, isopropyl alcohol
  - 4.2. Solvent temperature < 45 °C (max.)
  - 4.3. Time: 3 min (min.)



**TAPE PACKAGING INFORMATION** in millimeters

**DIMENSION OF CARRIER TAPE**

SIDE VIEW

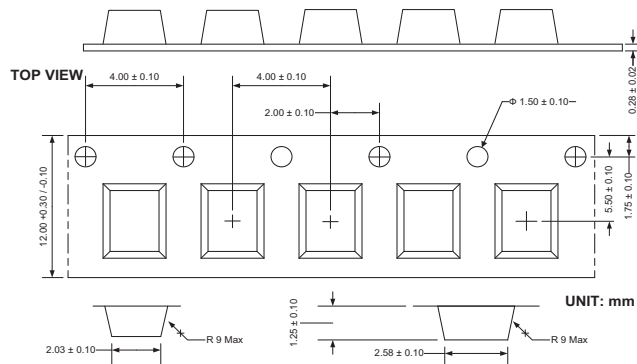


Fig. 15 - VEML6070 A3OP Package Carrier Tape

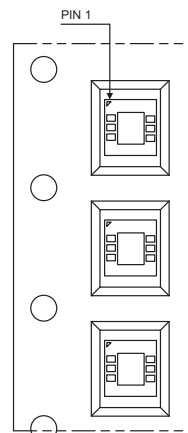


Fig. 16 - Taping Direction

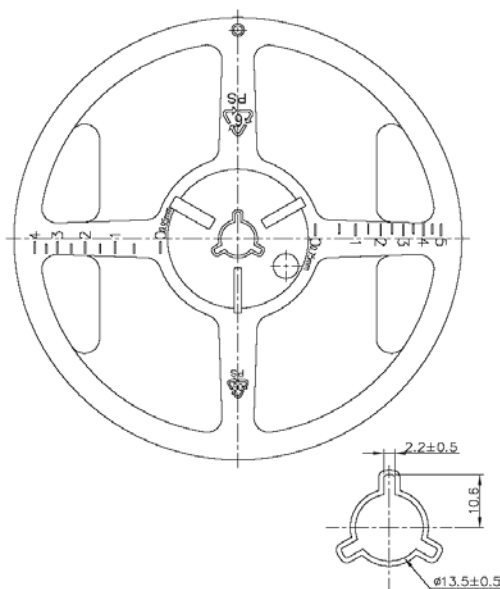


Fig. 17 - Reel Dimension

