260 Pin BGA
Commercial Temp
Industrial Temp

# 72Mb SigmaQuad-IIIe™ Burst of 2 ECCRAM™

Up to 725 MHz
1.35V $V_{DD}$
1.2V or 1.35V or 1.5V $V_{DDQ}$

Not Recommended for New Design – Discontinued Product

## Features

- For use with GSI SRAM Port IP
- 2Mb x 36 and 4Mb x 18 organizations available
- 725 MHz maximum operating frequency
- 1.45 BT/s peak transaction rate (in billions per second)
- 104 Gb/s peak data bandwidth (in x36 devices)
- Separate I/O DDR Data Buses
- Non-multiplexed DDR Address Bus
- Two operations - Read and Write - per clock cycle
- Burst of 2 Read and Write operations
- 3 cycle Read Latency
- On-chip ECC with virtually zero SER
- 1.35V core voltage
- 1.2V or 1.35V or 1.5V I/O interface (HSTL or SSTL)
- Configurable ODT (on-die termination)
- ZQ pin for programmable driver impedance
- ZT pin for programmable ODT impedance
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 260 pin, 14 mm x 22 mm, 1 mm ball pitch BGA package
  - –K: 5/6 RoHS-compliant package

## SigmaQuad-IIIe™ Family Overview

SigmaQuad-IIIe ECCRAMs are the Separate I/O half of the SigmaQuad-IIIe/SigmaDDR-IIIe family of high performance ECCRAMs. Although very similar to GSI's second generation of networking SRAMs (the SigmaQuad-II/SigmaDDR-II family), these third generation devices offer several new features that help enable significantly higher performance.

## Clocking and Addressing Schemes

The GS8673EQ18/36BK SigmaQuad-IIIe ECCRAMs are synchronous devices. They employ three pairs of positive and negative input clocks; one pair of master clocks, CK and $\overline{CK}$, and two pairs of write data clocks, KD[1:0] and $\overline{KD}$[1:0]. All six input clocks are single-ended; that is, each is received by a dedicated input buffer.

CK and $\overline{CK}$ are used to latch address and control inputs, and to control all output timing. KD[1:0] and $\overline{KD}$[1:0] are used solely to latch data inputs.

Each internal read and write operation in a SigmaQuad-IIIe B2 ECCRAM is two times wider than the device I/O bus. An input data bus de-multiplexer is used to accumulate incoming data before it is simultaneously written to the memory array. An output data multiplexer is used to capture the data produced from a single memory array read and then route it to the appropriate output drivers as needed. Therefore, the address field of a SigmaQuad-IIIe B2 ECCRAM is always one address pin less than the advertised index depth (e.g. the 4M x 18 has 2M addressable index).

## On-Chip ECC

GSI's ECCRAMs implement an ECC algorithm that detects and corrects all single-bit memory errors, including those induced by SER events such as cosmic rays, alpha particles, etc. The resulting Soft Error Rate of these devices is anticipated to be <0.002 FITs/Mb — a 5-order-of-magnitude improvement over comparable SRAMs with no on-chip ECC, which typically have an SER of 200 FITs/Mb or more.

All quoted SER values are at sea level in New York City.

### Parameter Synopsis

| Speed Grade | Max Operating Frequency | Read Latency | $V_{DD}$ |
|---|---|---|---|
| -725S | 725 MHz | 3 cycles | 1.3V to 1.4V |
| -625S | 625 MHz | 3 cycles | 1.3V to 1.4V |
| -550S | 550 MHz | 3 cycles | 1.3V to 1.4V |

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## 4M x 18 (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | MCL | MCH (CFG) | MCL | ZQ | PZT1 | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ |
| **B** | $V_{SS}$ | $NU_O$ | $V_{SS}$ | $NU_I$ | MVQ | MCL (B4M) | NC (RSVD) | MCH (SIOM) | PZT0 | D0 | $V_{SS}$ | Q0 | $V_{SS}$ |
| **C** | Q17 | $V_{DDQ}$ | D17 | $V_{DDQ}$ | $V_{SS}$ | SA | $V_{DD}$ | SA | $V_{SS}$ | $V_{DDQ}$ | $NU_I$ | $V_{DDQ}$ | $NU_O$ |
| **D** | $V_{SS}$ | $NU_O$ | $V_{SS}$ | $NU_I$ | SA | $V_{DDQ}$ | NC (288 Mb) | $V_{DDQ}$ | NC (144 Mb) | D1 | $V_{SS}$ | Q1 | $V_{SS}$ |
| **E** | Q16 | $V_{DDQ}$ | D16 | $V_{DD}$ | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | $V_{DD}$ | $NU_I$ | $V_{DDQ}$ | $NU_O$ |
| **F** | $V_{SS}$ | $NU_O$ | $V_{SS}$ | $NU_I$ | SA | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | SA | D2 | $V_{SS}$ | Q2 | $V_{SS}$ |
| **G** | Q15 | $NU_O$ | D15 | $NU_I$ | $V_{SS}$ | SA | MZT1 | SA | $V_{SS}$ | D3 | $NU_I$ | Q3 | $NU_O$ |
| **H** | Q14 | $V_{DDQ}$ | D14 | $V_{DDQ}$ | SA | $V_{DDQ}$ | $\overline{W}$ | $V_{DDQ}$ | SA | $V_{DDQ}$ | $NU_I$ | $V_{DDQ}$ | $NU_O$ |
| **J** | $V_{SS}$ | $NU_O$ | $V_{SS}$ | $NU_I$ | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | D4 | $V_{SS}$ | Q4 | $V_{SS}$ |
| **K** | CQ1 | $V_{DDQ}$ | $V_{REF}$ | $V_{DD}$ | KD1 | $V_{DD}$ | CK | $V_{DD}$ | KD0 | $V_{DD}$ | $V_{REF}$ | $V_{DDQ}$ | CQ0 |
| **L** | $\overline{CQ1}$ | $V_{SS}$ | QVLD1 | $V_{ss}$ | $\overline{KD1}$ | $V_{DDQ}$ | $\overline{CK}$ | $V_{DDQ}$ | $\overline{KD0}$ | $V_{SS}$ | QVLD0 | $V_{SS}$ | $\overline{CQ0}$ |
| **M** | $V_{SS}$ | Q13 | $V_{SS}$ | D13 | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | $NU_I$ | $V_{SS}$ | $NU_O$ | $V_{SS}$ |
| **N** | $NU_O$ | $V_{DDQ}$ | $NU_I$ | $V_{DDQ}$ | MCL | $V_{DDQ}$ | $\overline{R}$ | $V_{DDQ}$ | MCH | $V_{DDQ}$ | D5 | $V_{DDQ}$ | Q5 |
| **P** | $NU_O$ | Q12 | $NU_I$ | D12 | $V_{SS}$ | SA | MZT0 | SA | $V_{SS}$ | $NU_I$ | D6 | $NU_O$ | Q6 |
| **R** | $V_{SS}$ | Q11 | $V_{SS}$ | D11 | MCH | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | RST | $NU_I$ | $V_{SS}$ | $NU_O$ | $V_{SS}$ |
| **T** | $NU_O$ | $V_{DDQ}$ | $NU_I$ | $V_{DD}$ | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | $V_{DD}$ | D7 | $V_{DDQ}$ | Q7 |
| **U** | $V_{SS}$ | Q10 | $V_{SS}$ | D10 | $NU_I$ | $V_{DDQ}$ | MCL | $V_{DDQ}$ | $NU_I$ | $NU_I$ | $V_{SS}$ | $NU_O$ | $V_{SS}$ |
| **V** | $NU_O$ | $V_{DDQ}$ | $NU_I$ | $V_{DDQ}$ | $V_{SS}$ | SA (x18) | $V_{DD}$ | SA (B2) | $V_{SS}$ | $V_{DDQ}$ | D8 | $V_{DDQ}$ | Q8 |
| **W** | $V_{SS}$ | Q9 | $V_{SS}$ | D9 | TCK | MCH | NC (RSVD) | MCL | TMS | $NU_I$ | $V_{SS}$ | $NU_O$ | $V_{SS}$ |
| **Y** | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | TDO | ZT | MCH | MCL | TDI | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ |

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**Notes:**

1. Pins 5A, 5N, 7A, 7U, 8W, and 8Y must be tied Low in this device.
2. Pins 5R, 6W, 7Y, and 9N must be tied High in this device.
3. Pins 5U and 9U are unused in this device. They must be left unconnected or driven Low.
4. Pin 6A is defined as mode pin CFG in the pinout standard. It must be tied High in this device to select x18 configuration.
5. Pin 8B is defined as mode pin SIOM in the pinout standard. It must be tied High in this device to select Separate I/O configuration.
6. Pin 6B is defined as mode pin B4M in the pinout standard. It must be tied Low in this device to select Burst-of-2 configuration.
7. Pin 6V is defined as address pin SA for x18 devices. It is used in this device.
8. Pin 8V is defined as address pin SA for B2 devices. It is used in this device.
9. Pin 9D is reserved as address pin SA for 144 Mb devices. It is a true no connect in this device.
10. Pin 7D is reserved as address pin SA for 288 Mb devices. It is a true no connect in this device.

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## 2M x 36 (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | MCL | MCL (CFG) | MCL | ZQ | PZT1 | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ |
| **B** | $V_{SS}$ | Q35 | $V_{SS}$ | D35 | MVQ | MCL (B4M) | NC (RSVD) | MCH (SIOM) | PZT0 | D0 | $V_{SS}$ | Q0 | $V_{SS}$ |
| **C** | Q26 | $V_{DDQ}$ | D26 | $V_{DDQ}$ | $V_{SS}$ | SA | $V_{DD}$ | SA | $V_{SS}$ | $V_{DDQ}$ | D9 | $V_{DDQ}$ | Q9 |
| **D** | $V_{SS}$ | Q34 | $V_{SS}$ | D34 | SA | $V_{DDQ}$ | NC (288 Mb) | $V_{DDQ}$ | NC (144 Mb) | D1 | $V_{SS}$ | Q1 | $V_{SS}$ |
| **E** | Q25 | $V_{DDQ}$ | D25 | $V_{DD}$ | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | $V_{DD}$ | D10 | $V_{DDQ}$ | Q10 |
| **F** | $V_{SS}$ | Q33 | $V_{SS}$ | D33 | SA | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | SA | D2 | $V_{SS}$ | Q2 | $V_{SS}$ |
| **G** | Q24 | Q32 | D24 | D32 | $V_{SS}$ | SA | MZT1 | SA | $V_{SS}$ | D3 | D11 | Q3 | Q11 |
| **H** | Q23 | $V_{DDQ}$ | D23 | $V_{DDQ}$ | SA | $V_{DDQ}$ | $\overline{W}$ | $V_{DDQ}$ | SA | $V_{DDQ}$ | D12 | $V_{DDQ}$ | Q12 |
| **J** | $V_{SS}$ | Q31 | $V_{SS}$ | D31 | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | D4 | $V_{SS}$ | Q4 | $V_{SS}$ |
| **K** | CQ1 | $V_{DDQ}$ | $V_{REF}$ | $V_{DD}$ | KD1 | $V_{DD}$ | CK | $V_{DD}$ | KD0 | $V_{DD}$ | $V_{REF}$ | $V_{DDQ}$ | CQ0 |
| **L** | $\overline{CQ1}$ | $V_{SS}$ | QVLD1 | $V_{SS}$ | $\overline{KD1}$ | $V_{DDQ}$ | $\overline{CK}$ | $V_{DDQ}$ | $\overline{KD0}$ | $V_{SS}$ | QVLD0 | $V_{SS}$ | $\overline{CQ0}$ |
| **M** | $V_{SS}$ | Q22 | $V_{SS}$ | D22 | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | D13 | $V_{SS}$ | Q13 | $V_{SS}$ |
| **N** | Q30 | $V_{DDQ}$ | D30 | $V_{DDQ}$ | MCL | $V_{DDQ}$ | $\overline{R}$ | $V_{DDQ}$ | MCH | $V_{DDQ}$ | D5 | $V_{DDQ}$ | Q5 |
| **P** | Q29 | Q21 | D29 | D21 | $V_{SS}$ | SA | MZT0 | SA | $V_{SS}$ | D14 | D6 | Q14 | Q6 |
| **R** | $V_{SS}$ | Q20 | $V_{SS}$ | D20 | MCH | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | RST | D15 | $V_{SS}$ | Q15 | $V_{SS}$ |
| **T** | Q28 | $V_{DDQ}$ | D28 | $V_{DD}$ | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | $V_{DD}$ | D7 | $V_{DDQ}$ | Q7 |
| **U** | $V_{SS}$ | Q19 | $V_{SS}$ | D19 | $NU_I$ | $V_{DDQ}$ | MCL | $V_{DDQ}$ | $NU_I$ | D16 | $V_{SS}$ | Q16 | $V_{SS}$ |
| **V** | Q27 | $V_{DDQ}$ | D27 | $V_{DDQ}$ | $V_{SS}$ | $NU_I$ (x18) | $V_{DD}$ | SA (B2) | $V_{SS}$ | $V_{DDQ}$ | D8 | $V_{DDQ}$ | Q8 |
| **W** | $V_{SS}$ | Q18 | $V_{SS}$ | D18 | TCK | MCH | NC (RSVD) | MCL | TMS | D17 | $V_{SS}$ | Q17 | $V_{SS}$ |
| **Y** | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | TDO | ZT | MCH | MCL | TDI | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ |

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**Notes:**

1. Pins 5A, 5N, 7A, 7U, 8W, and 8Y must be tied Low in this device.
2. Pins 5R, 6W, 7Y, and 9N must be tied High in this device.
3. Pins 5U and 9U are unused in this device. They must be left unconnected or driven Low.
4. Pin 6A is defined as mode pin CFG in the pinout standard. It must be tied Low in this device to select x36 configuration.
5. Pin 8B is defined as mode pin SIOM in the pinout standard. It must be tied High in this device to select Separate I/O configuration.
6. Pin 6B is defined as mode pin B4M in the pinout standard. It must be tied Low in this device to select Burst-of-2 configuration.
7. Pin 6V is defined as address pin SA for x18 devices. It is unused in this device, and must be left unconnected or driven Low.
8. Pin 8V is defined as address pin SA for B2 devices. It is used in this device.
9. Pin 9D is reserved as address pin SA for 144 Mb devices. It is a true no connect in this device.
10. Pin 7D is reserved as address pin SA for 288 Mb devices. It is a true no connect in this device.

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## Pin Description

| Symbol | Description | Type |
|---|---|---|
| SA | **Address** — Read Address is registered on ↑CK and Write Address is registered on ↑$\overline{CK}$. | Input |
| D[35:0] | **Write Data** — Registered on ↑KD and ↑$\overline{KD}$ during Write operations.<br>D[17:0] - x18 and x36.<br>D[35:18] - x36 only. | Input |
| Q[35:0] | **Read Data** — Aligned with ↑CQ and ↑$\overline{CQ}$ during Read operations.<br>Q[17:0] - x18 and x36.<br>Q[35:18] - x36 only. | Output |
| QVLD[1:0] | **Read Data Valid**—Driven high one half cycle before valid read data. | Output |
| CK, $\overline{CK}$ | **Primary Input Clocks** — Dual single-ended. Used for latching address and control inputs, for internal timing control, and for output timing control. | Input |
| $\overline{KD}$[1:0], KD[1:0] | **Write Data Input Clocks** — Dual single-ended. Used for latching write data inputs.<br>KD0, $\overline{KD}$0: latch D[17:0] in x36, D[8:0] in x18.<br>KD1, $\overline{KD}$1: latch D[35:18] in x36, D[17:9] in x18. | Input |
| $\overline{CQ}$[1:0], CQ[1:0] | **Echo Clocks** — Free-running output (echo) clocks, tightly aligned with read data outputs. Facilitate source-synchronous operation.<br>CQ0, $\overline{CQ}$0: align with Q[17:0] in x36, Q[8:0] in x18.<br>CQ1, $\overline{CQ}$1: align with Q[35:18] in x36, Q[17:9] in x18. | Output |
| $\overline{R}$ | **Read Enable** — Registered on ↑CK. $\overline{R}$ = 0 initiates a Read operation. | Input |
| $\overline{W}$ | **Write Enable** — Registered on ↑CK. $\overline{W}$ = 0 initiates a Write operation. | Input |
| RST | **Reset** — Holds the device inactive and resets the device to its initial power-on state when asserted High. Weakly pulled Low internally. | Input |
| ZQ | **Driver Impedance Control Resistor Input** — Must be connected to $V_{SS}$ through an external resistor RQ to program driver impedance. | Input |
| ZT | **ODT Impedance Control Resistor Input** — Must be connected to $V_{SS}$ through an external resistor RT to program ODT impedance. | Input |
| MZT[1:0] | **ODT Mode Select** — Set the ODT state globally for all input groups. Must be tied High or Low.<br>MZT[1:0] = 00: disables ODT on all input groups, regardless of PZT[1:0].<br>MZT[1:0] = 01: enables strong ODT on select input groups, as specified by PZT[1:0].<br>MZT[1:0] = 10: enables weak ODT on select input groups, as specified by PZT[1:0].<br>MZT[1:0] = 11: reserved. | Input |
| PZT[1:0] | **ODT Configuration Select** — Set the ODT state for various combinations of input groups when MZT[1:0] = 01 or 10. Must be tied High or Low.<br>PZT[1:0] = 00: enables ODT on write data only.<br>PZT[1:0] = 01: enables ODT on write data and input clocks.<br>PZT[1:0] = 10: enables ODT on write data, address, and control.<br>PZT[1:0] = 11: enables ODT on write data, input clocks, address, and control. | Input |

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## Pin Description (Continued)

| Symbol | Description | Type |
|---|---|---|
| MVQ | **I/O Voltage Select** — Indicates what voltage is supplied to the $V_{DDQ}$ pins. Must be tied High or Low.<br>MVQ = 0: Configure for 1.2V or 1.35V nominal $V_{DDQ}$.<br>MVQ = 1: Configure for 1.5V nominal $V_{DDQ}$. | Input |
| $V_{DD}$ | **Core Power Supply** — 1.35V nominal core supply voltage. | — |
| $V_{DDQ}$ | **I/O Power Supply** — 1.2V or 1.35V or 1.5V nominal I/O supply voltage. Configurable via MVQ pin. | — |
| $V_{REF}$ | **Input Reference Voltage** — Input buffer reference voltage. | — |
| $V_{SS}$ | **Ground** | — |
| TCK | **JTAG Clock** | Input |
| TMS | **JTAG Mode Select** — Weakly pulled High internally. | Input |
| TDI | **JTAG Data Input** — Weakly pulled High internally. | Input |
| TDO | **JTAG Data Output** | Output |
| MCH | **Must Connect High** — May be tied to $V_{DDQ}$ directly or via a 1kΩ resistor. | Input |
| MCL | **Must Connect Low** — May be tied to $V_{SS}$ directly or via a 1kΩ resistor. | Input |
| NC | **No Connect** — There is no internal chip connection to these pins. They may be left unconnected, or tied High or Low. | — |
| $NU_I$ | **Not Used Input** — There is an internal chip connection to these input pins, but they are unused by the device. They are pulled Low internally. They may be left unconnected or tied/driven Low. They should not be tied/driven High. | Input |
| $NU_O$ | **Not Used Output** — There is an internal chip connection to these output pins, but they are unused by the device. The drivers are tri-stated internally. They should be left unconnected. | Output |

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## Power-Up and Reset Requirements

For reliability purposes, power supplies must power up simultaneously, or in the following sequence:
$V_{SS}$, $V_{DD}$, $V_{DDQ}$, $V_{REF}$ and inputs.
Power supplies must power down simultaneously, or in the reverse sequence.

After power supplies power up, the following start-up sequence must be followed.

**Step 1 (Recommended, but not required)**: Assert RST High for at least 1ms.
While RST is asserted high:
• Read and Write operations are ignored.

**Note**: If possible, RST should be asserted High before input clocks (begin toggling, and remain asserted High until input clocks are stable and toggling within specification, in order to prevent unstable, out-of-spec input clocks from causing trouble in the SRAM.

**Step 2:** Begin toggling input clocks.
After input clocks begin toggling, but not necessarily within specification:
• CQ, $\overline{CQ}$ begin toggling, but not necessarily within specification.

**Step 3**: Wait until input clocks are stable and toggling within specification.

**Step 4**: De-assert RST Low (if asserted High).

**Step 5**: Wait at least 160K (163,840) cycles for driver and ODT impedances to calibrate.
After the impedances have calibrated:
• CQ, $\overline{CQ}$ begin toggling within specification.

**Step 6**: Begin initiating Read and Write operations.

### Reset Usage

Although not generally recommended, RST may be asserted High at any time after completion of the initial power-up sequence described above, to reset the SRAM control logic to its initial power-on state. However, whenever RST is subsequently de-asserted Low (as in Step 4 in the power up sequence), at least 160K NOP cycles must be initiated (as in Step 5 in the power-up sequence) before Read and Write operations are initiated.

**Note**: Memory array content may be perturbed/corrupted when RST is asserted High.

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## Error Correction (ECC)

These devices implement a single-bit error detection and correction algorithm (specifically, a Hamming Code) on each DDR data word (comprising two 9-bit data bytes) transmitted on each 9-bit data bus (i.e., transmitted on D/Q[8:0], D/Q[17:9], D/Q[26:18], and D/Q[35:27]). To accomplish this, 5 ECC parity bits (invisible to the user) are utilized per every 18 data bits (visible to the user).

The ECC algorithm neither corrects nor detects multi-bit errors. However, ECCRAMs are architected in such a way that a single SER event very rarely causes a multi-bit error across any given "transmitted data unit", where a "transmitted data unit" represents the data transmitted as the result of a single read or write operation to a particular address. The extreme rarity of multi-bit errors results in the SER mentioned previously (i.e., <0.002 FITs/Mb (measured at sea level)).

Not only does the on-chip ECC significantly improve SER performance, but it also frees up the entire memory array for data storage. Frequently, SRAM applications allocate 1/9th of the memory array (i.e., one "error bit" per eight "data bits") for error detection (either simple parity error detection, or system-level ECC error detection and correction). Such error-bit allocation is unnecessary with ECCRAMs; the entire memory array can be utilized for data storage, effectively providing 12.5% greater storage capacity compared to SRAMs of the same density not equipped with on-chip ECC.

## Input Timing

These devices utilize three pairs of positive and negative input clocks, CK & $\overline{CK}$ and KD[1:0] & $\overline{KD}$[1:0], to latch the various synchronous inputs. Specifically:

↑CK and ↑$\overline{CK}$ latch all address (SA) inputs.

↑CK latches all control ($\overline{R}$, $\overline{W}$) inputs.

↑KD[1:0] and ↑$\overline{KD}$[1:0] latch particular write data (D) inputs, as follows:

- ↑KD0 and ↑$\overline{KD}$0 latch D[17:0] in x36, and D[8:0] in x18.
- ↑KD1 and ↑$\overline{KD}$1 latch D[35:18] in x36, and D[17:9] in x18.

## Output Timing

These devices provide two pairs of positive and negative output clocks (aka "echo clocks"), CQ[1:0] & $\overline{CQ}$[1:0], whose timing is tightly aligned with read data in order to enable reliable source-synchronous data transmission.

Output timing is generated by ↑CK and ↑$\overline{CK}$, as follows:

- ↑$\overline{CK}$ generates ↑CQ[1:0], ↓$\overline{CQ}$[1:0], Q1 active, and Q2 inactive.
- . ↑$\overline{CK}$ generates ↑$\overline{CQ}$[1:0], ↓CQ[1:0], Q1 inactive, Q2 active, and QVLD active/inactive.

**Note**: Q1 and Q2 indicate the first and second pieces of read data transferred in any given clock cycle during Read operations.

↑CQ[1:0] and ↑$\overline{CQ}$[1:0] align with particular read data (Q) and read data valid (QVLD) outputs, as follows:

- ↑CQ0 and ↑$\overline{CQ0}$ align with Q[17:0], QVLD0 in x36, and with Q[8:0], QVLD0 in x18.
- ↑CQ1 and ↑$\overline{CQ1}$ align with Q[35:18], QLVD1 in x36, and with Q[17:9], QVLD1 in x18.

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## Driver Impedance Control

**Programmable Driver Impedance** is implemented on the following output signals:

• CQ, $\overline{CQ}$, Q, QVLD.

Driver impedance is programmed by connecting an external resistor RQ between the ZQ pin and $V_{SS}$.

Driver impedance is set to the programmed value within 160K cycles after input clocks are operating within specification and RST is de-asserted Low. It is updated periodically thereafter to compensate for temperature and voltage fluctuations in the system.

| Output Signal | Pull-Down Impedance ($R_{OUTL}$) | Pull-Up Impedance ($R_{OUTH}$) |
|---|---|---|
| CQ, $\overline{CQ}$, Q, QVLD | RQ*0.2 ± 15% | RQ*0.2 ± 15% |

**Notes:**

1. $R_{OUTL}$ and $R_{OUTH}$ apply when 175Ω ≤ RQ ≤ 225Ω..
2. The mismatch between $R_{OUTL}$ and $R_{OUTH}$ is less than 10%, guaranteed by design.

## ODT Impedance Control

**Programmable ODT Impedance** is implemented on the following input signals:

• CK, $\overline{CK}$, KD, $\overline{KD}$, SA, $\overline{R}$, $\overline{W}$, D.

ODT impedance is programmed by connecting an external resistor RT between the ZT pin and $V_{SS}$.

ODT impedance is set to the programmed value within 160K cycles after input clocks are operating within specification and RST is de-asserted Low. It is updated periodically thereafter to compensate for temperature and voltage fluctuations in the system

| Input Signal | PZT[1:0] | MZT[1:0] | Pull-Down Impedance ($R_{INL}$) | Pull-Up Impedance ($R_{INH}$) |
|---|---|---|---|---|
| CK, $\overline{CK}$, KD, $\overline{KD}$ | X0 | XX | disabled | disabled |
| | X1 | 01 | RT ± 15% | RT ± 15% |
| | | 10 | RT*2 ± 20% | RT*2 ± 20% |
| SA, $\overline{R}$, $\overline{W}$ | 0X | XX | disabled | disabled |
| | 1X | 01 | RT ± 15% | RT ± 15% |
| | | 10 | RT*2 ± 20% | RT*2 ± 20% |
| D | XX | 01 | RT ± 15% | RT ± 15% |
| | | 10 | RT*2 ± 20% | RT*2 ± 20% |

**Notes:**

1. When MZT[1:0] = 00, ODT is disabled on all inputs. MZT[1:0] = 11 is reserved for future use.
2. $R_{INL}$ and $R_{INH}$ apply when 105Ω ≤ RT ≤ 135Ω.
3. The mismatch between $R_{INL}$ and $R_{INH}$ is less than 10%, guaranteed by design.
4. All ODT is disabled during JTAG EXTEST and SAMPLE-Z instructions.

**Note:** When ODT impedance is enabled on a particular input, that input should always be driven High or Low; it should never be tri-stated (i.e., in a High- Z state). If the input is tri-stated, the ODT will pull the signal to $V_{DDQ}$ / 2 (i.e., to the switch point of the diff-amp receiver), which could cause the receiver to enter a meta-stable state and consume more power than it normally would. This could result in the device's operating currents being higher.

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## Truth Table

| SA | | $\overline{R}$ | $\overline{W}$ | Current Operation | D | | Q | |
|---|---|---|---|---|---|---|---|---|
| ↑CK ($t_n$) | ↑$\overline{CK}$ ($t_{n+½}$) | ↑CK ($t_n$) | ↑CK ($t_n$) | ($t_n$) | ↑KD ($t_n$) | ↑$\overline{KD}$ ($t_{n+½}$) | ↑CQ ($t_{n+3}$) | ↑$\overline{CQ}$ ($t_{n+3½}$) |
| X | X | 1 | 1 | NOP | X | X | Hi-Z / 0 | |
| X | V | 1 | 0 | Write Only | D1 | D2 | Hi-Z / 0 | |
| V | X | 0 | 1 | Read Only | X | X | Q1 | Q2 |
| V | V | 0 | 0 | Read + Write | D1 | D2 | Q1 | Q2 |

**Notes:**

1. 1 = High; 0 = Low; V = Valid (High or Low); X = Don't Care.
2. D1 and D2 indicate the first and second pieces of write data transferred during Write operations.
3. Q1 and Q2 indicate the first and second pieces of read data transferred during Read operations.
4. When D ODT is disabled (MZT[1:0] = 00), Q pins are tri-stated for one cycle in response to NOP and Write Only commands, 3 cycles after the command is sampled.
5. When D ODT is enabled (MZT[1:0] = 01 or 10), Q pins are driven Low for one cycle in response to NOP and Write Only commands, 3 cycles after the command is sampled.

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## Electrical Specifications

### Absolute Maximum Ratings

| Parameter | Symbol | Rating | Units |
|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | -0.3 to +1.6 | V |
| I/O Supply Voltage when MVQ = 0 | $V_{DDQ}$ | -0.3 to $V_{DD}$ | V |
| I/O Supply Voltage when MVQ = 1 | $V_{DDQ}$ | -0.3 to $V_{DD}$ + 0.3 | V |
| Input Voltage when MVQ = 0 | $V_{IN}$ | -0.3 to $V_{DDQ}$ + 0.3 (1.7 max) | V |
| Input Voltage when MVQ = 1 | $V_{IN}$ | -0.3 to $V_{DDQ}$ + 0.3 (2.0 max) | V |
| Maximum Junction Temperature | $T_J$ | 125 | °C |
| Storage Temperature | $T_{STG}$ | -55 to 125 | °C |

**Note:**
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

### Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | 1.3 | 1.35 | 1.4 | V |
| I/O Supply Voltage - 1.2V nominal when MVQ = 0 | $V_{DDQ}$ | 1.15 | 1.2 | 1.25 | V |
| I/O Supply Voltage - 1.35V nominal when MVQ = 0 | $V_{DDQ}$ | 1.3 | 1.35 | $V_{DD}$ | V |
| I/O Supply Voltage - 1.5V nominal when MVQ = 1 | $V_{DDQ}$ | 1.4 | 1.5 | 1.6 | V |
| Commercial Junction Temperature | $T_{JC}$ | 0 | — | 85 | °C |
| Industrial Junction Temperature | $T_{JI}$ | -40 | — | 100 | °C |

**Note:**
For reliability purposes, power supplies must power up simultaneously, or in the following sequence:
$V_{SS}$, $V_{DD}$, $V_{DDQ}$, $V_{REF}$, and Inputs.
Power supplies must power down simultaneously, or in the reverse sequence.

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### Thermal Impedance

| Package | θ JA (C°/W) Airflow = 0 m/s | θ JA (C°/W) Airflow = 1 m/s | θ JA (C°/W) Airflow = 2 m/s | θ JB (C°/W) | θ JC (C°/W) |
|---|---|---|---|---|---|
| FBGA | 15.5 | 13.1 | 12.1 | 4.4 | 0.2 |

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## I/O Capacitance

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | — | 5.0 | pF | 1, 3 |
| Output Capacitance | $C_{OUT}$ | — | 5.5 | pF | 2, 3 |

**Notes:**
1. $V_{IN} = V_{DDQ}/2$.
2. $V_{OUT} = V_{DDQ}/2$.
3. $T_A = 25°C$, f = 1 MHz.

## Input Electrical Characteristics when MVQ = 0

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| DC Input Reference Voltage | $V_{REFdc}$ | 0.48 * $V_{DDQ}$ | 0.52 * $V_{DDQ}$ | V | — |
| DC Input High Voltage | $V_{IH1dc}$ | $V_{REF}$ + 0.08 | $V_{DDQ}$ + 0.15 | V | 4 |
| DC Input Low Voltage | $V_{IL1dc}$ | –0.15 | $V_{REF}$ – 0.08 | V | 4 |
| DC Input High Voltage | $V_{IH2dc}$ | 0.75 * $V_{DDQ}$ | $V_{DDQ}$ + 0.15 | V | 5 |
| DC Input Low Voltage | $V_{IL2dc}$ | –0.15 | 0.25 * $V_{DDQ}$ | V | 5 |
| AC Input Reference Voltage | $V_{REFac}$ | 0.47 * $V_{DDQ}$ | 0.53 * $V_{DDQ}$ | V | 1 |
| AC Input High Voltage | $V_{IH1ac}$ | $V_{REF}$ + 0.15 | $V_{DDQ}$ + 0.25 | V | 2, 3, 4 |
| AC Input Low Voltage | $V_{IL1ac}$ | –0.25 | $V_{REF}$ – 0.15 | V | 2, 3, 4 |
| AC Input High Voltage | $V_{IH2ac}$ | $V_{DDQ}$ – 0.2 | $V_{DDQ}$ + 0.25 | V | 2, 5 |
| AC Input Low Voltage | $V_{IL2ac}$ | – 0.25 | 0.2 | V | 2, 5 |

**Notes:**
1. $V_{REFac}$ is equal to $V_{REFdc}$ plus noise.
2. $V_{IH}$ max and $V_{IL}$ min apply for pulse widths less than one-quarter of the cycle time.
3. Input rise and fall times must be a minimum of 1 V/ns, and within 10% of each other.
4. Applies to: CK, $\overline{CK}$, KD, $\overline{KD}$, SA, $\overline{R}$, $\overline{W}$, D.
5. Applies to: RST, MVQ, MZT, PZT.

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## Input Electrical Characteristics when MVQ = 1

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| DC Input Reference Voltage | $V_{REFdc}$ | 0.47 * $V_{DDQ}$ | 0.53 * $V_{DDQ}$ | V | — |
| DC Input High Voltage | $V_{IH1dc}$ | $V_{REF}$ + 0.1 | $V_{DDQ}$ + 0.15 | V | 4 |
| DC Input Low Voltage | $V_{IL1dc}$ | –0.15 | $V_{REF}$ – 0.1 | V | 4 |
| DC Input High Voltage | $V_{IH2dc}$ | 0.75 * $V_{DDQ}$ | $V_{DDQ}$ + 0.15 | V | 5 |
| DC Input Low Voltage | $V_{IL2dc}$ | –0.15 | 0.25 * $V_{DDQ}$ | V | 5 |
| AC Input Reference Voltage | $V_{REFac}$ | 0.46 * $V_{DDQ}$ | 0.54 * $V_{DDQ}$ | V | 1 |
| AC Input High Voltage | $V_{IH1ac}$ | $V_{REF}$ + 0.2 | $V_{DDQ}$ + 0.25 | V | 2, 3, 4 |
| AC Input Low Voltage | $V_{IL1ac}$ | –0.25 | $V_{REF}$ – 0.2 | V | 2, 3, 4 |
| AC Input High Voltage | $V_{IH2ac}$ | $V_{DDQ}$ – 0.2 | $V_{DDQ}$ + 0.25 | V | 2, 5 |
| AC Input Low Voltage | $V_{IL2ac}$ | –0.25 | 0.2 | V | 2, 5 |

**Notes:**
1. $V_{REFac}$ is equal to $V_{REFdc}$ plus noise.
2. $V_{IH}$ max and $V_{IL}$ min apply for pulse widths less than one-quarter of the cycle time.
3. Input rise and fall times must be a minimum of 1V/ns, and within 10% of each other.
4. Applies to: CK, $\overline{CK}$, KD, $\overline{KD}$, SA, $\overline{R}$, $\overline{W}$, D.
5. Applies to: RST, MVQ, MZT, PZT.

## Output Electrical Characteristics

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| DC Output High Voltage | $V_{OHdc}$ | — | $V_{DDQ}$ + 0.15 | V | 1 |
| DC Output Low Voltage | $V_{OLdc}$ | -0.15 | — | V | 1 |
| AC Output High Voltage | $V_{OHac}$ | — | $V_{DDQ}$ + 0.25 | V | 1 |
| AC Output Low Voltage | $V_{OLac}$ | -0.25 | — | V | 1 |

**Notes:**
1. Applies to: CQ, $\overline{CQ}$, Q, QVLD.

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## Leakage Currents

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI1}$ | -2 | 2 | uA | 1, 2 |
| | $I_{LI2}$ | -20 | 2 | uA | 1, 3 |
| | $I_{LI3}$ | -2 | 20 | uA | 1, 4 |
| Output Leakage Current | $I_{LO}$ | -2 | 2 | uA | 5, 6 |

**Notes:**
1. $V_{IN} = V_{SS}$ to $V_{DDQ}$.
2. Applies to: CK, $\overline{CK}$, KD, $\overline{KD}$, SA, $\overline{R}$, $\overline{W}$, D when ODT is disabled.
   Applies to: MVQ, MZT, PZT, TCK.
3. Applies to: TMS, TDI (weakly pulled up).
4. Applies to: RST (weakly pulled down).
5. $V_{OUT} = V_{SS}$ to $V_{DDQ}$.
6. Applies to: CQ, $\overline{CQ}$, Q, QVLD, TDO.

## Operating Currents

| Parameter | Symbol | Operating Frequency | @ 1.3V $V_{DD}$ | @ 1.35V $V_{DD}$ | @ 1.4V $V_{DD}$ | Units |
|---|---|---|---|---|---|---|
| x18 Operating Current | $I_{DD}$ | 725 MHz | 2140 | 2260 | 2380 | mA |
| | | 625 MHz | 1900 | 2000 | 2110 | mA |
| | | 550 MHz | 1720 | 1820 | 1930 | mA |
| x36 Operating Current | $I_{DD}$ | 725 MHz | 3020 | 3170 | 3330 | mA |
| | | 625 MHz | 2680 | 2820 | 2970 | mA |
| | | 550 MHz | 2410 | 2540 | 2670 | mA |

**Notes:**
1. $I_{OUT}$ = 0 mA; $V_{IN} = V_{IH}$ or $V_{IL}$.
2. Applies at 100% Reads + Writes.

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## AC Test Conditions for 1.2V nominal $V_{DDQ}$ (MVQ = 0)

| Parameter | Symbol | Conditions | Units |
|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | 1.3 to 1.4 | V |
| I/O Supply Voltage | $V_{DDQ}$ | 1.15 to 1.25 | V |
| Input Reference Voltage | $V_{REF}$ | 0.6 | V |
| Input High Level | $V_{IH}$ | 0.9 | V |
| Input Low Level | $V_{IL}$ | 0.3 | V |
| Input Rise and Fall Time | — | 2.0 | V/ns |
| Input and Output Reference Level | — | 0.6 | V |

**Note:**
Output Load Conditions RQ = 200Ω. Refer to figure below.

## AC Test Conditions for 1.5V nominal $V_{DDQ}$ (MVQ = 1)

| Parameter | Symbol | Conditions | Units |
|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | 1.3 to 1.4 | V |
| I/O Supply Voltage | $V_{DDQ}$ | 1.4 to 1.6 | V |
| Input Reference Voltage | $V_{REF}$ | 0.75 | V |
| Input High Level | $V_{IH}$ | 1.25 | V |
| Input Low Level | $V_{IL}$ | 0.25 | V |
| Input Rise and Fall Time | — | 2.0 | V/ns |
| Input and Output Reference Level | — | 0.75 | V |

**Note:**
Output Load Conditions RQ = 200Ω. Refer to figure below.

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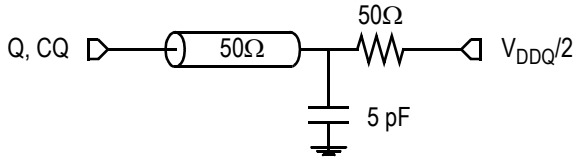
### AC Test Output Load

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## AC Timing Specifications

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| **Input Clock Timing (Met by the IP)** | | | | | |
| Clk Cycle Time (-725) | $t_{KHKH}$ | 1.38 | — | ns | 1 |
| Clk Cycle Time (-625) | | 1.6 | | | |
| Clk Cycle Time (-550) | | 1.8 | | | |
| Clk High Pulse Width | $t_{KHKL}$ | 0.45 | — | cycles | 1 |
| Clk Low Pulse Width | $t_{KLKH}$ | 0.45 | — | cycles | 1 |
| Clk High to $\overline{\text{Clk}}$ High | $t_{KH\overline{K}H}$ | 0.45 | 0.55 | cycles | 2 |
| Clk High to Write Data Clk High | $t_{KHKDH}$ | -200 | 200 | ps | 3 |
| **Input Timing (Met by the IP)** | | | | | |
| Input Valid to Clk High | $t_{IVKH}$ | not specified | — | ps | 4 |
| Clk High to Input Hold | $t_{KHIX}$ | not specified | — | ps | 4 |
| Input Pulse Width | $t_{IPW}$ | 200 | — | ps | 5 |
| **Output Timing (Accounted for by the IP)** | | | | | |
| Clk High to Data Output Valid / Hold | $t_{KHQV/X}$ | 1.0 | 2.5 | ns | 6 |
| Clk High to Echo Clock High | $t_{KHCQH}$ | 1.0 | 2.5 | ns | 7 |
| Echo Clk High to $\overline{\text{Echo Clk}}$ High | $t_{CQH\overline{CQH}}$ | $t_{KH\overline{K}H}$ (min) - 50 | $t_{KH\overline{K}H}$ (max) + 50 | ps | 8, 11 |
| $\overline{\text{Echo Clk}}$ High to Echo Clk High | $t_{\overline{CQH}CQH}$ | $t_{\overline{K}HKH}$ (min) - 50 | $t_{\overline{K}HKH}$ (max) + 50 | ps | 9, 11 |
| Echo Clk High to Data Output Valid / Hold | $t_{CQHQV/X}$ | -150 | 150 | ps | 10, 11 |

**Notes:**

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal.

1. Parameters apply to CK, $\overline{\text{CK}}$, KD, $\overline{\text{KD}}$.
2. Parameters specify ↑CK → ↑$\overline{\text{CK}}$ and ↑KD → ↑$\overline{\text{KD}}$ requirements.
3. Parameters specify ↑CK → ↑KD and ↑$\overline{\text{CK}}$ → ↑$\overline{\text{KD}}$ requirements.
4. Parameters apply to SA, and are referenced to ↑CK & ↑$\overline{\text{CK}}$.
   Parameters apply to R, W, and are referenced to ↑CK.
   Parameters apply to D, and are referenced to ↑KD & ↑$\overline{\text{KD}}$.
   The unspecified setup and hold time requirements for these inputs are met by the IP (via per-pin calibration for the DDR inputs).
5. Parameter applies to SA, R, W, D.
6. Parameters apply to Q and are referenced to ↑CK & ↑$\overline{\text{CK}}$.
7. Parameters specify ↑CK → ↑CQ and ↑$\overline{\text{CK}}$ → ↑$\overline{\text{CQ}}$ timing.
8. Parameter specifies ↑CQ → ↑$\overline{\text{CQ}}$ timing. $t_{KH\overline{K}H}$ (min) and $t_{KH\overline{K}H}$ (max) are the minimum and maximum input delays from ↑CK to ↑$\overline{\text{CK}}$.
9. Parameter specifies ↑$\overline{\text{CQ}}$ → ↑CQ timing. $t_{\overline{K}HKH}$ (min) and $t_{\overline{K}HKH}$ (max) are the minimum and maximum input delays from ↑$\overline{\text{CK}}$ to ↑CK.
10. Parameters apply to Q, QVLD and are referenced to ↑CQ & ↑$\overline{\text{CQ}}$.
11. Parameters are not tested. They are guaranteed by design, and verified through extensive corner-lot characterization.

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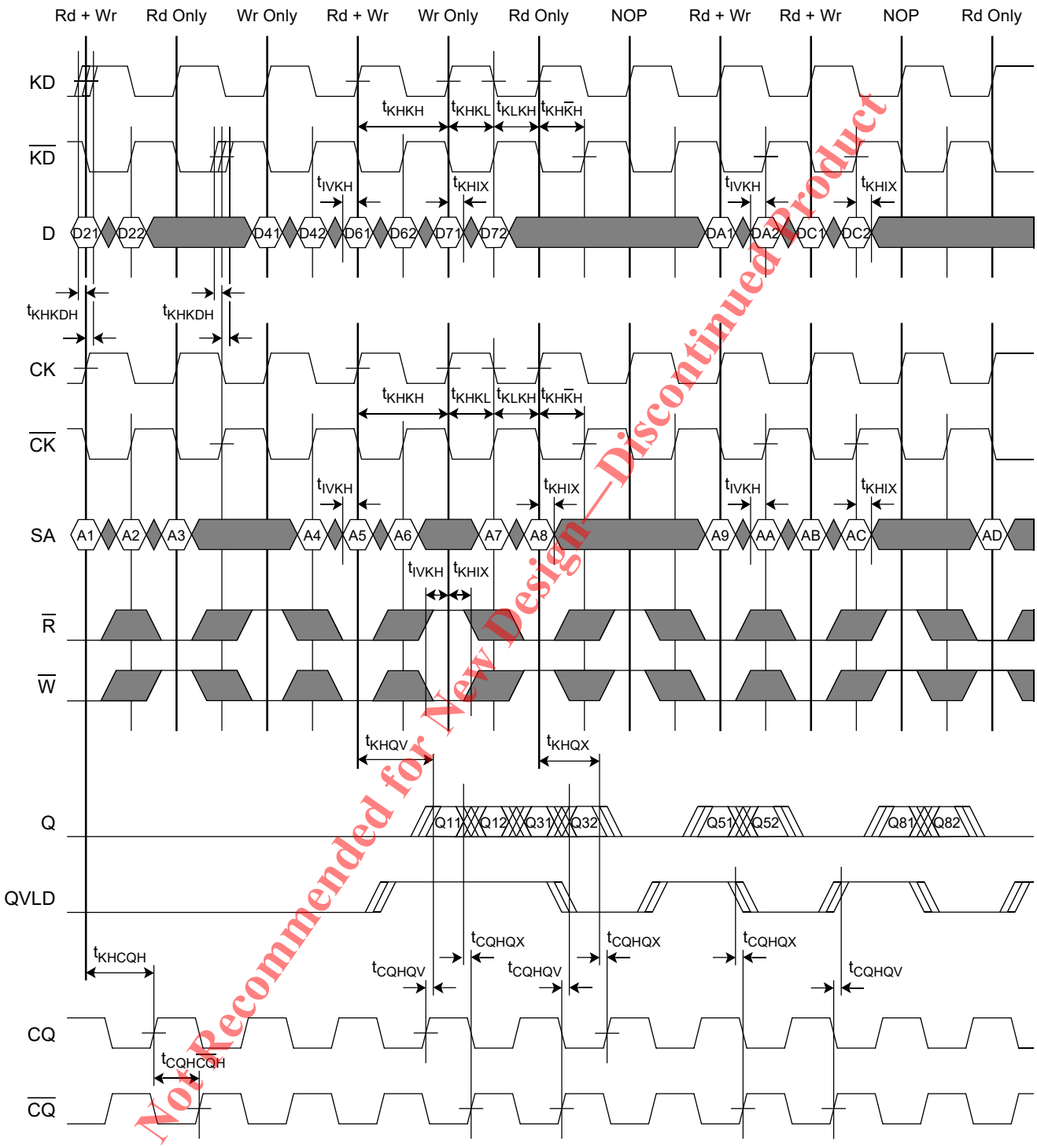
## Read and Write Timing Diagram

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## JTAG Test Mode Description

These devices provide a JTAG Test Access Port (TAP) and Boundary Scan interface using a limited set of IEEE std. 1149.1 functions. This test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), ECCRAM, other components, and the printed circuit board. In conformance with a subset of IEEE std. 1149.1, these devices contain a TAP Controller and multiple TAP Registers. The TAP Registers consist of one Instruction Register and multiple Data Registers.

The TAP consists of the following four signals:

| Pin | Pin Name | I/O | Description |
|---|---|---|---|
| TCK | Test Clock | I | Induces (clocks) TAP Controller state transitions. |
| TMS | Test Mode Select | I | Inputs commands to the TAP Controller. Sampled on the rising edge of TCK. |
| TDI | Test Data In | I | Inputs data serially to the TAP Registers. Sampled on the rising edge of TCK. |
| TDO | Test Data Out | O | Outputs data serially from the TAP Registers. Driven from the falling edge of TCK. |

### Concurrent TAP and Normal ECCRAM Operation

According to IEEE std. 1149.1, most public TAP Instructions do not disrupt normal device operation. In these devices, the only exceptions are EXTEST and SAMPLE-Z. See the Tap Registers section for more information.

### Disabling the TAP

When JTAG is not used, TCK should be tied Low to prevent clocking the ECCRAM. TMS and TDI should either be tied High through a pull-up resistor or left unconnected. TDO should be left unconnected.

## JTAG DC Operating Conditions

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| JTAG Input High Voltage | $V_{TIH}$ | 0.75 * $V_{DDQ}$ | $V_{DDQ}$ + 0.15 | V | 1 |
| JTAG Input Low Voltage | $V_{TIL}$ | –0.15 | 0.25 * $V_{DDQ}$ | V | 1 |
| JTAG Output High Voltage | $V_{TOH}$ | $V_{DDQ}$ – 0.2 | — | V | 2, 3 |
| JTAG Output Low Voltage | $V_{TOL}$ | — | 0.2 | V | 2, 4 |

**Notes:**

1. Parameters apply to TCK, TMS, and TDI during JTAG Testing.
2. Parameters apply to TDO during JTAG testing.
3. $I_{TOH}$ = –2.0 mA.
4. $I_{TOL}$ = 2.0 mA.

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## JTAG AC Timing Specifications

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| TCK Cycle Time | $t_{THTH}$ | 50 | — | ns |
| TCK High Pulse Width | $t_{THTL}$ | 20 | — | ns |
| TCK Low Pulse Width | $t_{TLTH}$ | 20 | — | ns |
| TMS Setup Time | $t_{MVTH}$ | 10 | — | ns |
| TMS Hold Time | $t_{THMX}$ | 10 | — | ns |
| TDI Setup Time | $t_{DVTH}$ | 10 | — | ns |
| TDI Hold Time | $t_{THDX}$ | 10 | — | ns |
| Capture Setup Time (Address, Control, Data, Clock) | $t_{CS}$ | 10 | — | ns |
| Capture Hold Time (Address, Control, Data, Clock) | $t_{CH}$ | 10 | — | ns |
| TCK Low to TDO Valid | $t_{TLQV}$ | — | 10 | ns |
| TCK Low to TDO Hold | $t_{TLQX}$ | 0 | — | ns |

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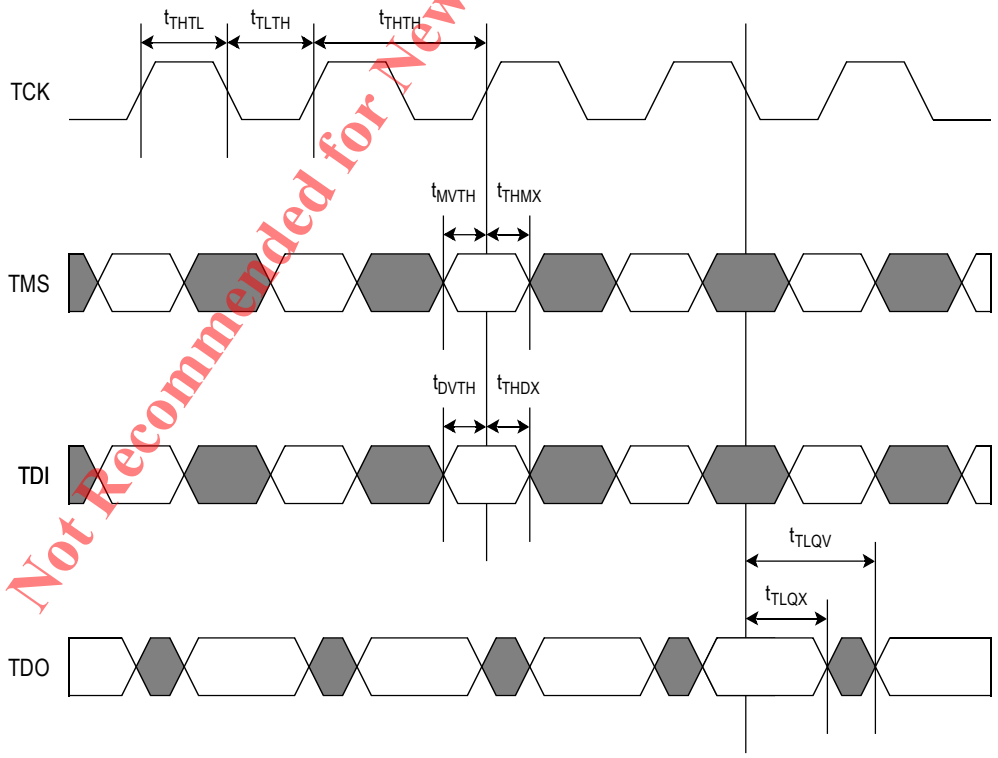
### JTAG Timing Diagram

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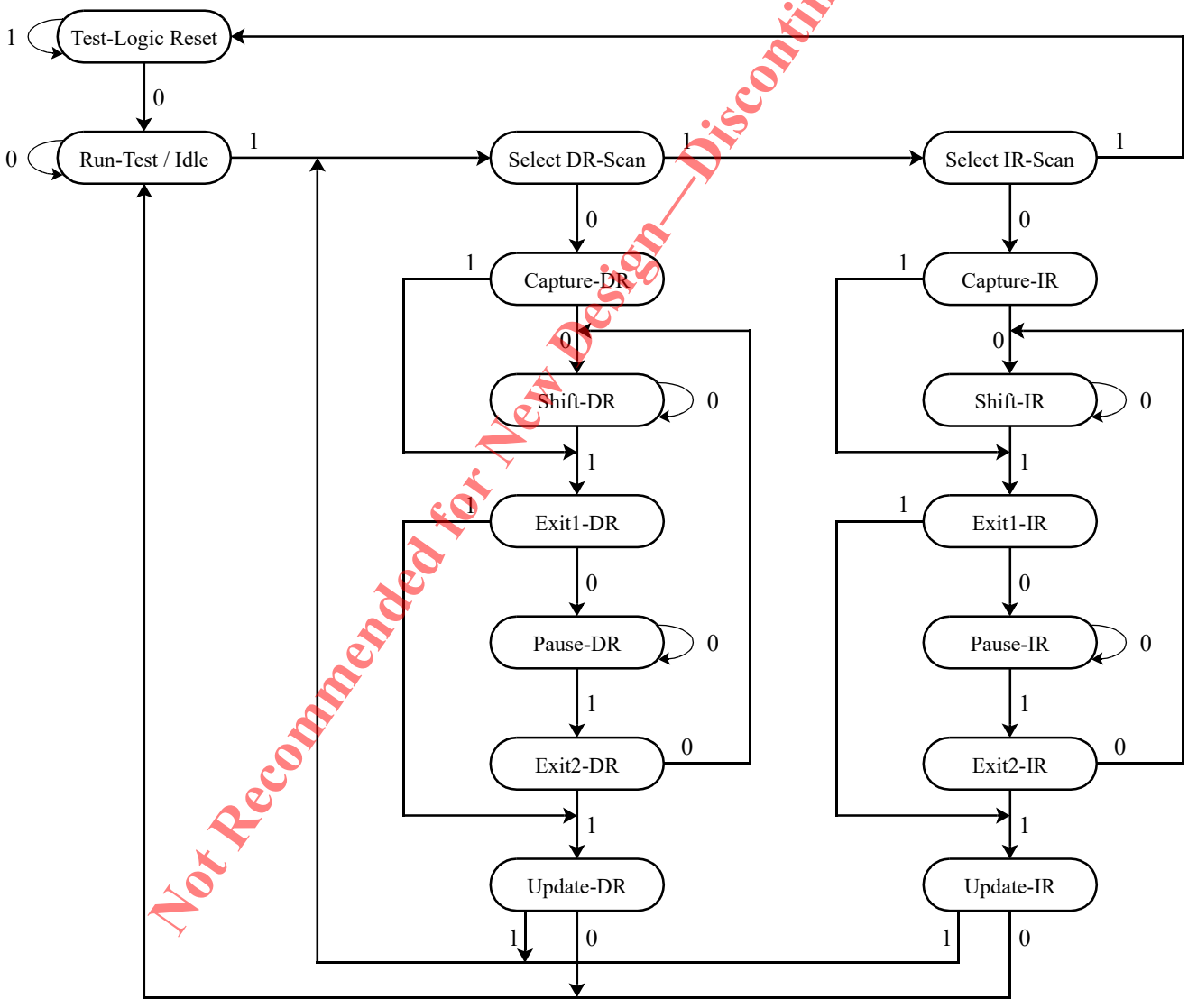
## TAP Controller

The TAP Controller is a 16-state state machine that controls access to the various TAP Registers and executes the operations associated with each TAP Instruction. State transitions are controlled by TMS and occur on the rising edge of TCK.
The TAP Controller enters the Test-Logic Reset state in one of two ways:

1. At power up.
2. When a logic 1 is applied to TMS for at least 5 consecutive rising edges of TCK.

The TDI input receiver is sampled only when the TAP Controller is in either the Shift-IR state or the Shift-DR state.
The TDO output driver is enabled only when the TAP Controller is in either the Shift-IR state or the Shift-DR state.

### TAP Controller State Diagram

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## TAP Registers

TAP Registers are serial shift registers that capture serial input data (from TDI) on the rising edge of TCK, and drive serial output data (to TDO) on the subsequent falling edge of TCK. They are divided into two groups: Instruction Registers (IR), which are manipulated via the IR states in the TAP Controller, and Data Registers (DR), which are manipulated via the DR states in the TAP Controller.

### Instruction Register (IR - 3 bits)

The Instruction Register stores the various TAP Instructions supported by ECCRAM. It is loaded with the IDCODE instruction (logic 001) at power-up, and when the TAP Controller is in the Test-Logic Reset and Capture-IR states. It is inserted between TDI and TDO when the TAP Controller is in the Shift-IR state, at which time it can be loaded with a new instruction. However, newly loaded instructions are not executed until the TAP Controller has reached the Update-IR state.

The Instruction Register is 3 bits wide, and is encoded as follows:

| Code (2:0) | Instruction | Description |
|---|---|---|
| 000 | EXTEST | Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>Also transfers the contents of the Boundary Scan Register associated with all output signals (Q, QVLD, CQ, $\overline{CQ}$) directly to their corresponding output pins. However, newly loaded Boundary Scan Register contents do not appear at the output pins until the TAP Controller has reached the Update-DR state.<br>Also disables all ODT.<br>See the Boundary Scan Register description for more information. |
| 001 | IDCODE | Loads a predefined device- and manufacturer-specific identification code into the ID Register when the TAP Controller is in the Capture-DR state, and inserts the ID Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>See the ID Register description for more information. |
| 010 | SAMPLE-Z | Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>Also disables all ODT.<br>Also forces Q output drivers to a High-Z state.<br>See the Boundary Scan Register description for more information. |
| 011 | PRIVATE | Reserved for manufacturer use only. |
| 100 | SAMPLE | Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>See the Boundary Scan Register description for more information. |
| 101 | PRIVATE | Reserved for manufacturer use only. |
| 110 | PRIVATE | Reserved for manufacturer use only. |
| 111 | BYPASS | Loads a logic 0 into the Bypass Register when the TAP Controller is in the Capture-DR state, and inserts the Bypass Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>See the Bypass Register description for more information. |

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### Bypass Register (DR - 1 bit)

The Bypass Register is one bit wide, and provides the minimum length serial path between TDI and TDO. It is loaded with a logic 0 when the BYPASS instruction has been loaded in the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the BYPASS instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

### ID Register (DR - 32 bits)

The ID Register is loaded with a predetermined device- and manufacturer-specific identification code when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

The ID Register is 32 bits wide, and is encoded as follows:

| See BSDL Model (31:12) | GSI ID (11:1) | Start Bit (0) |
|---|---|---|
| XXXX XXXX XXXX XXXX XXXX | 0001 1011 001 | 1 |

Bit 0 is the LSB of the ID Register, and Bit 31 is the MSB. When the ID Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

### Boundary Scan Register (DR - 127 bits)

The Boundary Scan Register is equal in length to the number of active signal connections to the ECCRAM (excluding the TAP pins) plus a number of place holder locations reserved for functional and/or density upgrades. It is loaded with the logic states of all signals composing the ECCRAM's I/O ring when the EXTEST, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the EXTEST, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

Additionally, the contents of the Boundary Scan Register associated with the ECCRAM outputs (Q, QVLD, CQ, $\overline{CQ}$) are driven directly to the corresponding ECCRAM output pins when the EXTEST instruction is selected. However, after the EXTEST instruction has been selected, any new data loaded into Boundary Scan Register when the TAP Controller is in the Shift-DR state does not appear at the output pins until the TAP Controller has reached the Update-DR state.

The value captured in the boundary scan register for NU pins is determined by the external pin state while the NC pins are 0 regardless of the external pin state. The value captured in the internal cells is 1.

### Output Driver State During EXTEST

EXTEST allows the Internal Cell (Bit 127) in the Boundary Scan Register to control the state of Q drivers. That is, when Bit 127 = 1, Q drivers are enabled (i.e., driving High or Low), and when Bit 127 = 0, Q drivers are disabled (i.e., forced to High-Z state). See the Boundary Scan Register section for more information.

### ODT State During EXTEST and SAMPLE-Z

ODT on all inputs is disabled during EXTEST and SAMPLE-Z.

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**Boundary Scan Register Bit Order Assignment**

The table below depicts the order in which the bits are arranged in the Boundary Scan Register. Bit 1 is the LSB and Bit 127 is the MSB. When the Boundary Scan Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

| Bit | Pad | Bit | Pad | Bit | Pad | Bit | Pad | Bit | Pad |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 7L | 27 | 10F | 53 | 10U | 79 | 3V | 105 | 3G |
| 2 | 7K | 28 | 12F | 54 | 13V | 80 | 1V | 106 | 2F |
| 3 | 9L | 29 | 11G | 55 | 11V | 81 | 4U | 107 | 4F |
| 4 | 9K | 30 | 13G | 56 | 12W | 82 | 2U | 108 | 1E |
| 5 | 8J | 31 | 10G | 57 | 10W | 83 | 3T | 109 | 3E |
| 6 | 7H | 32 | 12G | 58 | 8V | 84 | 1T | 110 | 2D |
| 7 | 9H | 33 | 11H | 59 | 9U | 85 | 4R | 111 | 4D |
| 8 | 7G | 34 | 13H | 60 | 8T | 86 | 2R | 112 | 1C |
| 9 | 8G | 35 | 10J | 61 | 9R | 87 | 3P | 113 | 3C |
| 10 | 9F | 36 | 12J | 62 | 8P | 88 | 1P | 114 | 2B |
| 11 | 8E | 37 | 13K | 63 | 9N | 89 | 4P | 115 | 4B |
| 12 | 7D | 38 | 13L | 64 | 8M | 90 | 2P | 116 | 6A |
| 13 | 9D | 39 | 11L | 65 | 6M | 91 | 3N | 117 | 6B |
| 14 | 8C | 40 | 12M | 66 | 7N | 92 | 1N | 118 | 6C |
| 15 | 8B | 41 | 10M | 67 | 5N | 93 | 4M | 119 | 5D |
| 16 | 9B | 42 | 13N | 68 | 7P | 94 | 2M | 120 | 6E |
| 17 | 7A | 43 | 11N | 69 | 6P | 95 | 3L | 121 | 5F |
| 18 | 9A | 44 | 12P | 70 | 5R | 96 | 1L | 122 | 6G |
| 19 | 10B | 45 | 10P | 71 | 6T | 97 | 1K | 123 | 5H |
| 20 | 12B | 46 | 13P | 72 | 7U | 98 | 2J | 124 | 6J |
| 21 | 11C | 47 | 11P | 73 | 5U | 99 | 4J | 125 | 5K |
| 22 | 13C | 48 | 12R | 74 | 6V | 100 | 1H | 126 | 5L |
| 23 | 10D | 49 | 10R | 75 | 6W | 101 | 3H | 127 | Internal |
| 24 | 12D | 50 | 13T | 76 | 7Y | 102 | 2G | | |
| 25 | 11E | 51 | 11T | 77 | 4W | 103 | 4G | | |
| 26 | 13E | 52 | 12U | 78 | 2W | 104 | 1G | | |

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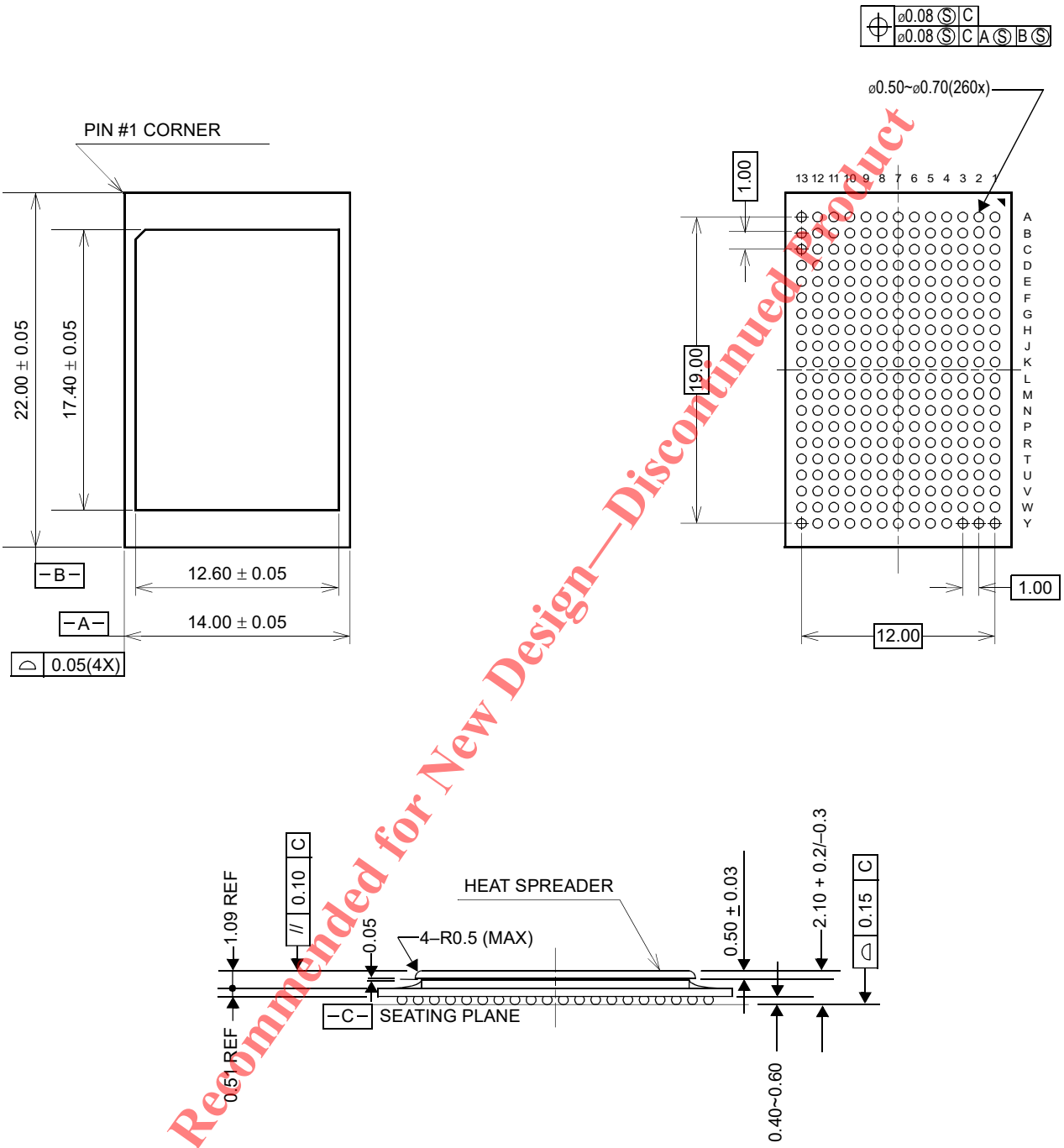
## 260-Pin BGA Package Drawing (Package K)

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| | | | |
|---|---|---|---|
| Ball Pitch: | 1.00 | Substrate Thickness: | 0.51 |
| Ball Diameter: | 0.60 | Mold Thickness: | — |

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## Ordering Information — GSI SigmaQuad-IIIe ECCRAMs

| Org | Part Number | Type | Package | Speed (MHz) | $T_A$ |
|---|---|---|---|---|---|
| 4M x 18 | GS8673EQ18BK-725S | SigmaQuad-IIIe B2 | 260 Pin BGA | 725 | C |
| 4M x 18 | GS8673EQ18BK-625S | SigmaQuad-IIIe B2 | 260 Pin BGA | 625 | C |
| 4M x 18 | GS8673EQ18BK-550S | SigmaQuad-IIIe B2 | 260 Pin BGA | 550 | C |
| 4M x 18 | GS8673EQ18BK-725IS | SigmaQuad-IIIe B2 | 260 Pin BGA | 725 | I |
| 4M x 18 | GS8673EQ18BK-625IS | SigmaQuad-IIIe B2 | 260 Pin BGA | 625 | I |
| 4M x 18 | GS8673EQ18BK-550IS | SigmaQuad-IIIe B2 | 260 Pin BGA | 550 | I |
| 2M x 36 | GS8673EQ36BK-725S | SigmaQuad-IIIe B2 | 260 Pin BGA | 725 | C |
| 2M x 36 | GS8673EQ36BK-625S | SigmaQuad-IIIe B2 | 260 Pin BGA | 625 | C |
| 2M x 36 | GS8673EQ36BK-550S | SigmaQuad-IIIe B2 | 260 Pin BGA | 550 | C |
| 2M x 36 | GS8673EQ36BK-725IS | SigmaQuad-IIIe B2 | 260 Pin BGA | 725 | I |
| 2M x 36 | GS8673EQ36BK-625IS | SigmaQuad-IIIe B2 | 260 Pin BGA | 625 | I |
| 2M x 36 | GS8673EQ36BK-550IS | SigmaQuad-IIIe B2 | 260 Pin BGA | 550 | I |

**Note:** C = Commercial Temperature Range. I = Industrial Temperature Range.

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## Revision History

| Rev. Code | Types of Changes Format or Content | Revisions |
|---|---|---|
| GS8673EQ1836BK_r1 | | Creation of new datasheet |
| GS8673EQ1836BK_r1_01 | Content | Corrected P/Ns for Industrial Temp Range (“I” before “S”) |
| GS8673EQ1836BK_r1_02 | Content | Redefined pin 5B from MCH to MVQ.<br>Added support for $V_{DDQ}$ = 1.2V (requires MVQ = 0). |
| GS8673EQ1836BK_r1_03 | Content | Redefined pins 3L, 11L from $DNU_O$ to QVLD1, QVLD0.<br>Redefined pins 9A, 9B from MCH to PZT1, PZT0.<br>Redefined pins 7G, 7P from MCL, MCH to MZT1, MZT0.<br>Added support for $V_{DDQ}$ = 1.35V (requires MVQ = 0).<br>Updated Power-Up and Reset Requirements section. |
| GS8673EQ1836BK_r1_04 | Content | Separated into BK and BGK datasheets due to BK EOL |

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